



**FAST CMOS
16-BIT REGISTERED
TRANSCIVER**

IDT54/74FCT162H952AT/BT/CT/ET

FEATURES:

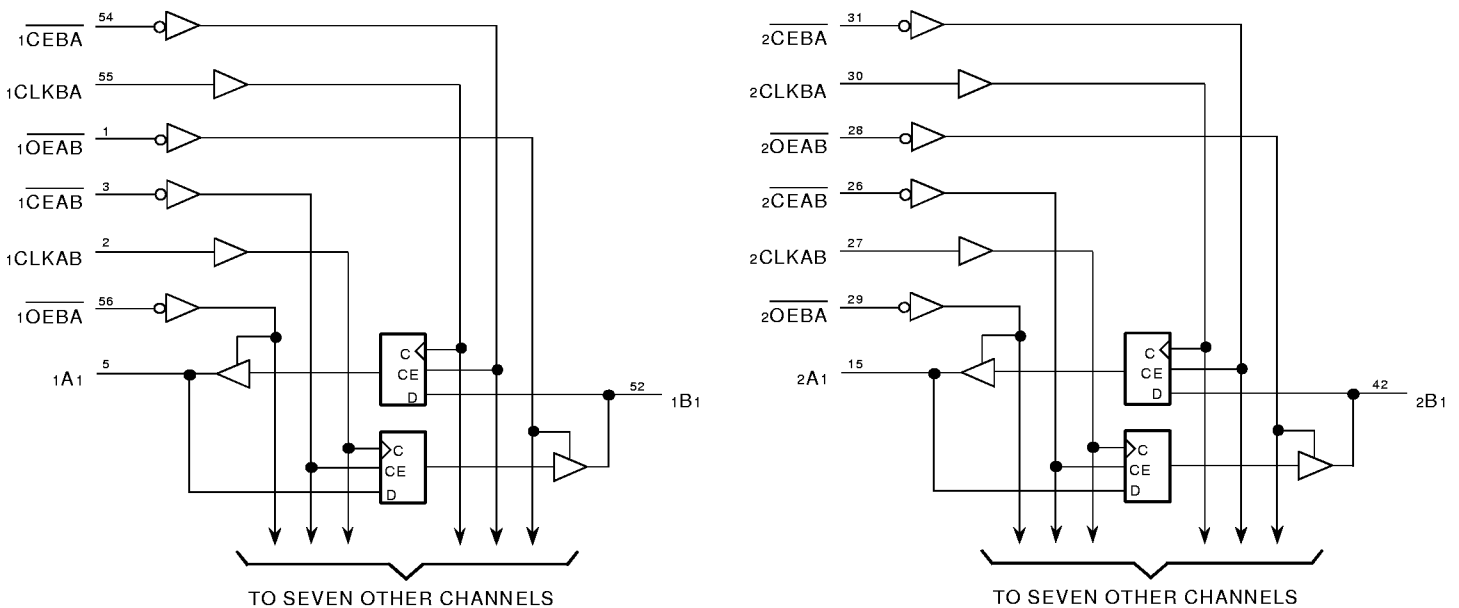
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical tsk(o) (Output Skew) < 250ps
- Low input and output leakage $\leq 1\mu A$ (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil pitch SSOP, 19.6 mil pitch TSSOP, 15.7 mil pitch TVSOP and 25 mil pitch CERPACK packages
- Extended commercial range of -40°C to +85°C
- Bus Hold retains last active bus state during 3-state
- Eliminates the need for external pull up resistors

DESCRIPTION:

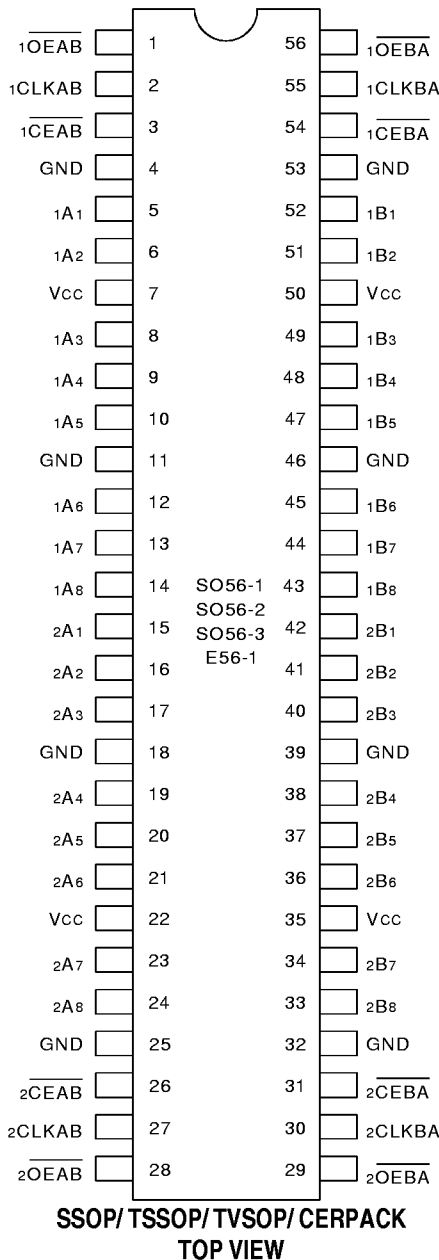
The FCT162H952AT/BT/CT/ET 16-bit registered transceiver is built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type registered transceivers with separate input and output control for independent control of data flow in either direction. For example, the A-to-B Enable ($x\overline{CEAB}$) must be LOW to enter data from the A port. $xCLKAB$ controls the clocking function. When $xCLKAB$ toggles from LOW-to-HIGH, the data present on the A port will be clocked into the register. $x\overline{OEAB}$ performs the output enable function on the B port. Data flow from the B port to A port is similar but requires using $x\overline{CEBA}$, $xCLKBA$, and $x\overline{OEBA}$ inputs. Full 16-bit operation is achieved by tying the control pins of the independent transceivers together.

The FCT162H952AT/BT/CT/ET has "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin Names	Description
\overline{xOEAB}	A-to-B Output Enable Input (Active LOW)
\overline{xOEBA}	B-to-A Output Enable Input (Active LOW)
\overline{xCEAB}	A-to-B Clock Enable Input (Active LOW)
\overline{xCEBA}	B-to-A Clock Enable Input (Active LOW)
xCLKAB	A-to-B Clock Input
xCLKBA	B-to-A Clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾

NOTE:

1. These pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to +7	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC}+0.5$	V
TSTG	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXXXT Output and I/O terminals.
- Output and I/O terminals for FCT162XXXXT.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	$V_{IN} = 0V$	3.5	6	pF
C _{OUT}	Output Capacitance	$V_{OUT} = 0V$	3.5	8	pF

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NOTE:

- This parameter is measured at characterization but not tested.

FUNCTION TABLE^(1,3)

Inputs				Outputs
\overline{xCEAB}	xCLKAB	\overline{xOEAB}	xAx	xBx
H	X	L	X	B ⁽²⁾
X	L	L	X	B ⁽²⁾
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

NOTES:

- A-to-B data flow is shown: B-to-A data flow is similar but uses \overline{xCEBA} , xCLKBA, and \overline{xOEBA} .
- Level of B before the indicated steady-state input conditions were established.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↑ = LOW-to-HIGH Transition
Z = High-impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS-HOLD)

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = -40°C to +85°C, VCC = 5.0V ±10%; Military: TA = -55°C to +125°C, VCC = 5.0V ±10%

Symbol	Parameter		Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level		Guaranteed Logic HIGH Level		2	—	—	V
V _{IL}	Input LOW Level		Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current ⁽⁴⁾	Standard Input ⁽⁵⁾	V _{CC} = Max.	V _I = V _{CC}	—	—	±1	μA
		Standard I/O ⁽⁵⁾			—	—	±1	
		Bus-hold Input			—	—	±100	
		Bus-hold I/O			—	—	±100	
I _{IL}	Input LOW Current ⁽⁴⁾	Standard Input ⁽⁵⁾	V _{CC} = Max.	V _I = GND	—	—	±1	μA
		Standard I/O ⁽⁵⁾			—	—	±1	
		Bus-hold Input			—	—	±100	
		Bus-hold I/O			—	—	±100	
I _{BHH} I _{BHL}	Bus-hold Sustain Current ⁽⁴⁾	Bus-hold Input	V _{CC} = Min.	V _I = 2V V _I = 0.8V	-50 50	— —	— —	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins) ^(5, 6)		V _{CC} = Max.	V _O = 2.7V V _O = 0.5V	— —	— —	±1 ±1	μA
V _{IK}	Clamp Diode Voltage		V _{CC} = Min., I _{IN} = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current		V _{CC} = Max., V _O = GND ⁽³⁾		-80	-140	-250	mA
V _H	Input Hysteresis			—	—	100	—	mV
I _{CC1} I _{CC2} I _{CCZ}	Quiescent Power Supply Current		V _{CC} = Max. V _{IN} = GND or V _{CC}		—	5	500	μA

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Pins with Bus-hold are identified in the pin description.
- The test limit for this parameter is ±5μA at TA = -55°C.
- Does not include Bus-hold I/O pins.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾		60	115	200	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾		-60	-115	-200	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -16mA MIL. I _{OH} = -24mA COM'L.	2.4	3.3	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 16mA MIL. I _{OL} = 24mA COM'L.	—	0.3	0.55	V

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NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- Duration of the condition can not exceed one second.
- The test limit for this parameter is ±5μA at TA = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$	—	0.5	1.5	mA	
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open \overline{xOEAB} or $\overline{xOEBA} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	75	120	$\mu\text{A}/\text{MHz}$	
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ ($xCLKAB$) 50% Duty Cycle $\overline{xOEAB} = \overline{xCEAB} = \text{GND}$ $\overline{xOEBA} = V_{CC}$ One Bit Toggling $f_i = 5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.8	1.7	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.3	3.2	
		$V_{CC} = \text{Max.}$, Outputs Open $f_{CP} = 10\text{MHz}$ ($xCLKAB$) 50% Duty Cycle $\overline{xOEAB} = \overline{xCEAB} = \text{GND}$ $\overline{xOEBA} = V_{CC}$ Sixteen Bits Toggling $f_i = 2.5\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	6.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	8.3	20 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - COMMERCIAL

Symbol	Parameter	Condition ⁽¹⁾	FCT162H952AT		FCT162H952BT		FCT162H952CT		FCT162H952ET		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	CL = 50pF RL = 500Ω	2	10	2	7.5	2	6.3	1.5	3.7	ns
t _{PZH} t _{PZL}	Output Enable Time xOEBA, xOEAB to xAx, xBx		1.5	10.5	1.5	8	1.5	7	1.5	4.4	ns
t _{PHZ} t _{PLZ}	Output Disable Time xOEBA, xOEAB to xAx, xBx		1.5	10	1.5	7.5	1.5	6.5	1.5	3.6	ns
tsu	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	2.5	—	1.5	—	ns
tH	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2	—	1.5	—	1.5	—	0	—	ns
tsu	Set-up Time, HIGH or LOW xCEAB, xCEBA to xCLKAB, xCLKBA		3	—	3	—	3	—	2	—	ns
tH	Hold Time HIGH or LOW xCEAB, xCEBA to xCLKAB, xCLKBA		2	—	2	—	2	—	0	—	ns
tw	Pulse Width HIGH or LOW xCLKAB or xCLKBA ⁽⁴⁾		3	—	3	—	3	—	3	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - MILITARY

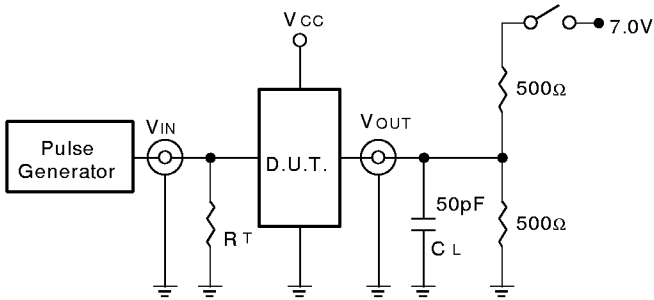
Symbol	Parameter	Condition ⁽¹⁾	FCT162H952AT		FCT162H952BT		FCT162H952CT		FCT162H952ET		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	CL = 50pF RL = 500Ω	2	11	2	8	2	7.3	—	—	ns
t _{PZH} t _{PZL}	Output Enable Time xOEBA, xOEAB to xAx, xBx		1.5	13	1.5	8.5	1.5	8	—	—	ns
t _{PHZ} t _{PLZ}	Output Disable Time xOEBA, xOEAB to xAx, xBx		1.5	10	1.5	8	1.5	7.5	—	—	ns
tsu	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	2.5	—	—	—	ns
tH	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2	—	1.5	—	1.5	—	—	—	ns
tsu	Set-up Time, HIGH or LOW xCEAB, xCEBA to xCLKAB, xCLKBA		3	—	3	—	3	—	—	—	ns
tH	Hold Time HIGH or LOW xCEAB, xCEBA to xCLKAB, xCLKBA		2	—	2	—	2	—	—	—	ns
tw	Pulse Width HIGH or LOW xCLKAB or xCLKBA ⁽⁴⁾		3	—	3	—	3	—	—	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	—	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. Guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

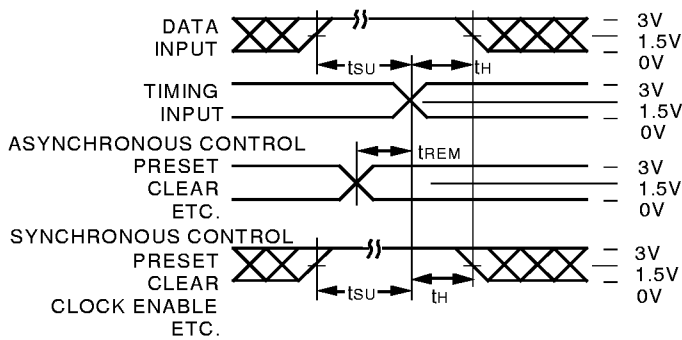
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DEFINITIONS:

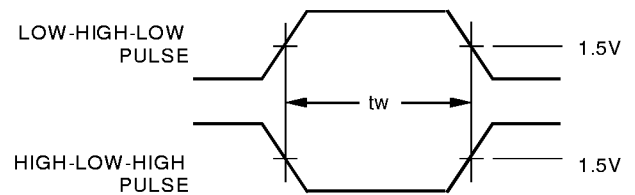
CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

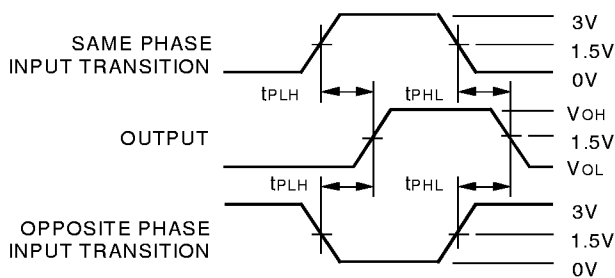
SET-UP, HOLD, AND RELEASE TIMES



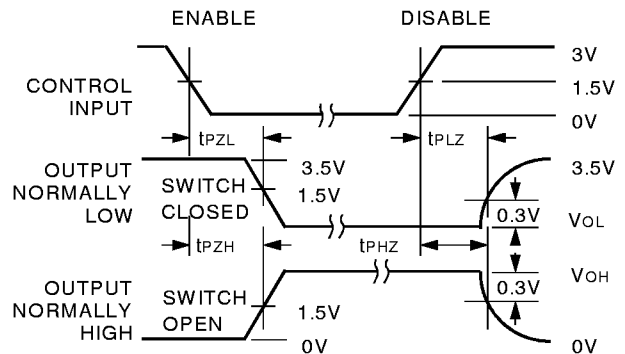
PULSE WIDTH



PROPAGATION DELAY



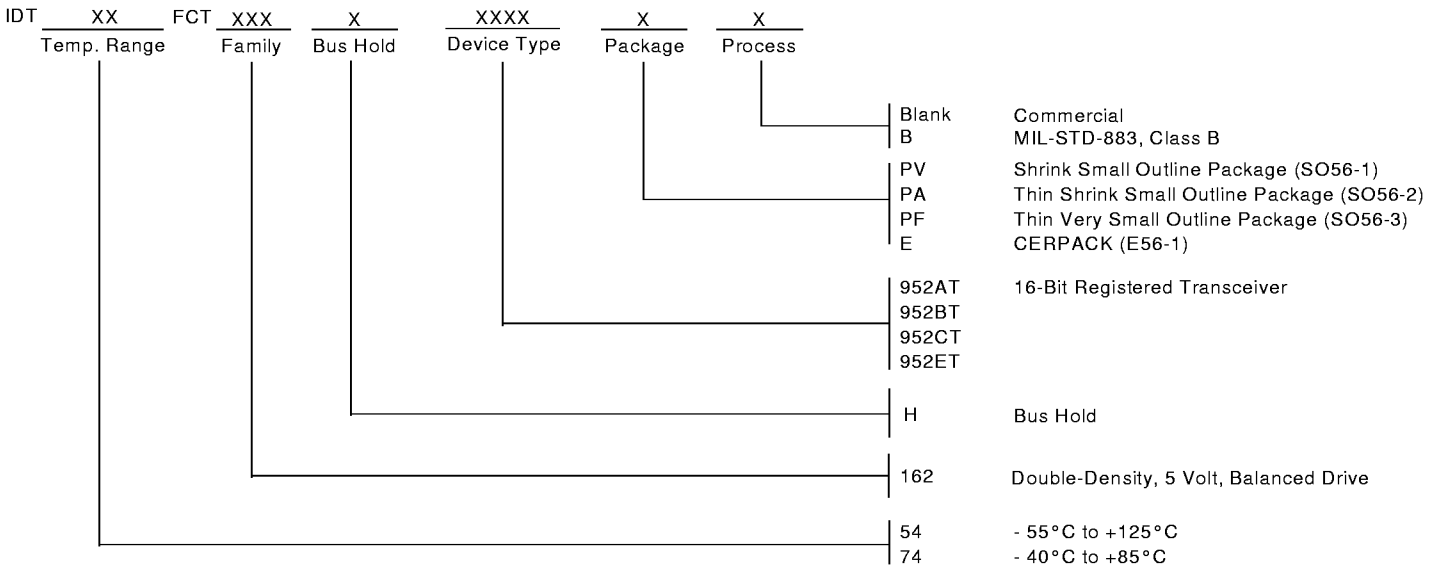
ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$.

ORDERING INFORMATION



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