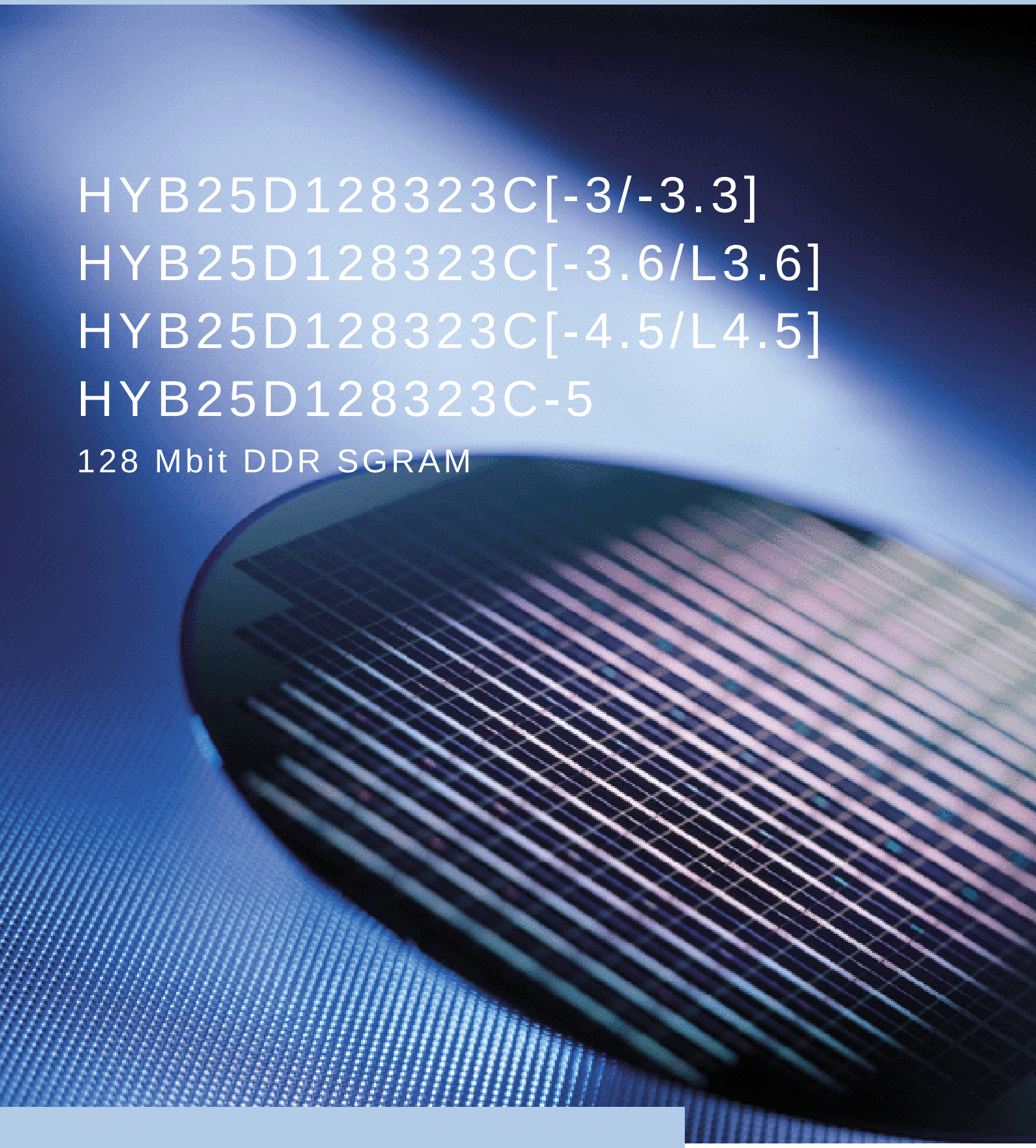
HYB25D128323C[-3/-3.3]
HYB25D128323C[-3.6/L3.6]
HYB25D128323C[-4.5/L4.5]
HYB25D128323C-5

128 Mbit DDR SGRAM



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Edition 2003-07

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HYB25D128323C-5

128 Mbit DDR SGRAM

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Revision History:	**V1.7**	**2003-07**
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Page	Subjects (major changes since last revision)	
all	new data sheet template	
43	**AC Operation Conditions**: Input Slew Rate added	
46	**Timing Parameters for speed sorts –3, –3.3, –3.6, –4.5, and –5**: Write DQS High/Low added	
48	**Timing Parameters for speed sorts L3.6 and L4.5**: Write DQS High/Low added	
Previous Version:	V1.51	2002-07
9, **13**, **42**, **46**, **48**	extended V_{DD} range for –3.6 and L3.6	

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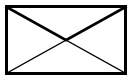

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1 Overview

1.1 Features

- Maximum clock frequency up to 333 MHz
- Maximum data rate up to 666 Mbps/pin
- Data transfer on both edges of clock
- Programmable CAS latency of 2, 3 and 4 clocks
- Programmable burst length of 2, 4 and 8
- Integrated DLL to align DQS and DQ transitions with CLK
- Data transfer signals are synchronized with byte wise bidirectional Data Strobe
- Data Strobe signal edge-aligned with data for Read operations
- Data Strobe signal center aligned with data for Write operations
- Differential clock inputs (CLK and $\overline{\text{CLK}}$)
- Data mask for masking write data, one DM per byte
- Organization 1024K × 32 × 4 banks
- 4096 rows and 256 columns per bank
- 4K Refresh (32ms)
- Refresh Interval 7.8 µsec
- Autorefresh and Self Refresh available
- Standard JEDEC TF-XBGA 128 package
- Self-mirrored, symmetrical ball out
- Matched Impedance Mode interface (Z_0=60Ω)
- SSTL-2 JEDEC Weak Mode interface (Z_0=34Ω)
- IO voltage V_{DDQ} = 2.5 V
- V_{DD} power supply memory core:
  - Speed sorts –3 and –3.3: 2.5 V < V_{DD} < 2.9 V
  - Speed sorts L4.5, –4.5, and –5: V_{DD} = 2.5 V
  - Speed sorts L3.6 and –3.6 support both V_{DD} modes

Table 1 Performance

Part Number Speed Code		–3	–3.3	–3.6	–4.5	–5.0	L3.6	L4.5	Unit
CAS Latency 4	$t_{CK4min.}$	3	3.3	3.6	4.5	5.0	3.6	4.5	ns
	$f_{CK4max.}$	333	300	278	222	200	278	222	MHz
CAS Latency 3	$t_{CK3min.}$	4.0	4.0	4.2	4.5	5.0	4.2	4.5	ns
	$f_{CK3max.}$	250	250	238	222	200	238	222	MHz
Data Out Window	t_{QH}	1.05	1.15	1.26	1.58	1.75	1.26	1.58	ns
DQS-DQ Skew	t_{DQSQ}	0.30	0.30	0.33	0.45	0.5	0.33	0.45	ns

1.2 Description

The Infineon 128Mbit DDR SGRAM is a ultra high performance graphics memory device, designed to meet all requirements for high bandwidth intensive applications like PC graphics systems.

The 128Mbit DDR SGRAM uses a double-data-rate DRAM architecture organized as 4 banks × 4096 rows × 256 columns × 32 bits. The double-data-rate architecture is essentially a 2n prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single Read or Write access to the DDR

SGRAM consists of a single 64-bit wide, one clock cycle data transfer at the internal DRAM core and two corresponding 32-bit wide, one-half clock cycle data transfers at the I/O pins. The result is a data rate of 666 Mbits / sec per pin. The external data interface is 32 bit wide and achieves at 333 MHz system clock a peak bandwidth of 2.66 Gigabytes/sec.

The device is supplied with 2.5 V resp. within the range of 2.5 V - 2.9 V for the memory core and 2.5 V for the output drivers. Two drivers strengths are available: 2.5 V Matched Impedance Mode and SSTL2 Weak Mode. The “Matched Impedance Mode” interface is optimized for high frequency digital data transfers and matches the impedance of graphics board systems (60Ohm).

Auto Refresh and Self Refresh operations are both supported.

A standard JEDEC TF-XBGA 128 package is used which enables ultra high speed clock and data transfer rates. The signals are mapped symmetrically to the balls in order to enable mirrored mounting in application.

The chip is fabricated in Infineon technologies advanced 256M process technology.

2 Pin Configuration

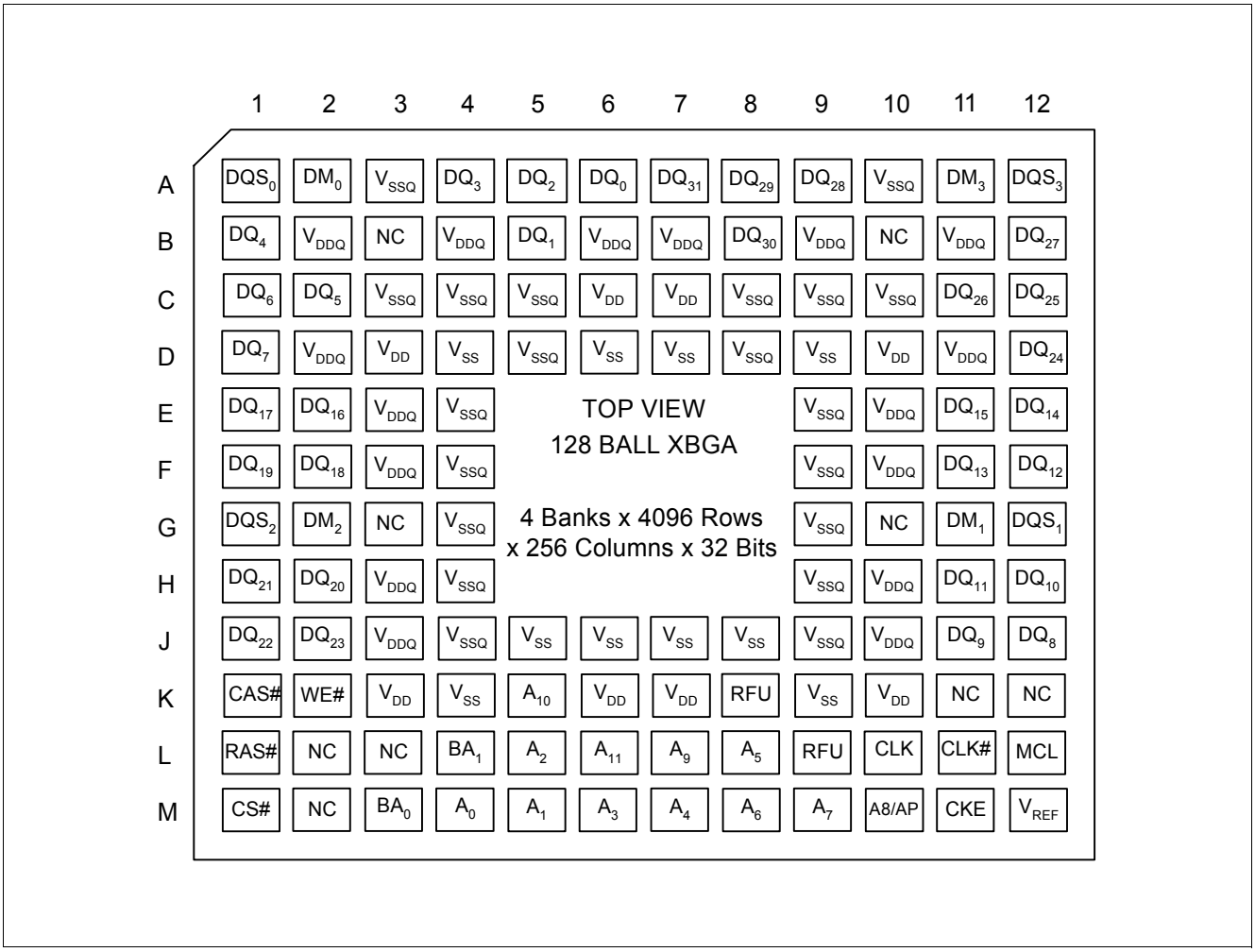

Figure 1 Ball Out 128Mbit DDR SGRAM

Note: The inner matrix of 4 × 4 balls will be used as thermal V_{SS} contacts ncluding the thermal V_{SS} contacts, the total amount of balls is 144

Table 2 Signal and Pin Description

Pin	IO Type	Detailed Function
CLK, $\overline{CLK}$	Input	**Clock**: CLK and CLK# are differential clock inputs. All address and command inputs are latched on the crossing of the positive edge of CLK and the negative edge of $\overline{CLK}$. Output data (DQ's and DQS) is referenced to the crossing of CLK and $\overline{CLK}$.
CKE	Input	**Clock Enable**: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row active in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF-REFRESH exit. CKE must be maintained HIGH trough out READ and WRITE accesses. Input buffers (excluding CLK, $\overline{CLK}$) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL2 input but will detect an LVCMOS LOW level after VDD is applied.
$\overline{CS}$	Input	**Chip Select**: CS# enables the command decoder when low and disables it when high. When the command decoder is disabled, new commands are ignored, but internal operations continue. CS# is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs**: $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ (along with $\overline{CS}$) define the command to be executed.
BA1, BA0	Input	**Bank Address Inputs**: BA0 and BA1 select to which internal bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. They also define which mode register (mode register or extended mode register) is loaded during a MODE REGISTER SET command.
A11.. A0	Input	**Address Inputs**: During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11). During a Read or Write command cycle, A0-A7 defines the column address (CA0-CA7). In addition to the column address, A8/AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A8 is high, the active bank is precharged. If A8 is low, the Autoprecharge function is disabled. During a Precharge command cycle, A8/AP is used to determine, which bank(s) will be precharged. If A8/AP is high, all four banks will be precharged regardless of the state of BA0 and BA1. If A8/AP is low, BA0 and BA1 define the bank to be precharged. The address inputs also provide the op-code during a MODE REGISTER SET command.
DQS3.. DQS0	I/O	**Data Strobes**: The DQSx are the bidirectional strobe signals. At read cycles, the DQSx signals are generated by the SGRAM and are edge-aligned to the data. At write cycles, the DQS signals are generated by the controller. The rising or falling edge indicates the center of the data valid window. Before and after a transfer cycle, DQSx enters a preamble and a postamble state. The DQSx signals are mapped to the following data bytes: DQS0 to DQ0.. DQ7, DQS1 to DQ8.. DQ15, DQS2 to DQ16..DQ23, DQS3 to DQ24.. DQ31.
DQ31.. DQ0	I/O	**Data Input/Output**: The DQx signals form the 32 bit wide data bus. At READ cycles the pins are outputs and during WRITE cycles inputs. The data is transferred at both edges of the DQSx signals.

Table 2 Signal and Pin Description (cont'd)

Pin	IO Type	Detailed Function
DM3.. DM0	Input	**Input Data Mask**: The DM signals are input mask signal for WRITE data. They mask off a complete byte on the data bus. DMx = 1 prevents the corresponding byte from being written. DM3 corresponds to DQ31..DQ24, DM2 to DQ23..DQ16, DM1 to DQ15..DQ8, DM0 to DQ7..DQ0. DM signals are sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
V_{REF}	Input	**Voltage Reference**: V_{REF} is the reference voltage input signal.
V_{DD}, V_{SS}	Supply	**Power Supply**: Power and Ground for the internal logic. V_{DD} = 2.5 V ±5% for L4.5, –4.5, and -5 2.5 V – 5% < V_{DD} < 2.9 V for –3.6 and L3.6 2.5 V < V_{DD} < 2.9 V for –3 and –3.3
V_{DDQ}, V_{SSQ}	Supply	**IO Power Supply**: Isolated Power and Ground for the output buffers to provide improved noise immunity. V_{DDQ} = 2.5V ± 5%
NC, RFU	–	Please do not connect No Connect, Reserved for Future Use pins.
MCL	–	Must be connected to low

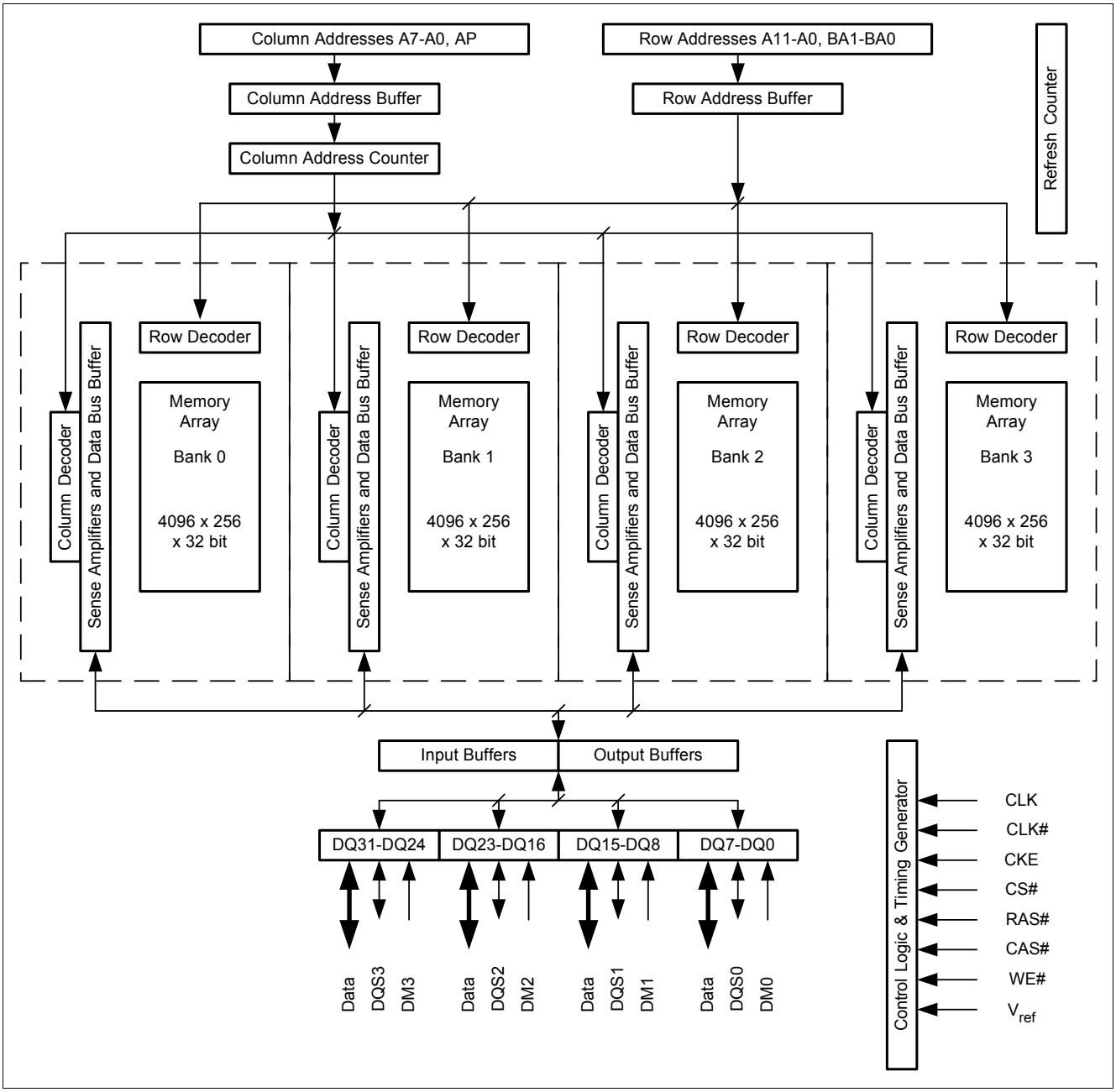

Figure 2 Functional blocks

3 Register Set

3.1 Mode Register

The mode register stores the data for controlling the various operating modes of the DDR SGRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL ON and various vendor specific options. The default value of the mode register is not defined. Therefore the mode register must be written after power up to operate the DDR SGRAM. The DDR SGRAM should be activated with CKE already high prior to writing into the Mode Register. The Mode Register is written by using the MRS command. The state of the address signals registered in the same cycle as MRS command is written in the mode register. The value can be changed as long as all banks are in the idle state.

The mode register is divided into various fields depending on functionality. The burst length uses A2.. A0, CAS latency (read latency from column address) uses A6.. A4. A7 is used for test mode, A8 is used for DLL Reset. A7, A8 and BA1 must be set to low for normal DDR SGRAM operation. A9.. A11 is reserved for future use. BA0 selects Extended Mode Register Setup operation when set to 1. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.

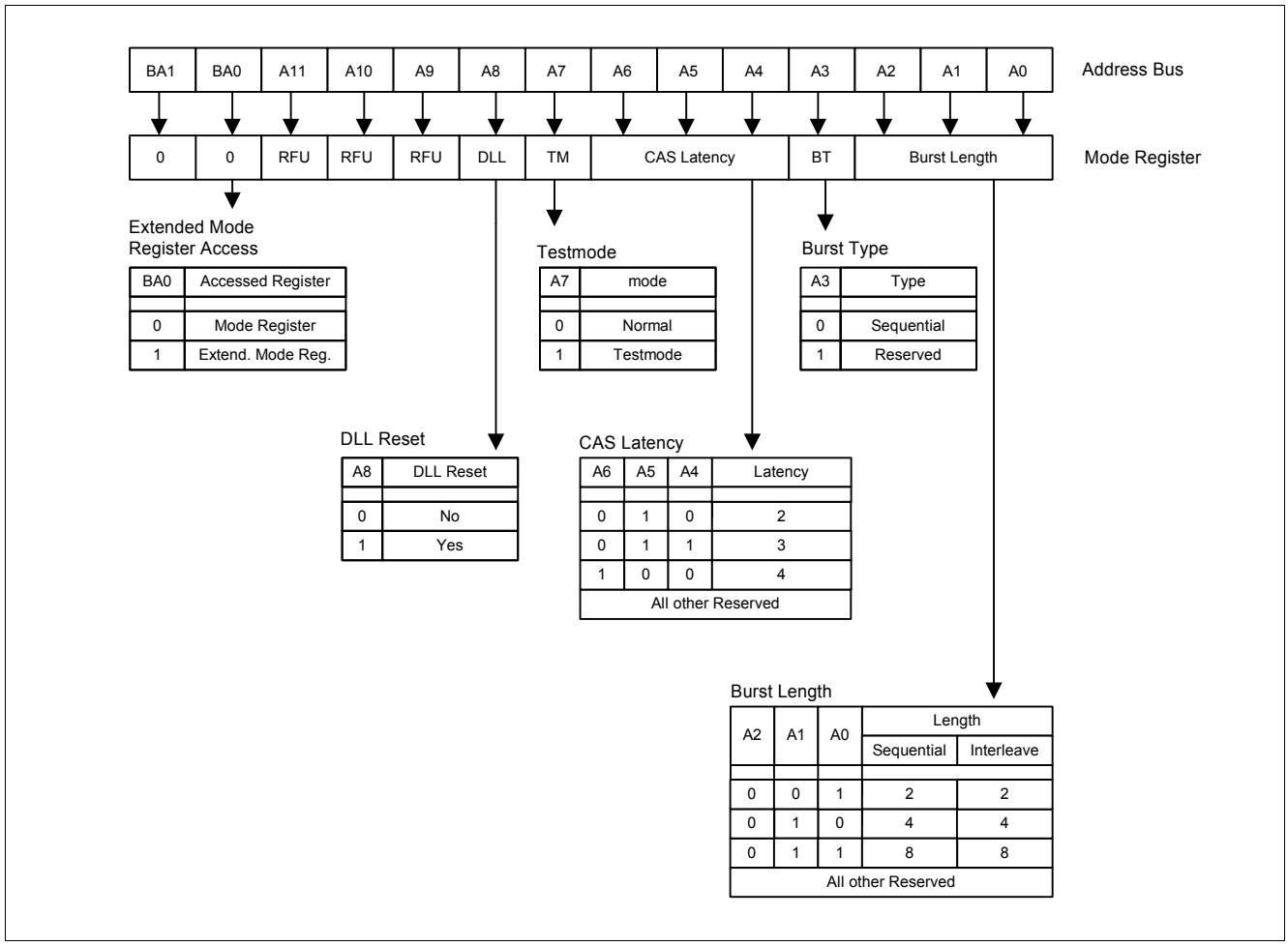

Figure 3 Mode Register Bitmap

3.2 Extended Mode Register Setup (EMRS)

The Extended Mode Register is responsible for enabling / disabling the DLL in the HYB25D128323C and for selecting the interface type for the IOs and input pins. The Extended Mode Register can be programmed by performing a normal Mode Register Setup operation and setting the BA0 bit to high. All other bits of the EMRS register are reserved and should be set to low.

The Bit A0 enables / disables the DLL.

The Bits A1 and A6 set the driver strength of the IOs. For detailed explanation, refer to the following table.

Table 3 IO Driver Strength and Interface Settings

A6	A1	Drive Strength	Strength/ Impedance	IO Power Supply VDDQ	Comment
0	0	SSTL-2 weak	60% / 34Ohm	2.5V	replacement for strong mode
0	1	SSTL-2 weak	60% / 34Ohm	2.5V	–
1	0	RFU	RFU	RFU	Do not use
1	1	matched impedance mode	30% / 60Ohm	2.5V	output driver matches line impedance

Note: The combination A6=0 and A1=0 defines SSTL-2 strong mode in 32M DDR SGRAM which is not supported in this device.

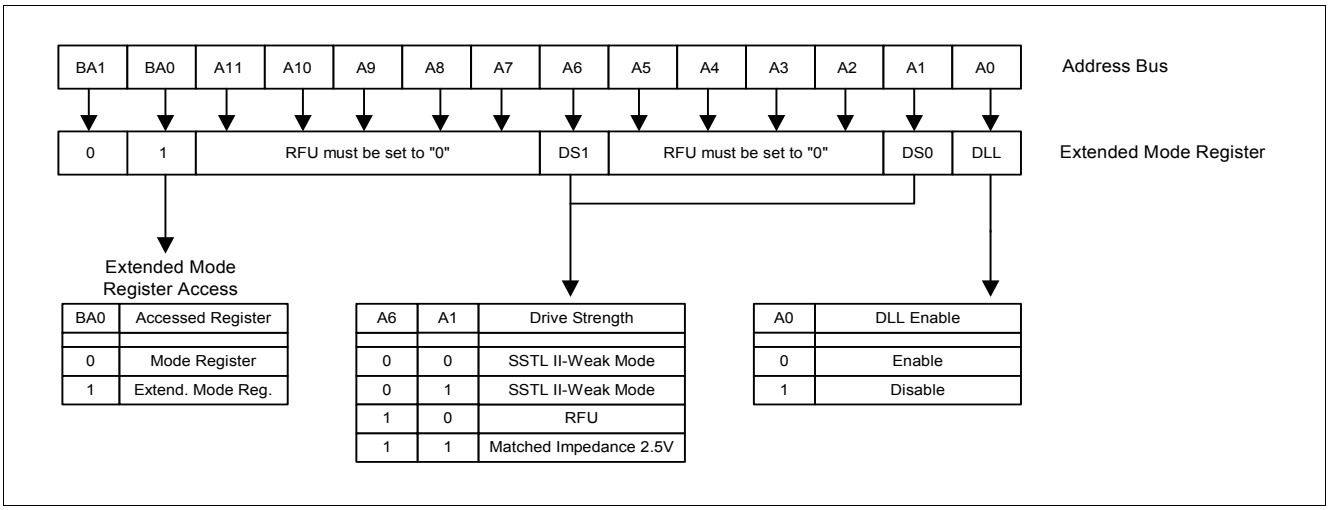

Figure 4 Extended Mode Register Bitmap

3.3 Signal and Timing Description

3.3.1 General Description

The 128Mbit DDR SGRAM is a 16MByte Synchronous Graphics DRAM. It consists of four banks. Each bank is organized as 4096 rows × 256 columns × 32 bits.

Read and Write accesses are burst oriented. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address bits registered coincident with the Activate command are used to select the bank and the row to be accessed. BA1 and BA0 select the bank, address bits A11.. A0 select the row. Address bits A7.. A0 registered coincident with the Read or Write command are used to select the starting column location for the burst access.

The regular Single Data Rate SGRAM read and write cycles only use the rising edge of the external clock input. For the DDR SGRAM, the special signals DQSx (Data Strobe) are used to mark the data valid window. During

read bursts, the data valid window coincides with the high or low level of the DQSx signals. During write bursts, the DQSx signal marks the center of the valid data window. Data is available at every rising and falling edge of DQSx, therefore the data transfer rate is doubled.

For Read accesses, the DQSx signals are aligned to the clock signal CLK.

3.4 Special Signal Description

3.4.1 Clock Signal

The DDR SGRAM operates with a differential clock (CLK and CLK#) input. CLK is used to latch the address and command signals. Data input and DMx signals are latched with DQSx. The DDR SGRAM implements a Delay Locked Loop circuit (DLL) which tracks both edges of the CLK input signal and aligns the DQS output edges with the CLK input edges.

The minimum and maximum clock cycle time is defined by t_{CK}. The maximum value for t_{CK} is defined to provide a lower bound for the operation frequency of the internal DLL circuit. The minimum and maximum clock duty cycle are specified using the minimum clock high time t_{CH} and the minimum clock low time t_{CL} respectively.

The internal DLL circuit requires additional 200 clock cycles after DLL reset for internal clock stabilization.

3.4.2 Command Inputs and Addresses

Like single data rate SGRAMs, each combination of RAS#, CAS# and WE# input in conjunction with CS# input at a rising edge of the clock determines a DDR SGRAM command.

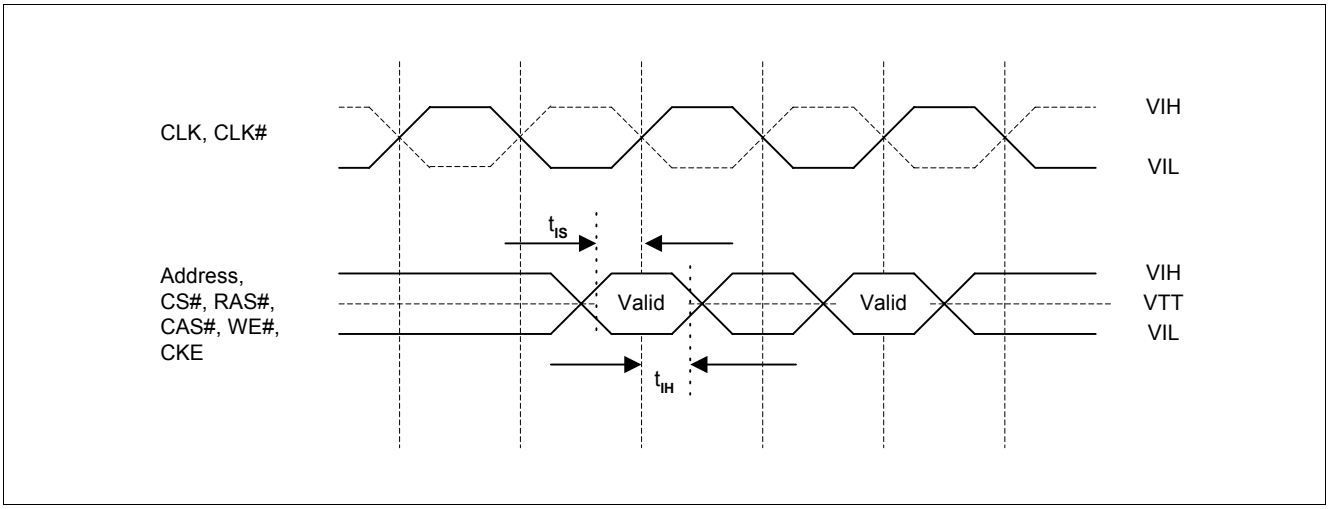

Figure 5 Command and Address Signal Timing

3.4.3 Data Strobe and Data Mask

3.4.3.1 Operation at Burst Reads

The Data Strobes provide a 3-state output signal to the receiver circuits of the controller during a read burst. The data strobe signal goes t_{RPRE} clock cycle low before data is driven by the DDR SGRAM and then toggles low to high and high to low till the end of the burst. The CAS latency is specified to the first low to high transition. The edges of the Output Data signals and the edges of the data strobe signals during a read are nominally coincident with edges of the input clock. The tolerance of these edges is specified by the parameters t_{AC} and t_{DQSCK} and is referenced to the crossing point of the CLK and CLK# signal. The t_{DQSQ} timing parameter describes the skew between the data strobe edge and the output data edge.

The following table summarizes the mapping of DQSx and DMx signals to the data bus.

Table 4 Mapping of DQSx and DMx

data strobe signal	data mask signal	Controlled data bus
DQS0	DM0	DQ7 .. DQ0
DQS1	DM1	DQ8 .. DQ15
DQS2	DM2	DQ16 .. DQ23
DQS3	DM3	DQ24 .. DQ31

The minimum time during which the output data is valid is critical for the receiving device. This also applies to the Data Strobe DQS during a read since it is tightly coupled to the output data. The parameters t_{QH} and t_{DQSQ} define the minimum output data valid window.

Prior to a burst of read data, given that the device is not currently in burst read mode, the data strobe signals transit from Hi-Z to a valid logic low. This is referred to as the data strobe “read preamble” t_{RPRE}.

Once the burst of read data is concluded, given that no subsequent burst read operation is initiated, the data strobe signals transit from a valid logic low to Hi-Z. This is referred to as the data strobe “read postamble” t_{RPST}.

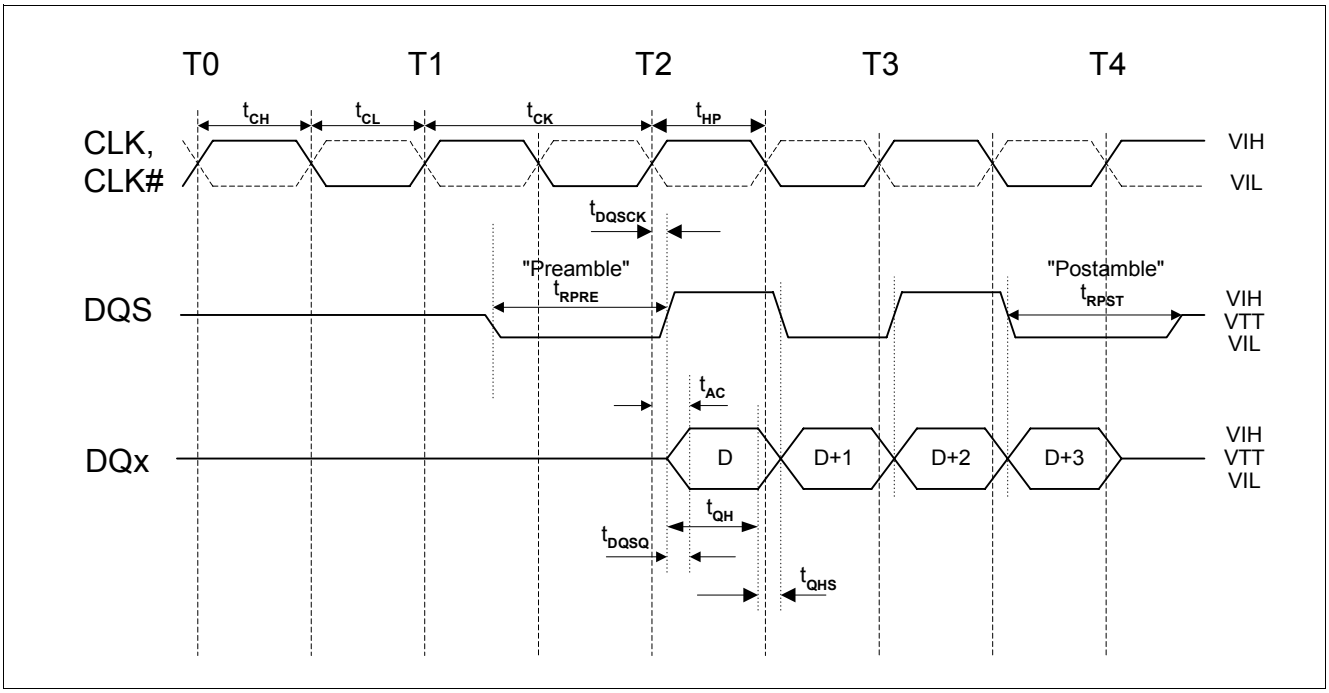

Figure 6 DQS Timing for Read

3.4.3.2 Operation at Burst Write

During a write burst, control of the data strobe is driven by the memory controller. The DQSx signals are nominally centered with respect to data and data mask. The tolerance of the data and data mask edges versus the data strobe edges during writes are specified by the setup and hold time parameters of data (t_{QDQSS} & t_{QDQSH}) and data mask (t_{DMDQSS} & t_{DMDQSH}). The input data is masked in the same cycle when the corresponding DMx signal is high (i.e. the DMx mask to write latency is zero.)

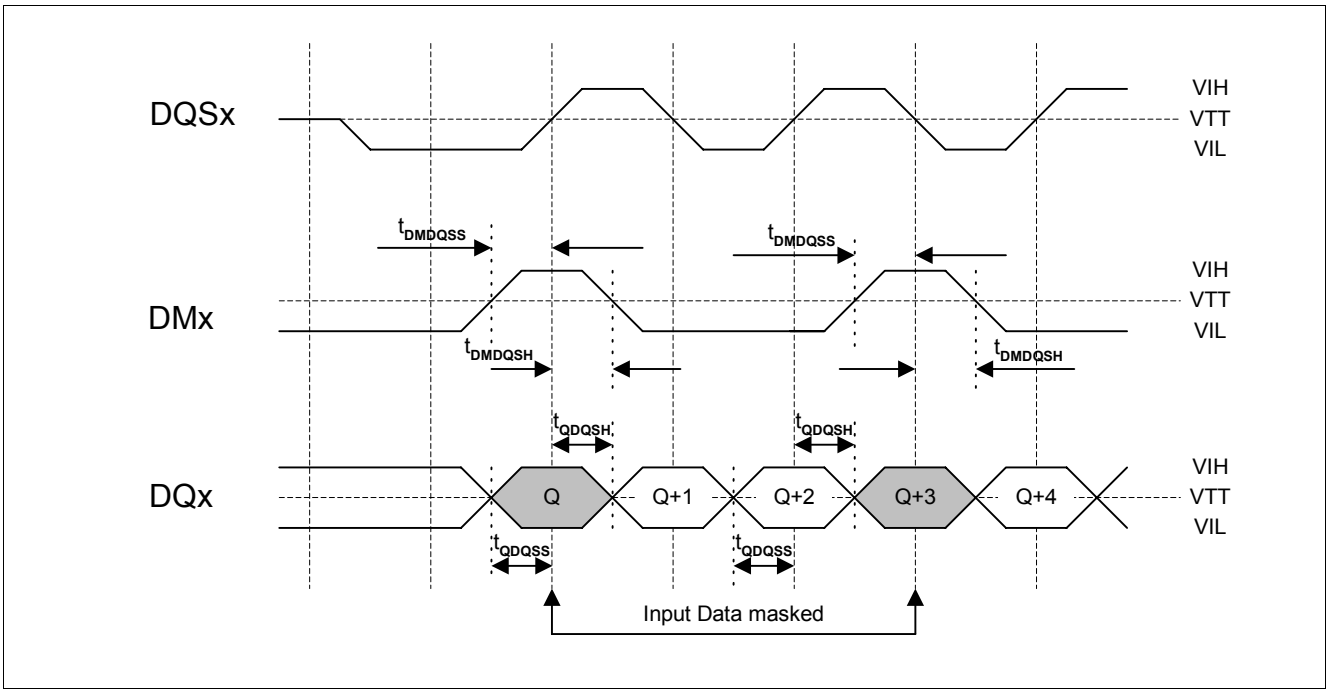

Figure 7 DQS and DM Timing at Write

Prior to a burst of write data, given that the controller is not currently in burst write mode, the data strobe signal (DQSx) transits from Hi-Z to a valid logic low. This is referred to as the data strobe “Write Preamble”. Once the burst of write data is concluded, given that no subsequent burst write operation is initiated, the data strobe signal (DQSx) transits from a valid logic low to Hi-Z. This is referred to as the data strobe “Write Postamble”, t_{WPST}. For DDR SGRAM, data is written with a delay which is defined by the parameter t_{DQSS} (DDR write latency). This is different than the single data rate SGRAM where data is written in the same cycle as the Write command is issued.

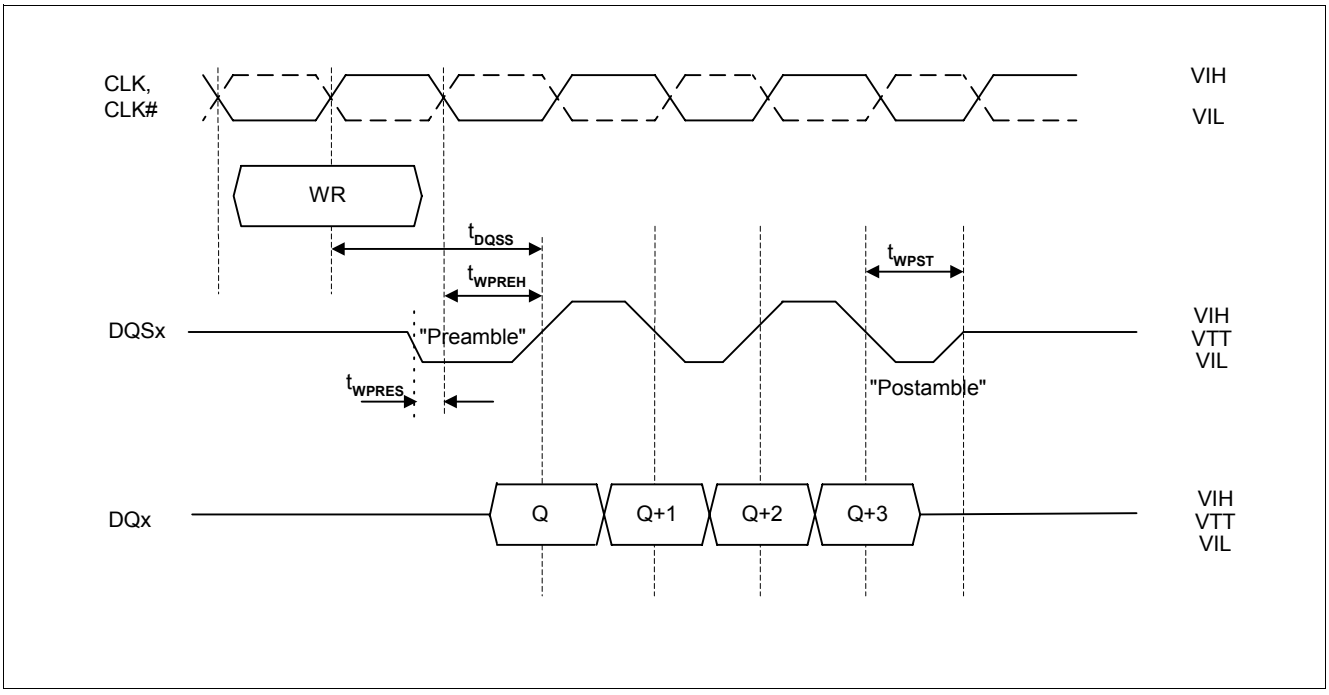

Figure 8 DQS Pre/Postamble at Write

3.5 Description of Timings

3.5.1 Power-Up Sequence

The following sequence is highly recommended for Power-Up:

1. Apply power and start clock. Maintain CKE=L and the other pins are in NOP conditions at the input
2. Apply V_{DD} before or at the same time as V_{DDQ}, apply V_{DDQ} before or at the same time as V_{REF} & V_{TT}
3. Start clock, maintain stable conditions for 200 µs min.
4. Apply NOP and set CKE to high
5. Apply a Precharge All command
6. Issue EMRS (extended mode register set) command to enable the DLL
7. Issue a Mode Register Set command for “DLL reset“. 200 cycles of clock input are required to lock the DLL.
8. Issue Precharge commands for all banks of the device.
9. Issue two or more Auto-Refresh commands.
10. Issue a Mode Register Set command. (This step may also be taken as step 6)

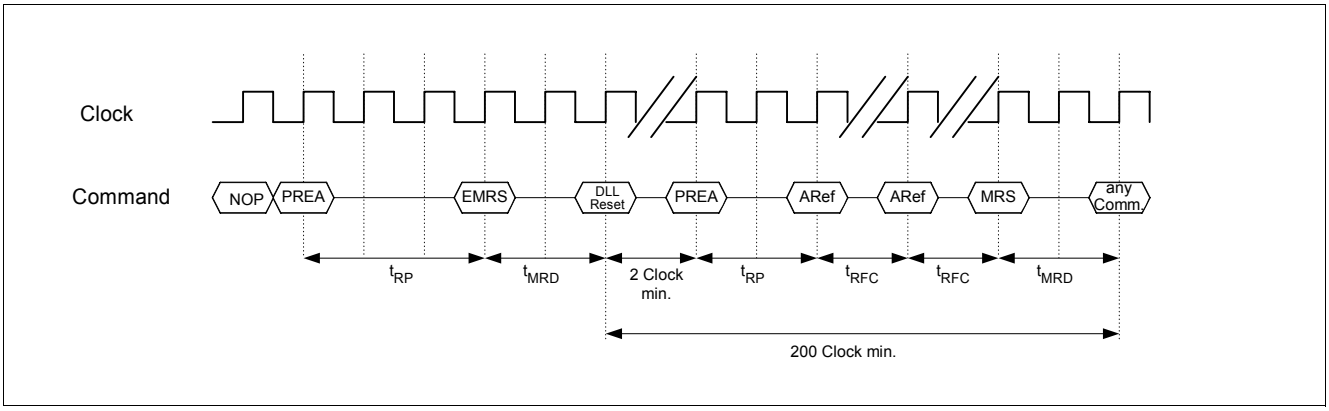

Figure 9 Power-Up Sequence

3.5.2 Mode Register Set Timing

The DDR SGRAM should be activated with CKE already high prior to writing into the mode register. Two clock cycles are required to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state.

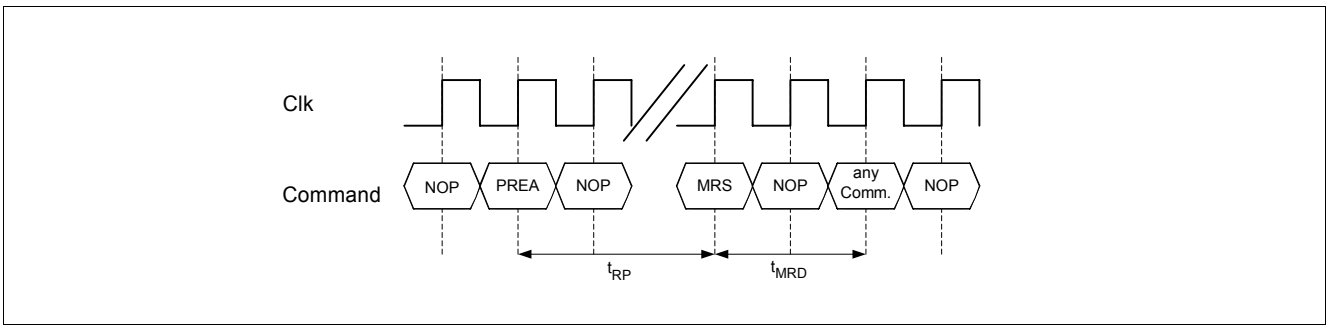

Figure 10 Mode Register Set Timing

3.5.3 Extended Mode Register Set Timing

The timing of the Extended Mode Register Setup operation is equivalent to the Mode Register Setup timing.

3.5.4 Bank Activation Command (ACT)

The Bank Activation command is initiated by issuing an ACT command at the rising edge of the clock. The DDR SGRAM has four independent banks which are selected by the two Bank select Addresses (BA0, BA1). The Bank Activation command must be applied before any Read or Write operation can be executed. The delay from the Bank Activation command to the first read or write command must meet or exceed the minimum of RAS to CAS delay time (t_{RCDDC} min. for read commands and t_{RCDWR} min. for write commands). Once a bank has been activated, it must be precharged before another Bank Activate command can be applied to the same bank. The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank activation delay time (t_{RRD} min).

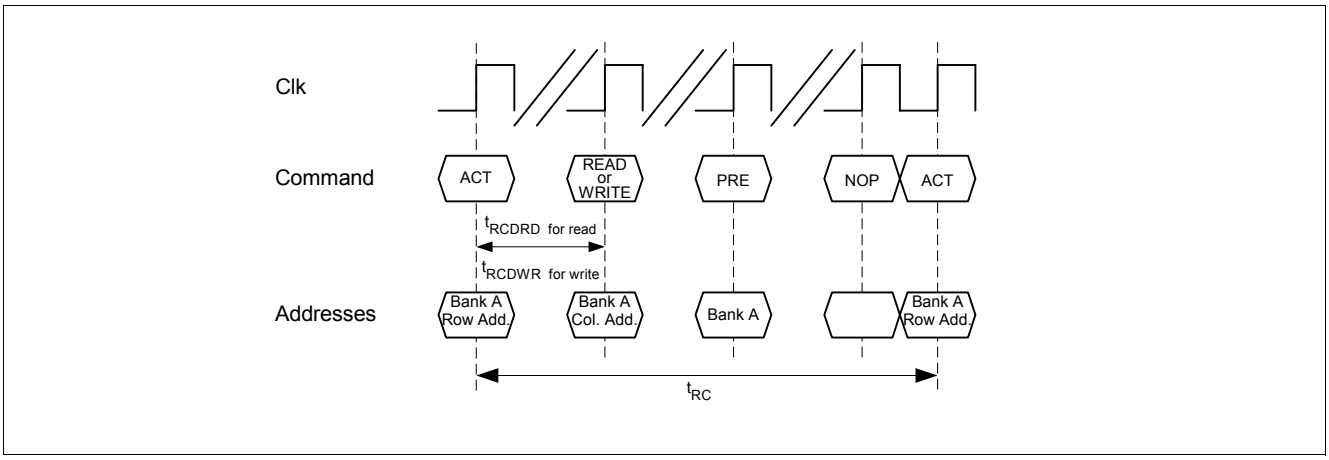

Figure 11 Activate to Read or Write Command Timing (one bank)

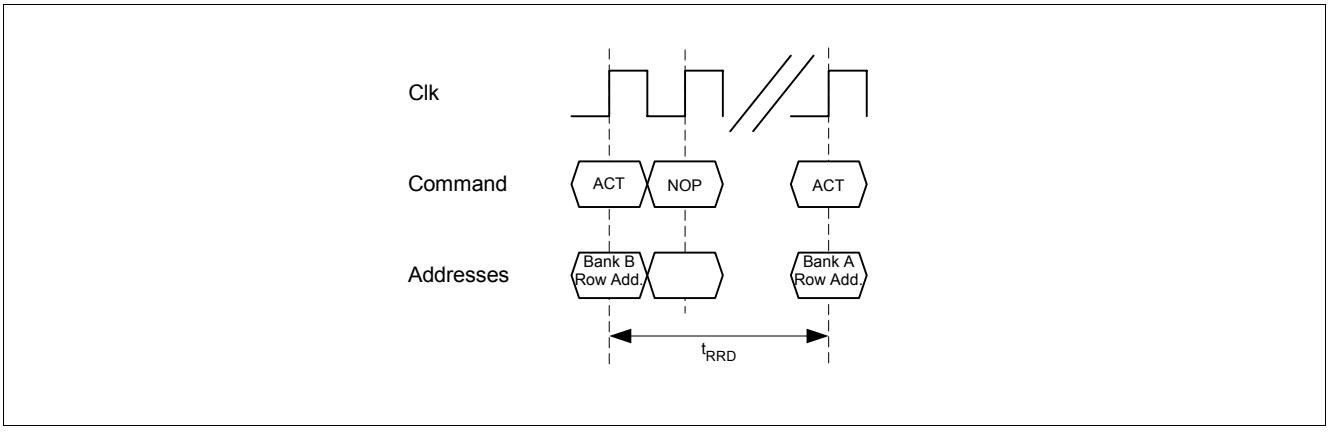

Figure 12 Activate Bank A to Activate Bank B Timing

3.5.5 Precharge Command

This command is used to precharge or close a bank that has been activated. Precharge is initiated by issuing a Precharge command at the rising edge of the clock. The Precharge command can be used to precharge each bank respectively or all banks simultaneously. The Bank addresses BA0 and BA1 select the bank to be precharged. After a Precharge command, the analog delay t_{RP} has to be met until a new Activate command can be initiated to the same bank.

Table 5 Precharge Control

A8/AP	BA1	BA0	Precharged
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

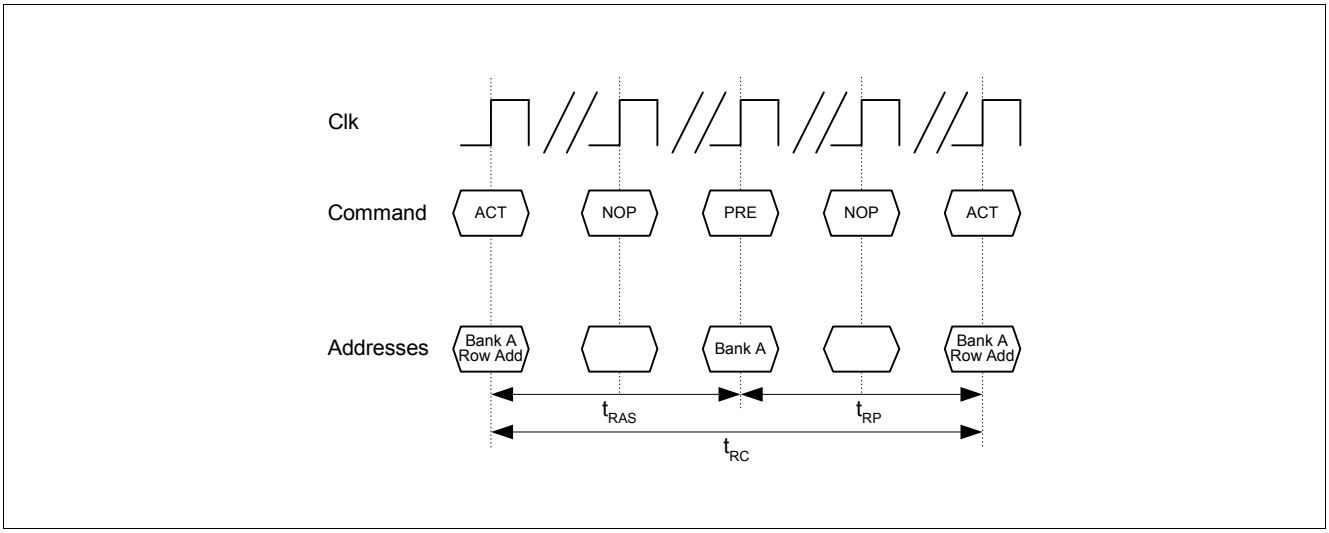

Figure 13 Precharge Command Timing

3.5.6 Self Refresh

The self refresh mode can be used to retain the data in the DDR SGRAM if the chip is powered down. To set the DDR SGRAM into a self refreshing mode, a Self Refresh command must be issued and CKE held low at the rising edge of the clock. Once the self Refresh command is initiated, CKE must stay low to keep the device in Self Refresh mode. During the Self refresh mode, all of the external control signals are disabled except CKE. The clock is internally disabled during Self Refresh operation to reduce power. An internal timing generator guarantees the self refreshing of the memory content. To exit the Self Refresh mode, a stable external clock is needed for the DLL before returning CKE high. After the Power Down Exit time(t_{PDEX}), a Deselect or NOP command is issued and CKE is held high for longer than t_{SREX} in order to lock the DLL.

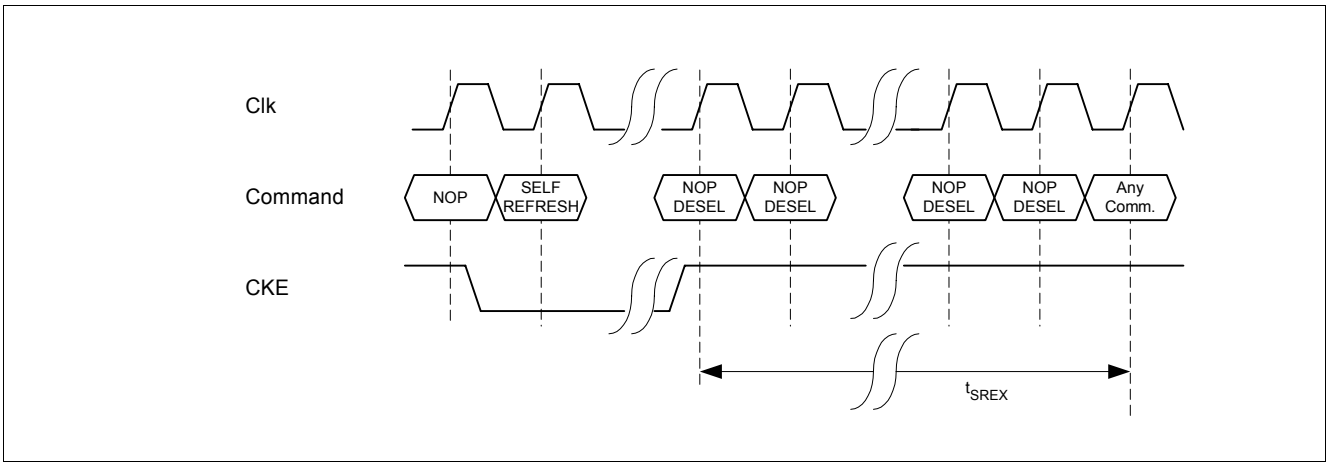

Figure 14 Self Refresh timing

3.5.7 Auto Refresh

The auto refresh function is initiated by issuing an Auto Refresh command at the rising edge of the clock. All banks must be precharged and idle before the Auto Refresh command is applied. No control of the external address pins is required once this cycle has started. All necessary addresses are generated in the device itself. When the refresh cycle has completed, all banks will be in the idle state. A delay between the Auto Refresh command and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the t_{RFC}(min).

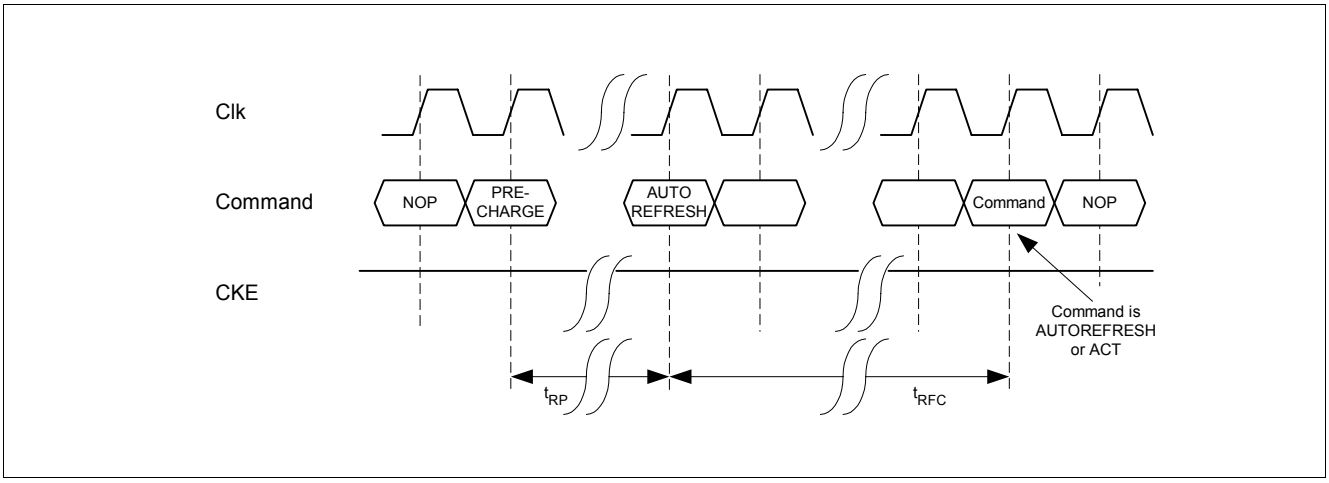

Figure 15 Autorefresh timing

3.5.8 Power Down Mode

The Power Down Mode is entered when CKE is set low and exited when CKE is set high. The CKE signal is sampled at the rising edge of the clock. Once the Power Down Mode is initiated, all of the receiver circuits except CLK, CKE and DLL circuits are gated off to reduce power consumption. All banks can be set to idle state or stay activate during Power Down Mode, but burst activity may not be performed. After exiting from Power Down Mode, at least one clock cycle of command delay must be inserted before starting a new command. During Power Down Mode, refresh operations cannot be performed; therefore, the device cannot remain in Power Down Mode longer than the refresh period (t_{REF}) of the device.

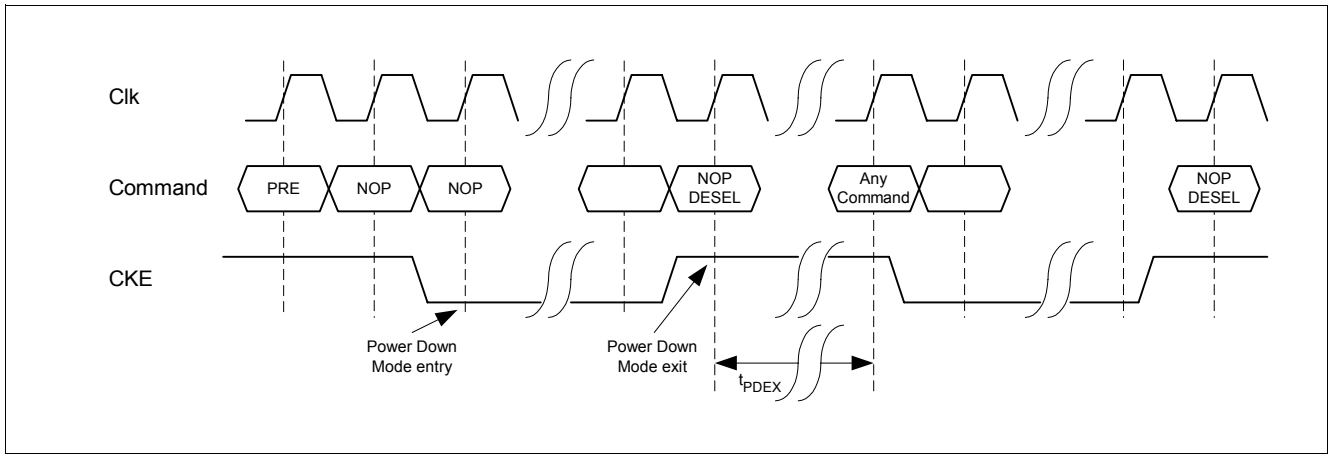

Figure 16 Power Down Mode timing

3.5.9 Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to the memory (write cycle) or from the memory (read cycle). The burst length is programmable and set by address bits A0 - A3 during the Mode Register Setup command. The burst length controls the number of words that will be output after a read command or the number of words to be input after a write command. One word is 32 bits wide. The sequential burst length can be set to 2, 4 or 8 data words.

Table 6 Burst Mode and Sequence

Burst Length	Starting Column Address			Order of Access within a Burst
	A2	A1	A0	Type = Sequential
2			0	0 - 1
			1	1 - 0
4		0	0	0 - 1 - 2 - 3
		0	1	1 - 2 - 3 - 0
		1	0	2 - 3 - 0 - 1
		1	1	3 - 0 - 1 - 2
8	0	0	0	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
	0	0	1	1 - 2 - 3 - 4 - 5 - 6 - 7 - 0
	0	1	0	2 - 3 - 4 - 5 - 6 - 7 - 0 - 1
	0	1	1	3 - 4 - 5 - 6 - 7 - 0 - 1 - 2
	1	0	0	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3
	1	0	1	5 - 6 - 7 - 0 - 1 - 2 - 3 - 4
	1	1	0	6 - 7 - 0 - 1 - 2 - 3 - 4 - 5
	1	1	1	7 - 0 - 1 - 2 - 3 - 4 - 5 - 6

3.5.10 Burst Read Operation: (READ)

The Burst Read operation is initiated by issuing a READ command at the rising edge of the clock after t_{RCD} from the bank activation. The address inputs (A7.. A0) determine the starting address for the burst. The burst length (2, 4 or 8) must be defined in the Mode Register. The first data after the READ command is available depending on the CAS latency. The subsequent data is clocked out on the rising and falling edge of DQSx until the burst is completed. The DQSx signal is generated by the DDR SGRAM during Burst Read Operations.

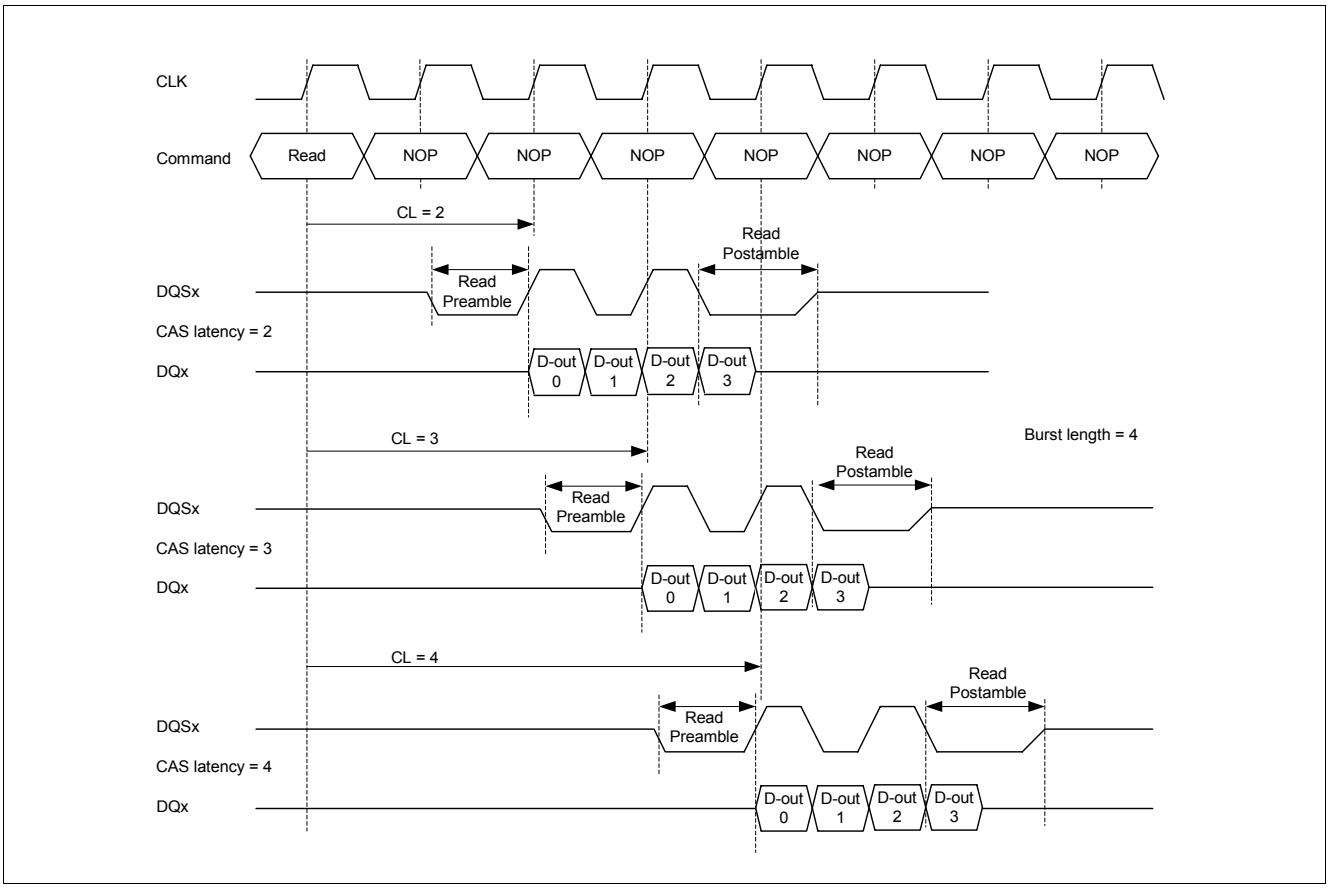

Figure 17 Burst Read Operation

3.5.11 Burst Write Operation (WRITE)

The Burst Write is initiated by issuing a WRITE command at the rising edge of the clock. The address inputs (A7.. A0) determine the starting column address. Data for the first burst write cycle must be applied on the DQ pins on the first rising edge of DQSx following the WRITE command. The time between the WRITE command and the first corresponding edge of the data strobe is t_{DQSS}. The remaining data inputs must be supplied on each subsequent rising and falling edge of the data strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

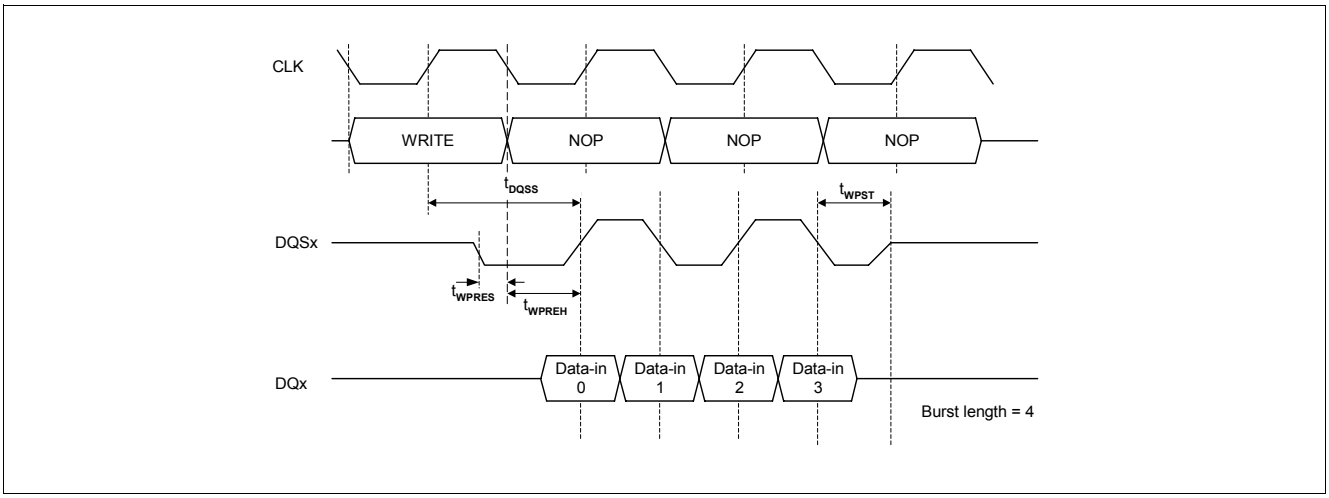

Figure 18 Burst Write Operation

3.5.12 Burst Stop Command (BST)

A Burst Stop is initiated by issuing a BURST STOP command at the rising edge of the clock. The Burst Stop Command has the fewest restrictions, making it the easiest method to terminate a burst operation before it has been completed. When the Burst Stop Command is issued during a burst read cycle, read data and DQSx go to a high impedance state after a delay which is equal to the CAS Latency set in the Mode Register. The Burst Stop latency is equal to the CAS latency CL.The Burst Stop command is not supported during a write burst operation. Burst Stop is also illegal during Read with Auto-Precharge.

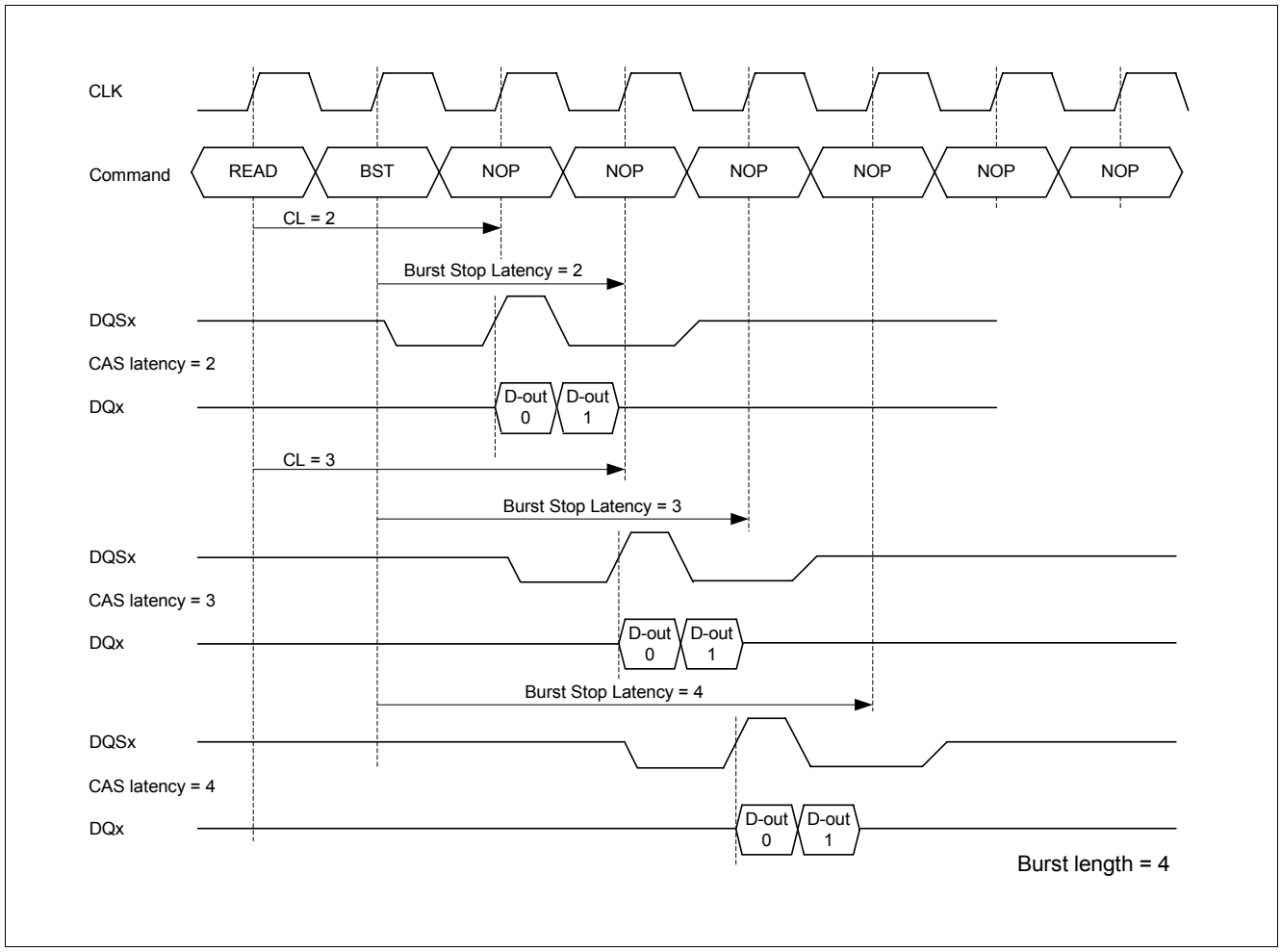

Figure 19 Burst Stop for Read

3.5.13 Data Mask (DMx) Function

The DDR SGRAM has a Data Mask function that can be used only during write cycles. When the Data Mask is activated (DMx high) during burst write, the write operation is masked immediately. The DMx to data-mask latency is zero. DMx can be issued at the rising or falling edge of Data Strobe.

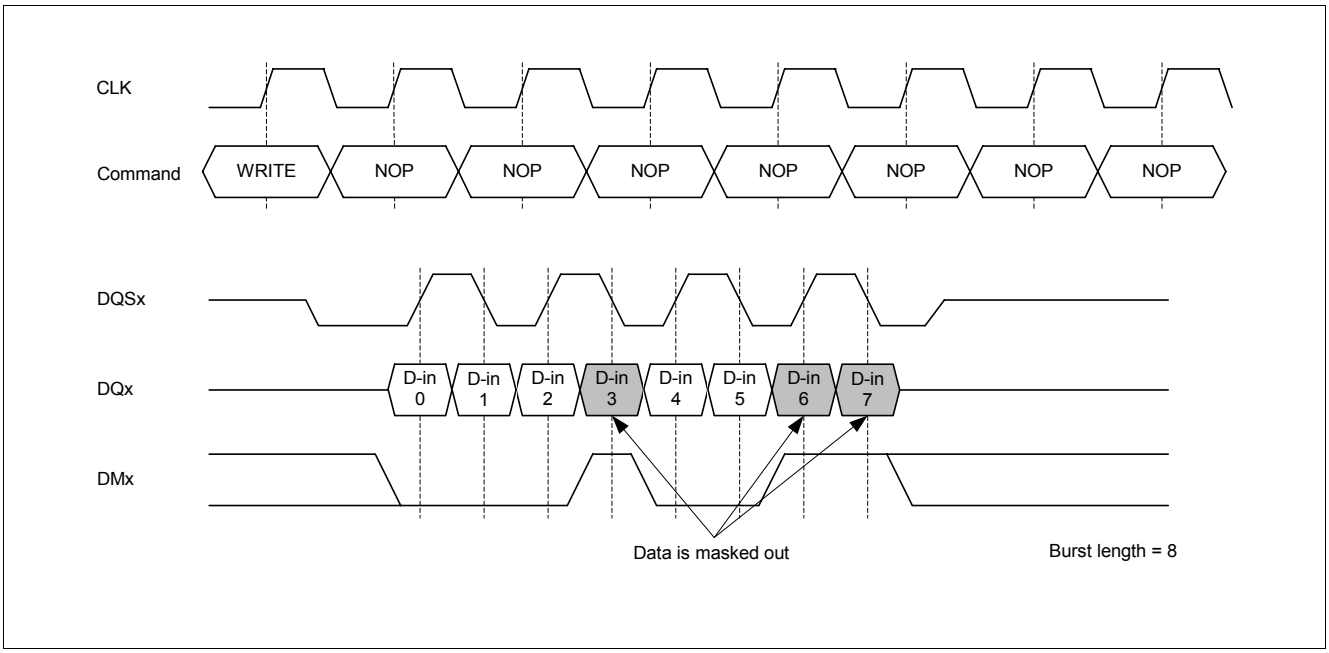

Figure 20 Data Mask Timing

3.5.14 Autoprecharge Operation

The Autoprecharge command is issued by setting column address A8 high when a Read or a Write command is asserted to the DDR SGRAM. If A8 is low when Read or Write command is issued, a normal Read or Write burst operation is executed and the bank remains active at the end of the burst sequence. When the Auto Precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during the Read or Write cycle after $t_{RAS(min.)}$ is satisfied.

3.5.15 Read with Autoprecharge (READA)

If a Read with Auto-precharge command is initiated, the DDR SGRAM automatically enters the precharge operation BL/2 clock cycles after the READA command and $t_{RAS(min.)}$ is satisfied. If $t_{RAS(min.)}$ has not been satisfied yet, an internal interlock will delay the precharge operation until it is satisfied. Once the precharge operation has started, the bank cannot be reactivated and the new command can not be asserted until the Precharge time (t_{RP}) has been satisfied.

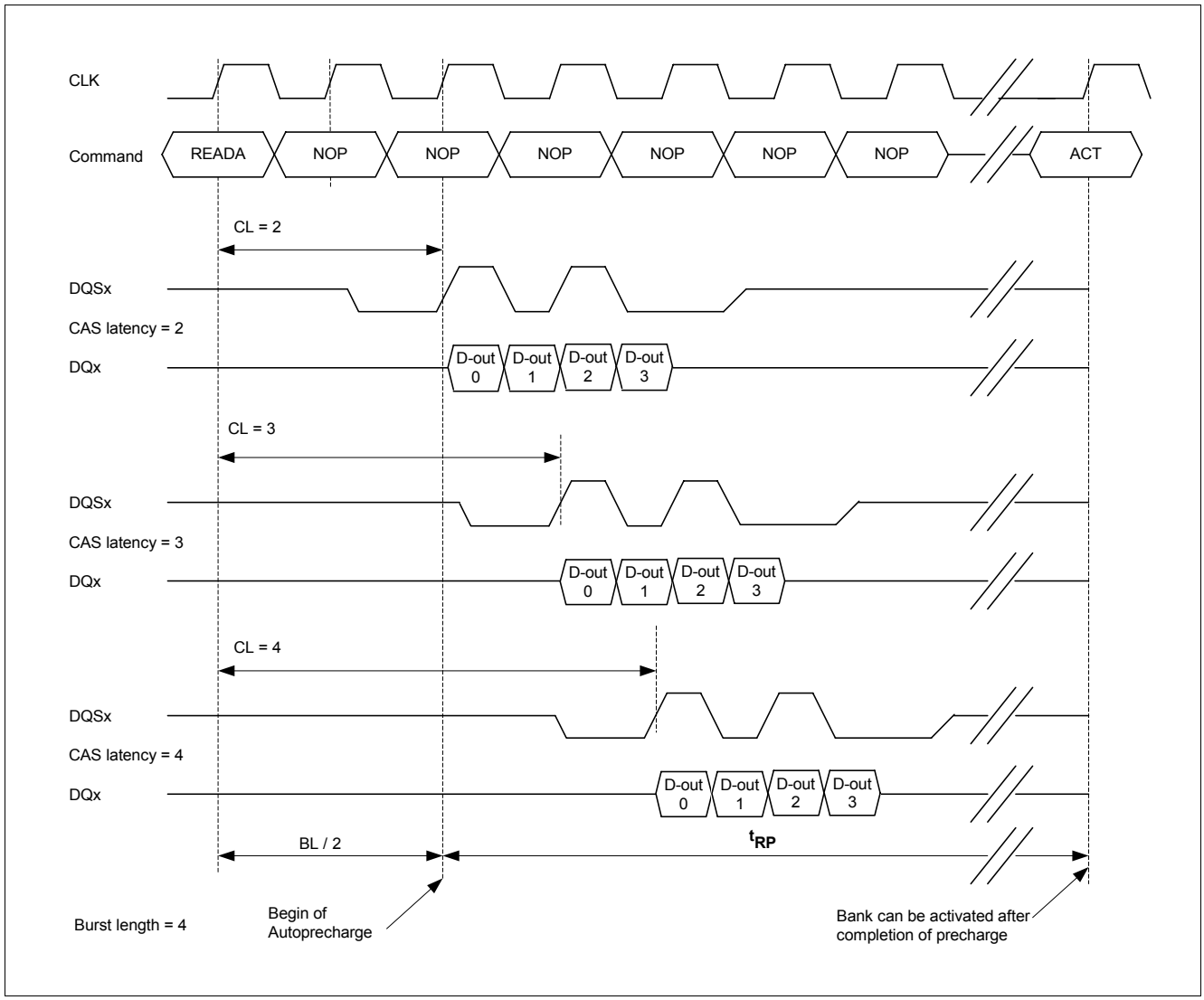

Figure 21 Read Burst with Autoprecharge

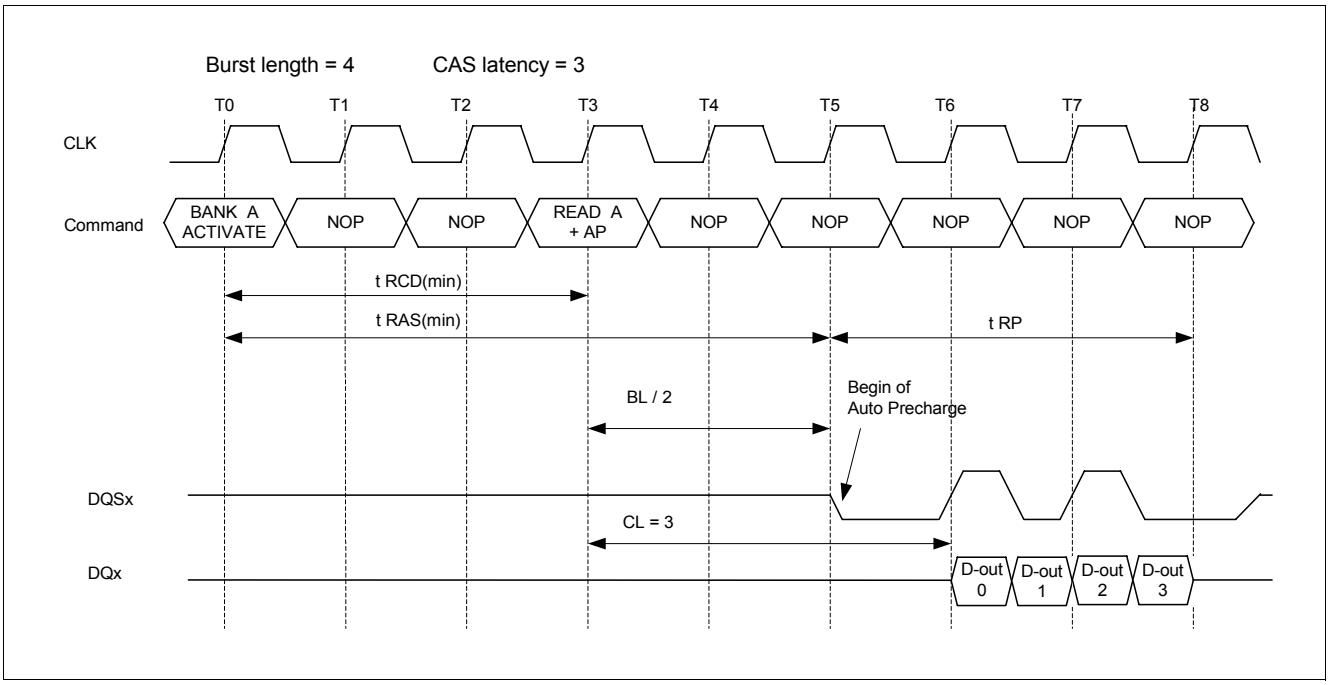

Figure 22 Read Concurrent Auto Precharge

Table 7 Concurrent Read Auto Precharge Support

Asserted Command	For same Bank			For different Bank		
	T4	T5	T6	T4	T5	T6
READ	NO	NO	NO	NO	YES	YES
READ+AP	YES	YES	NO	NO	YES	YES
ACTIVATE	NO	NO	NO	YES	YES	YES
PRECHARGE	YES	YES	NO	YES	YES	YES

Note: This table is for the case of Burst Length = 4, CAS Latency =3 and t_{WR}=2 clocks

When READ with Auto Precharge is asserted, new commands can be asserted at T4,T5 and T6 as shown in **Table 7**.

An Interrupt of a running READ burst with Auto Precharge i.e. at T4 and T5 to the same bank with another READ+AP command is allowed, it will extend the begin of the internal Precharge operation to the last READ+AP command.

Interrupts of a running READ burst with Auto Precharge i.e. at T4 are not allowed when doing concurrent command to another active bank. ACTIVATE or PRECHARGE commands to another bank are always possible while a READ with Auto Precharge operation is in progress.

3.5.16 Write with Autoprecharge (WRITEA)

If A8 is high when a Write command is issued, the Write with Auto-Precharge function is performed. The internal precharge begins after the write recovery time t_{WR} and $t_{RAS(min.)}$ are satisfied.

If a Write with Auto Precharge command is initiated, the DDR SGRAM automatically enters the precharge operation at the first rising edge of CLK after the last valid edge of DQS (completion of the burst) plus the write recovery time t_{WR}. Once the precharge operation has started, the bank cannot be reactivated and the new command can not be asserted until the Precharge time (t_{RP}) has been satisfied. If $t_{RAS(min.)}$ has not been satisfied yet, an internal interlock will delay the precharge operation until it is satisfied.

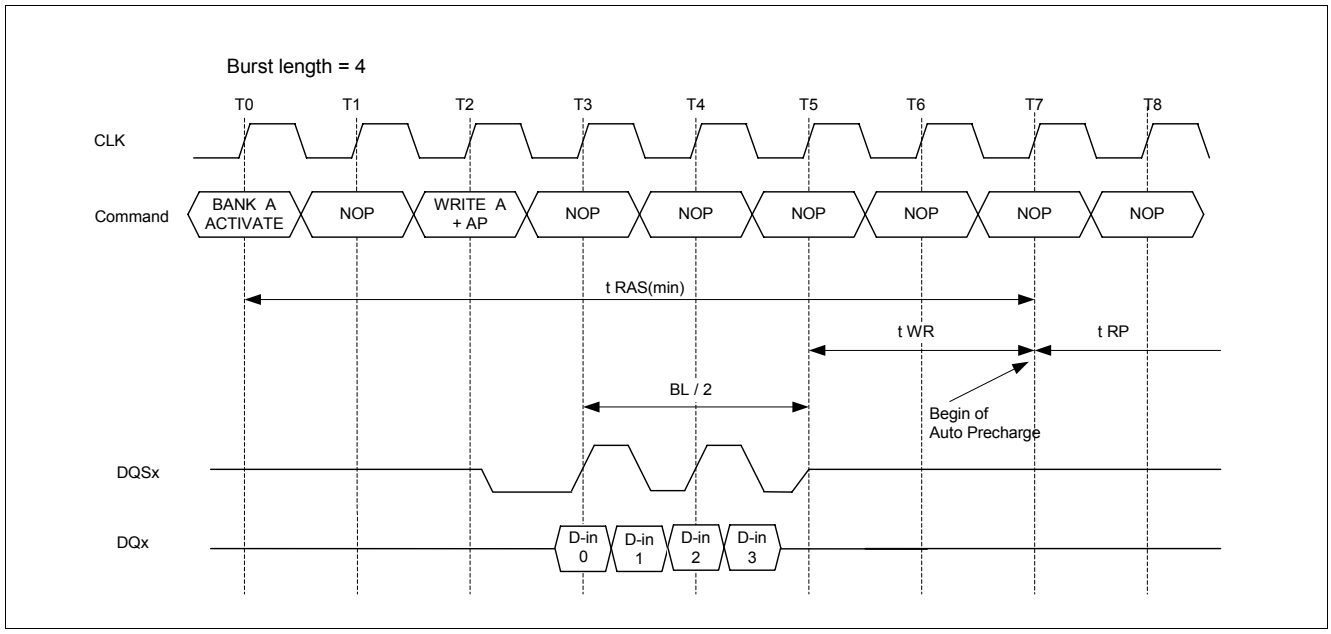

Figure 23 Write Burst with Auto Precharge

Note: t_{WR} starts at the first rising edge of clock after the last valid edge of the 4 DQSx.

Table 8 Concurrent Write Auto Precharge Support

Asserted Command	For same Bank						For different Bank				
	T3	T4	T5	T6	T7	T8	T3	T4	T5	T6	T7
WRITE	NO	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES
WRITE+AP	YES	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES
READ	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	YES
READ+AP	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	YES
ACTIVATE	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES	YES
PRECHARGE	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES	YES

When Write with Auto Precharge is asserted, new commands can be asserted at T3.. T8 as shown in **Table 8**.

An Interrupt of a running WRITE burst with Auto Precharge i.e. at T3 to the same bank with another WRITE+AP command is allowed as long as the burst is running, it will extend the begin of the internal Precharge operation to the last WRITE+AP command.

Interrupts of a running WRITE burst with Auto Precharge i.e. at T3 are not allowed when doing concurrent WRITE's to another active bank. Consecutive WRITE or WRITE+AP bursts (T4.. T7) to other open banks are possible. ACTIVATE or PRECHARGE commands to another bank are always possible while a WRITE with Auto Precharge operation is in progress.

3.6 Burst Interruption

3.6.1 Read Interrupted by a Read

A Burst Read can be interrupted before completion of the burst by a new Read command given to any bank. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read command continues to appear on the outputs until the CAS latency from the

interrupting Read command is satisfied. At this point, the data from the interrupting Read command appears. Read to Read interval (CAS#(a) to CAS#(b) Command period, t_{CCD}) is minimum 1 CLK.

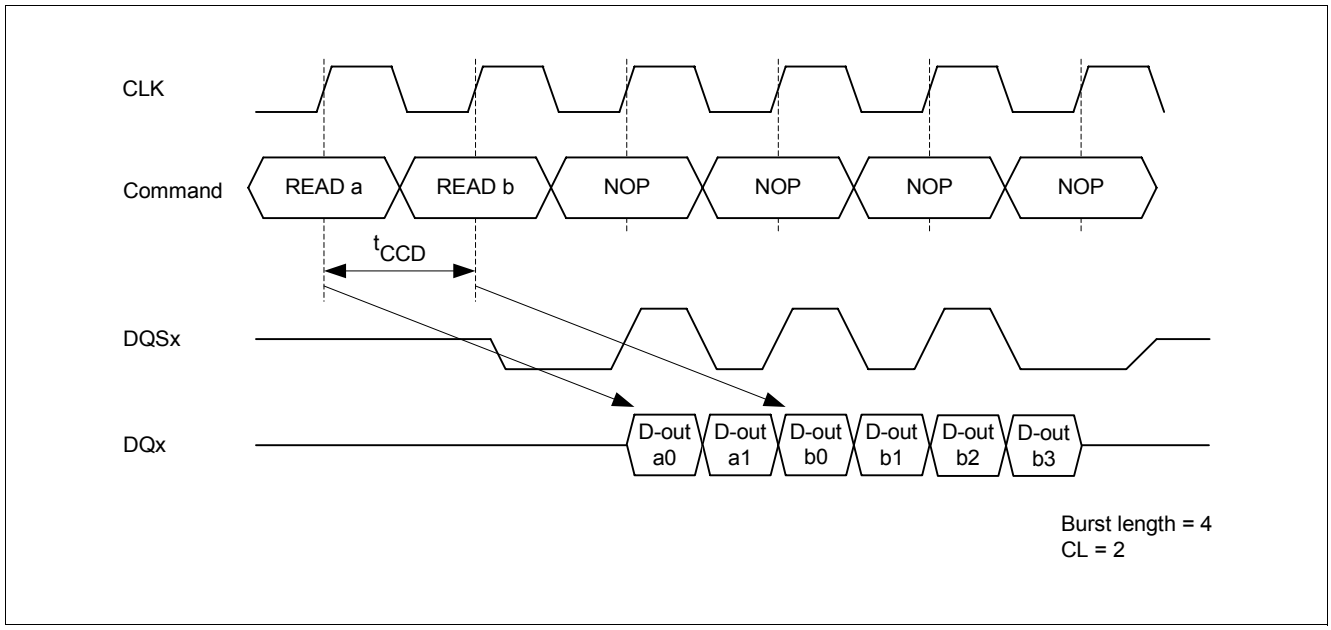

Figure 24 Read interrupted by Read

3.6.2 Read Interrupted by a Write

To interrupt a burst read with a write command, a Burst Stop command must be asserted to avoid data contention on the I/O bus by placing the DQ's (Output drivers) in a high impedance state at least one clock cycle before the Write Command is initiated (Last Output to Write Command Latency). To insure that the DQs are tri-stated one cycle before the write operation begins, the Burst Stop command must be applied at least 3 clock cycles for CL = 2, at least 4 clock cycles for CL = 3 or at least 5 clock cycles for CL = 4 before the Write command.

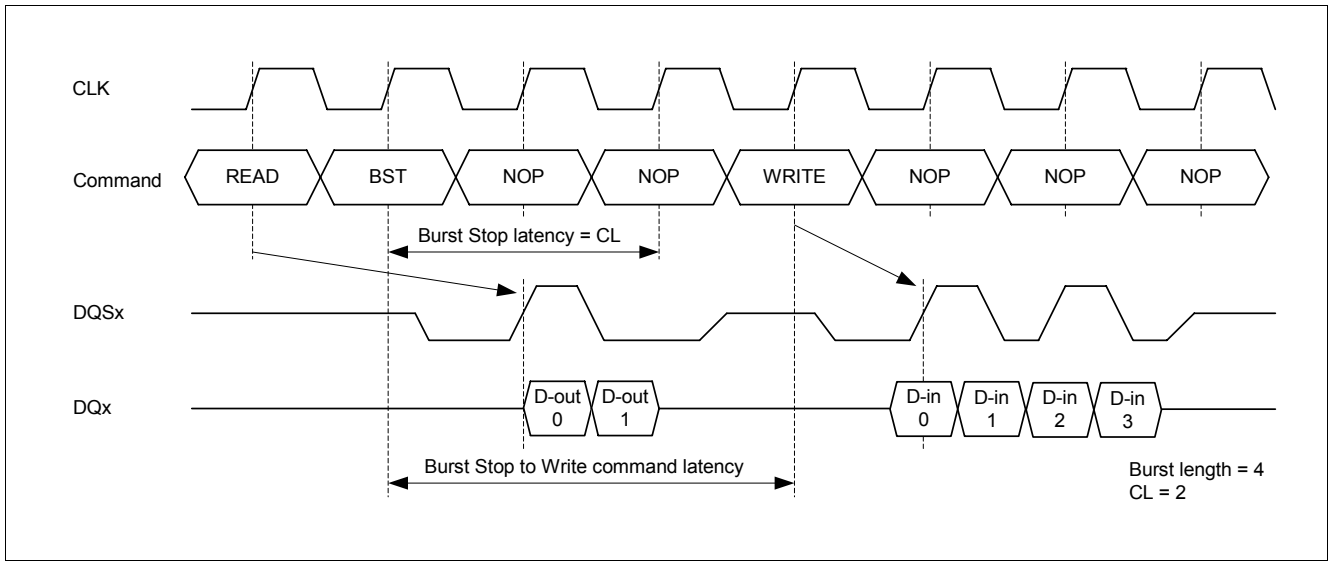

Figure 25 Read interrupted by Write

3.6.3 Read Interrupted by a Precharge

A Burst Read operation can be interrupted by a Precharge of the same bank. The Read command to Precharge time is minimum 1 clock cycle. The Precharge command disables the data output depending on the CAS latency. Once the last data bit has been outputted, the output buffers are tristated. A new Bank Activate command may be issued to the same bank after t_{RP}.

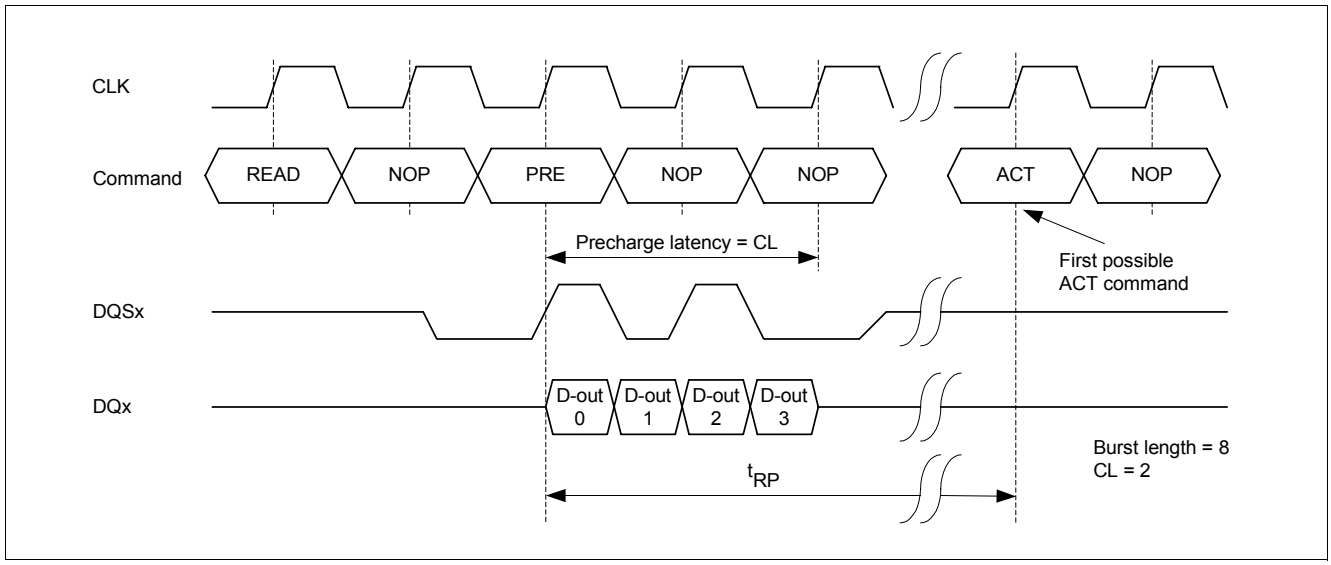

Figure 26 Read interrupted by Precharge

3.6.4 Write Interrupted by a Write

A Burst Write can be interrupted before completion of the burst by a new Write Command. The minimum distance between two different Write commands is one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied. The Write to Write interval (CAS a to CAS b command period) is defined by the parameter t_{CCD}.

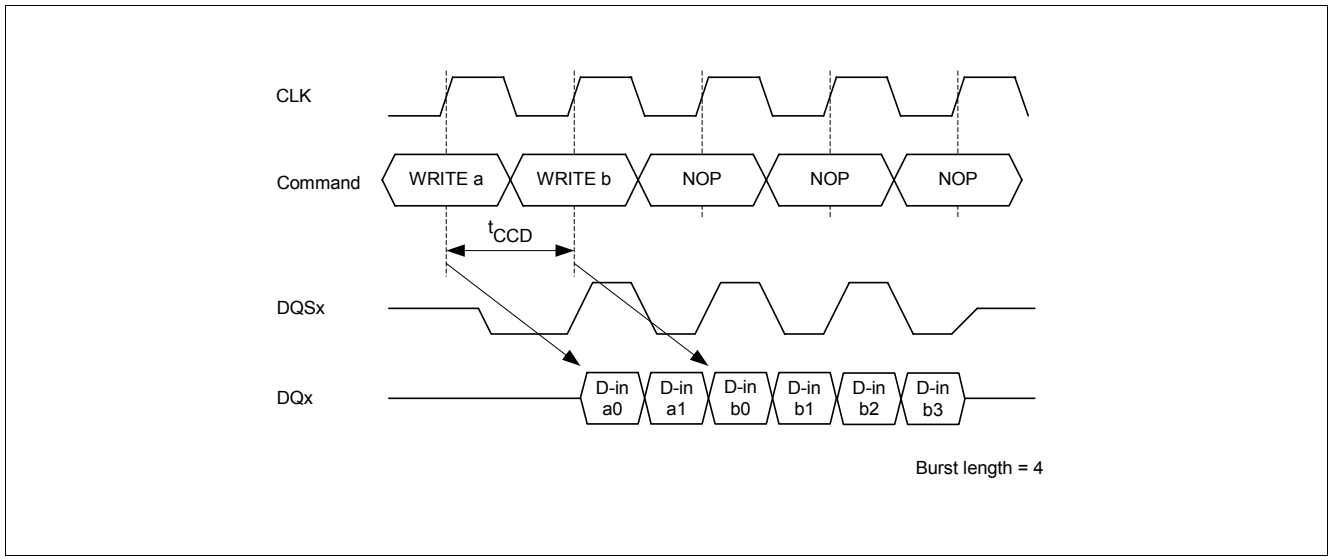

Figure 27 Write interrupted by Write

3.6.5 Write Interrupted by a Read

A Burst Write can be interrupted by a Read command sent to any bank. The DQs must be in the high impedance state at least one clock cycle before the data of the interrupting read appears on the outputs to avoid data contention. Before the Read Command is registered, any residual data from the burst write cycle must be masked by DMx. Data that is presented on the DQ pins before the Read command is initiated, will actually be written to the memory.

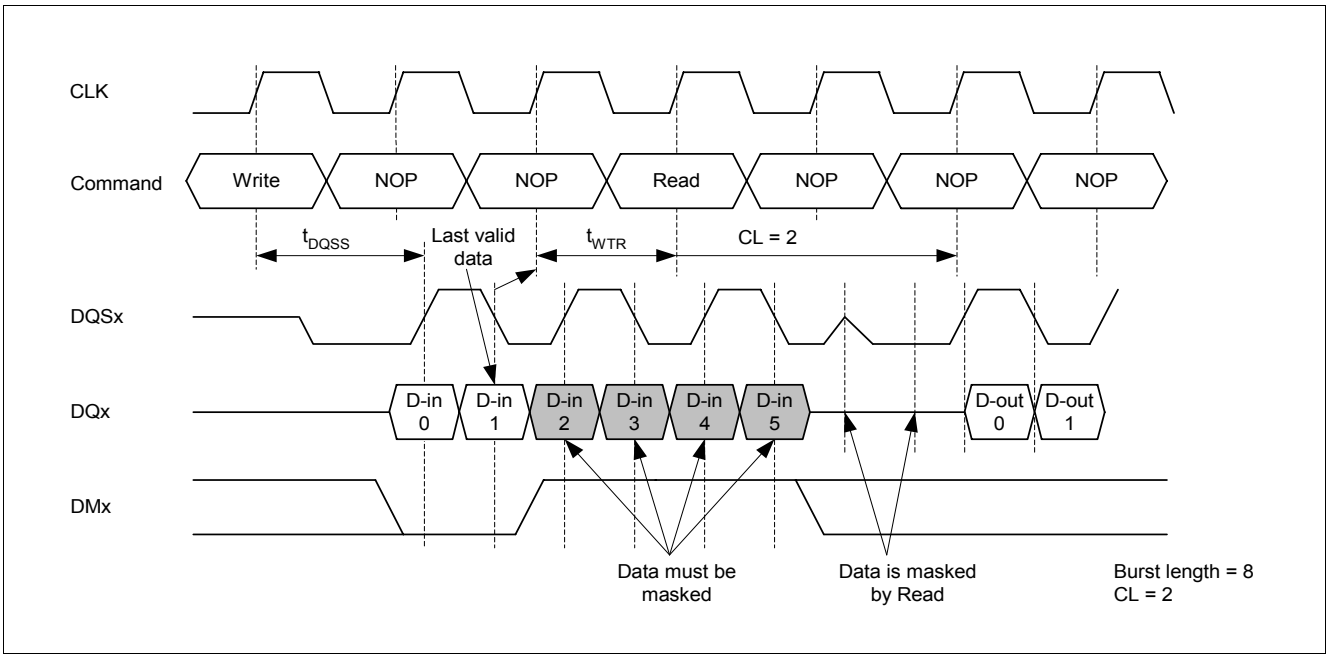

Figure 28 Write interrupted by Read

3.6.6 Write Interrupted by a Precharge

A Burst Write operation can be interrupted before completion of the burst by a Precharge of the same bank. Random column access is allowed. A Write Recovery time (t_{WR}) is required from the last data to Precharge command. When Precharge command is asserted, any residual data from the burst write cycle must be masked by DMx.

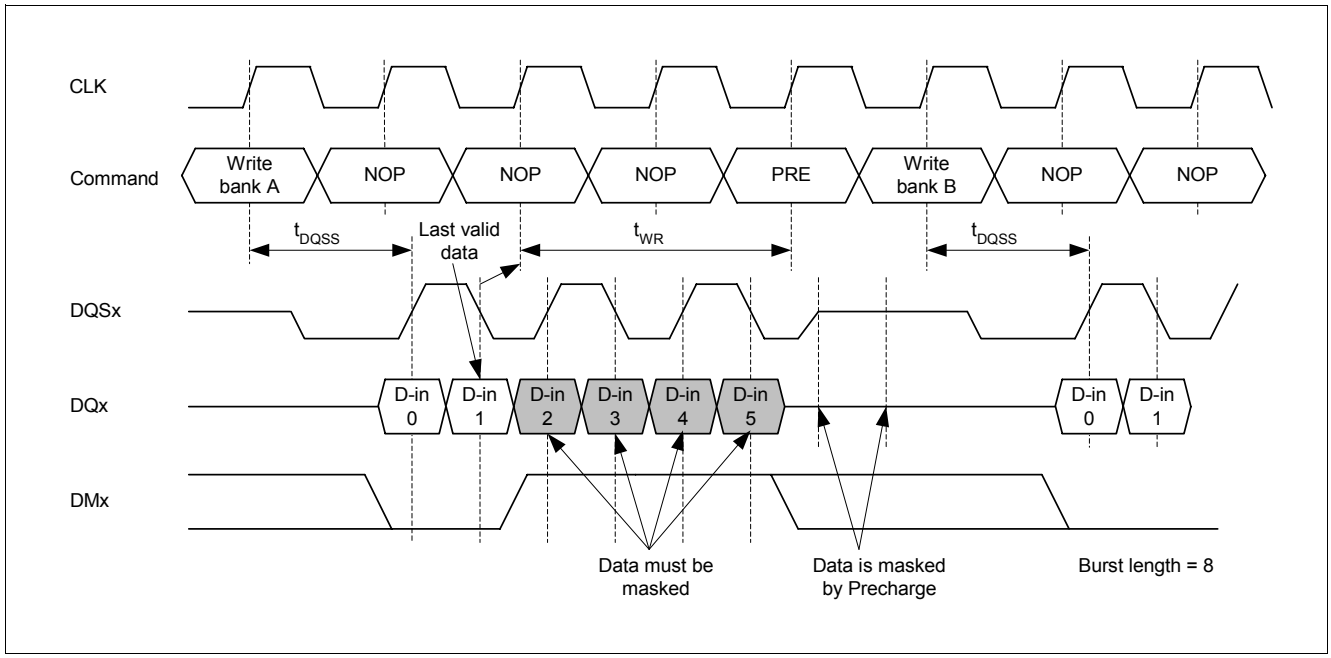

Figure 29 Write interrupted by Precharge

3.7 Operations and Functions

Table 9 Command Overview

Operation	Code	CKE n-1	CKE n	CS#	RAS#	CAS#	WE#	BA0	BA1	A8	A0-7 A9-11
Device Deselect	DESEL	H	X	H	X	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X	X
Mode Register Setup	MRS	H	X	L	L	L	L	0	0	OPCODE	
Extended Mode Register Setup	MRS	H	X	L	L	L	L	1	0	OPCODE	
Bank Activate	ACT	H	X	L	L	H	H	BA	BA	Row Address	
Read	READ	H	X	L	L	H	H	BA	BA	L	Col.
Read with Auto Precharge	READA	H	X	L	H	L	H	BA	BA	H	Col.
Write Command	WRITE	H	X	L	L	H	H	BA	BA	L	Col.
Write Command with Auto Precharge	WRITEA	H	X	L	H	L	H	BA	BA	H	Col.
Burst Stop	BST	H	X	L	H	H	L	X	X	X	X
Precharge Single Bank	PRE	H	X	L	L	H	L	BA	BA	L	X
Precharge All Banks	PREAL	H	X	L	L	H	L	X	X	H	X
Auto Refresh	AREF	H	H	L	L	L	H	X	X	X	X
Self Refresh Entry	SREFEN	H	L	L	L	L	H	X	X	X	X
Self Refresh Exit	SREFEX	L L	H H	H L	X H	X H	X H	X X	X X	X X	X X

Table 9 Command Overview (cont'd)

Operation	Code	CKE n-1	CKE n	CS#	RAS#	CAS#	WE#	BA0	BA1	A8	A0-7 A9-11
Power Down Mode Entry *(Note)*	PWDNEN	H H	L L	H L	X H	X H	X H	X X	X X	X X	X X
Power Down Mode Exit	PWDNEX	L	H	H L	X valid	X valid	X valid	X	X	X	X

Note: The Power Down Mode Entry command is illegal during Burst Read or Burst Write operations.

3.8 Function Truth Tables

Table 10 lists all abbreviations used in **Table 11** and **Table 12**.

Table 10 Abbreviations

H	High Level
L	Low Level
X	Don't Care
V	Valid Data Input
RA	Row Address
BA	Bank Address
PA	Precharge All
NOP	No Operation
CA	Column Address
Ax	Address Line x

Table 11 Function Truth Table I

Current State	Command	Address	Action	Notes
IDLE	DESEL	X	NOP	3)
	NOP	X	NOP	3)
	BST	X	NOP	3)
	READ / READA	BA,CA,A8	ILLEGAL	1)
	WRITE / WRITEA	BA,CA,A8	ILLEGAL	1)
	ACT	BA, RA	Bank Active	
	PRE / PREAL	BA, A8	NOP	
	AREF / SREF	X	AUTO-Refresh or Self-Refresh	4)
	MRS / EMRS	Op-Code	Mode Register Set or Extended Mode Register Set	

Table 11 Function Truth Table I (cont'd)

Current State	Command	Address	Action	Notes
ROW ACTIVE	DESEL	X	NOP	
	NOP	X	NOP	
	BST	X	NOP	
	READ / READA	BA, CA, A8	Begin Read, Determine Auto Precharge	9)
	WRITE / WRITEA	BA, CA, A8	Begin Write, Determine Auto Precharge	9)
	ACT	BA, RA	ILLEGAL	1), 5)
	PRE / PREAL	BA, A8	Precharge / Precharge All	6)
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
READ	DESEL	X	Continue burst to end	
	NOP	X	Continue burst to end	
	BST	X	Terminate Burst	
	READ / READA	BA, CA, A8	Terminate burst, Begin New Read, Determine Auto-Prechgarge	7)
	WRITE / WRITEA	BA, CA, A8	ILLEGAL	2), 7)
	ACT	BA, RA	ILLEGAL	1)
	PRE / PREAL	BA ,A8	Terminate Burst / Precharge	
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	Op-Code	ILLEGAL	
READ with Auto Precharge	DESEL	X	Continue burst to end, Precharge	
	NOP	X	Continue burst to end, Precharge	
	BST	BA	ILLEGAL	
	READ / READA	BA, CA, A8	ILLEGAL	
	WRITE / WRITEA	BA, CA, A8	ILLEGAL	
	ACT	BA, RA	ILLEGAL	1)
	PRE / PREAL	BA ,A8	ILLEGAL	1)
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	Op-Code	ILLEGAL	
WRITE	DESEL	X	Continue burst to end	
	NOP	X	Continue burst to end	
	BST	X	ILLEGAL	
	READ / READA	BA, CA, A8	Terminate Burst, Begin Read, Determine Auto-Precharge.	7), 8)
	WRITE / WRITEA	BA, CA, A8	Terminate Burst, Begin new Write, Determine Auto-Precharge	2), 7)
	ACT	BA, RA	ILLEGAL	1)
	PRE / PREAL	BA ,A8	Terminate Burst , Precharge	8)
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	

Table 11 Function Truth Table I (cont'd)

Current State	Command	Address	Action	Notes
WRITE with Autoprecharge	DESEL	X	Continue burst to end, Precharge	
	NOP	X	Continue burst to end, Precharge	
	BST	X	ILLEGAL	
	READ / READA	BA, CA, A8	ILLEGAL	
	WRITE / WRITEA	BA, CA, A8	ILLEGAL	
	ACT	BA, RA	ILLEGAL	1)
	PRE / PREAL	BA ,A8	ILLEGAL	1)
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
ROW ACTIVATING	DESEL	X	NOP (Row Active after t_{RCD})	
	NOP	X	NOP (Row Active after t_{RCD})	
	BST	X	NOP (Row Active after t_{RCD})	
	READ / READA	BA, CA, A8	ILLEGAL	1), 9)
	WRITE / WRITEA	BA, CA, A8	ILLEGAL	1), 9)
	ACT	BA, RA	ILLEGAL	1), 5)
	PRE / PREAL	BA ,A8	ILLEGAL	1), 6)
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
PRECHARGE	DESEL	X	NOP (Row Idle after t_{RP})	
	NOP	X	NOP (Row Idle after t_{RP})	
	BST	X	NOP (Row Idle after t_{RP})	
	READ / READA	BA, CA, A8	ILLEGAL	1)
	WRITE / WRITEA	BA, CA, A8	ILLEGAL	1)
	ACT	BA, RA	ILLEGAL	1)
	PRE / PREAL	BA ,A8	NOP (Row Idle after t_{RP})	1)
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
WRITE RECOVERING	DESEL	X	NOP (Row Active after t_{WR})	
	NOP	X	NOP (Row Active after t_{WR})	
	BST	X	NOP (Row Active after t_{WR})	
	READ / READA	BA, CA, A8	Begin Read, Determine Auto-Prechgarge	2)
	WRITE / WRITEA	BA, CA, A8	Begin Write, Determine Auto-Prechgarge	
	ACT	BA, RA	ILLEGAL	2)
	PRE / PREAL	BA ,A8	ILLEGAL	1),10)
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	

Table 11 Function Truth Table I (cont'd)

Current State	Command	Address	Action	Notes
WRITE RECOVERING with Auto-precharge	DESEL	X	NOP (Precharge after t_{WR})	
	NOP	X	NOP (Precharge after t_{WR})	
	BST	X	NOP (Precharge after t_{WR})	
	READ / READA	BA, CA, A8	ILLEGAL	1), 2)
	WRITE / WRITEA	BA, CA, A8	ILLEGAL	1)
	ACT	BA, RA	ILLEGAL	1)
	PRE / PREAL	BA ,A8	ILLEGAL	1)
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
REFRESH	DESEL	X	NOP (Idle after t_{RC})	
	NOP	X	NOP (Idle after t_{RC})	
	BST	X	NOP (Idle after t_{RC})	
	READ / READA	BA, CA, A8	ILLEGAL	
	WRITE / WRITEA	BA, CA, A8	ILLEGAL	
	ACT	BA, RA	ILLEGAL	11)
	PRE / PREAL	BA ,A8	ILLEGAL	
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	
(EXTENDED MODE REGISTER SET)	DESEL	X	NOP (Idle after two clocks)	
	NOP	X	NOP (Idle after two clocks)	
	BST	X	NOP (Idle after two clocks)	
	READ / READA	BA, CA, A8	ILLEGAL	
	WRITE / WRITEA	BA, CA, A8	ILLEGAL	
	ACT	BA, RA	ILLEGAL	
	PRE / PREAL	BA ,A8	ILLEGAL	
	AREF / SREF	X	ILLEGAL	
	MRS / EMRS	OP-Code	ILLEGAL	

1) Illegal to bank specified states; function may be legal in the bank indicated by BAx, depending on the state of that bank

2) Must satisfy bus contention, bus turn around, write recovery requirements.

3) If both banks are idle, and CKE is inactive, the device will enter Power Down Mode. All input buffers except CKE, CLK and CLK# will be disabled.

4) If both banks are idle, and CKE is deactivated coincidentally with an AutoRefresh command, the device will enter SelfRefresh Mode. All input buffers except CKE will be disabled.

5) Illegal, if t_{RRD} is not satisfied.

6) Illegal, if t_{RAS} is not satisfied.

7) Must satisfy burst interrupt condition.

8) Must mask two preceding data bits with the DM pin.

9) Illegal, if t_{RCD} is not satisfied.

10) Illegal, if t_{WR} is not satisfied.

11) Illegal, if t_{RC} is not satisfied.

Note: All entries assume the CKE was High during the preceding clock cycle

Table 12 Function Truth Table for CKE

Current State	CKE n-1	CKE n	CS#	RAS #	CAS #	WE#	Address	Action	Notes
SELF REFRESH	H	X	X	X	X	X	X	INVALID	1)
	L	H	H	X	X	X	X	Exit Self-Refresh (Idle after t_{SRX})	1)
	L	H	L	H	H	H	X	Exit Self-Refresh (Idle after t_{SRX})	1)
	L	H	L	H	H	X	X	ILLEGAL	1)
	L	H	L	H	H	X	X	ILLEGAL	1)
	L	H	L	L	L	X	X	ILLEGAL	1)
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	1)
POWER DOWN	H	X	X	X	X	X	X	INVALID	
	L	H	X	X	X	X	X	Exit Power Down (Idle after t_{PDEX})	
	L	L	X	X	X	X	X	NOP (Maintain Power Down)	
ALL BANKS IDLE	H	H	X	X	X	X	X	Refer to Function Truth Table	2)
	H	L	L	L	L	H	X	Enter Self Refresh	3)
	H	L	H	X	X	X	X	Enter Power-Down	2)
	H	L	L	H	H	H	X	Enter Power-Down	2)
	H	L	L	H	H	L	X	ILLEGAL	2)
	H	L	L	H	L	X	X	ILLEGAL	2)
	H	L	L	L	X	X	X	ILLEGAL	2)
	L	X	X	X	X	X	X	Refer to Power Down in this table	
All other states	H	H	X	X	X	X	X	Refer to Funtion Truth Table	

1) CKE low-to-high transition re-enables inputs asynchronously. A minimum setup time to CLK must be satisfied before any commands other than EXIT are executed.

2) Power Down can be entered when all banks are idle (banks can be active or precharged)

3) Self Refresh can be entered only from the Precharge / Idle state.

3.9 DDR SGRAM Simplified State Diagram

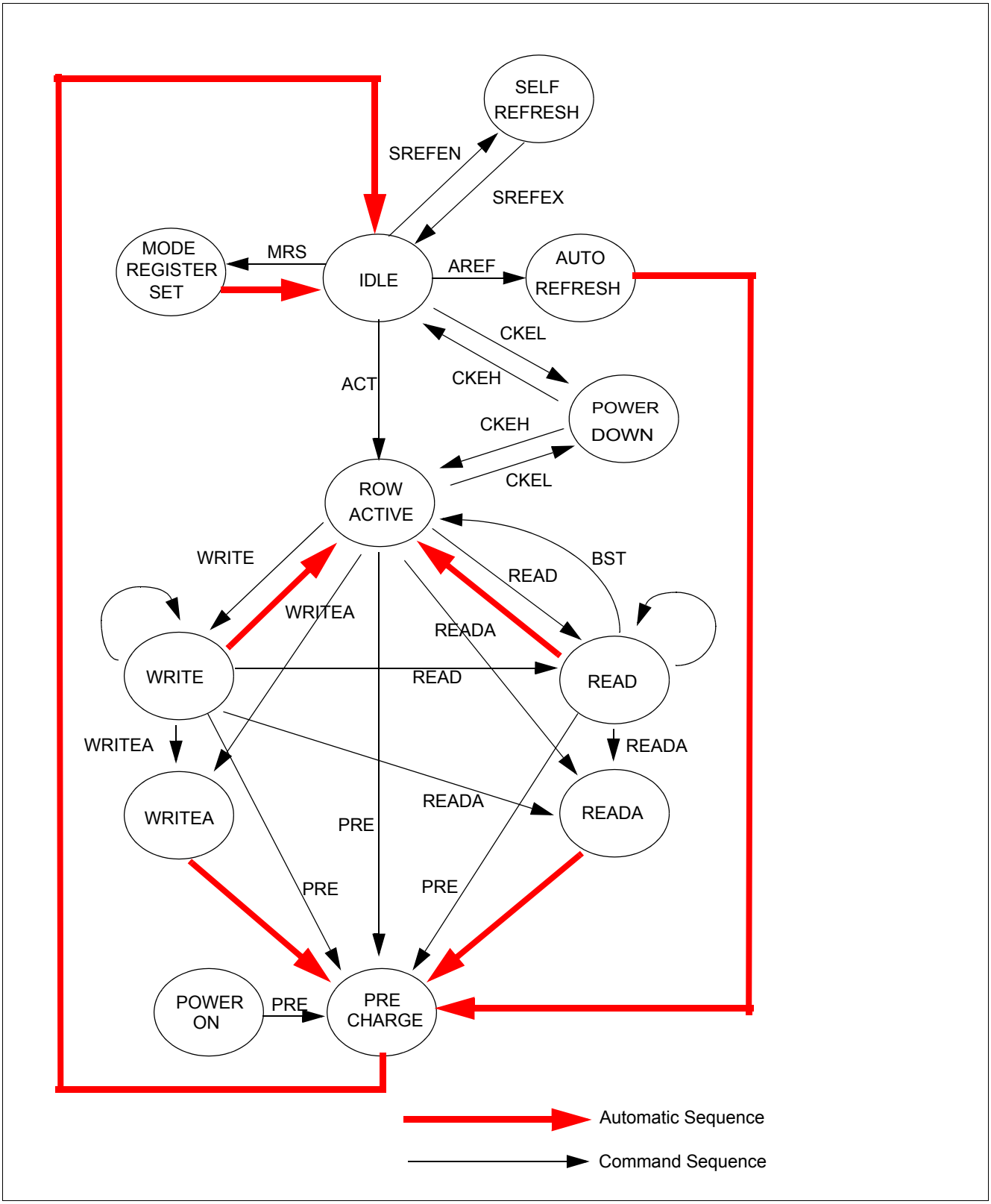

Figure 30 DDR SGRAM Simplified State Diagram

4 Electrical Characteristics

Table 13 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		min.	typ.	max.		
Voltage on I/O pins relative to V_{SS}	V_{IN}, V_{OUT}	–0.5	–	V_{DDQ} + 0.5	V	–
Voltage on Inputs relative to V_{SS}	V_{IN}	–0.5	–	+3.6	V	–
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–0.5	–	+3.6	V	–
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–0.5	–	+3.6	V	–
Operating Temperature (Ambient)	T_A	0	–	+70	°C	–
Storage Temperature (Plastic)	T_{STG}	–55	–	+150	°C	–
Power Dissipation	P_D	–	1.4	–	W	–
Short Circuit Output Current	I_{OUT}	–	50	–	mA	–

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 14 Power & DC Operation Conditions

Parameter	Symbol	Values			Unit	Notes [1]
		min.	typ.	max.		
Power Supply Voltage	V_{DD}	2.38	2.5	2.63	V	L3.6, L4.5[2]
	V_{DD}	2.38	2.5	2.63	V	–3.6, –4.5, –5 [2]
	V_{DD}	2.5	—	2.9	V	–3.6, L3.6 [2][3]
	V_{DD}	2.5	—	2.9	V	–3, –3.3 [2]
Power Supply Voltage for I/O Buffer	V_{DDQ}	2.38	2.5	2.63	V	[2] [4]
Reference Voltage	V_{REF}	0.49 × V_{DDQ}	1.25	0.51 × V_{DDQ}	V	[5] [6]
Termination Voltage	V_{Tt}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	[7]
Input leakage current	I_{IL}	–5	—	5	µA	—
CLK Input leakage current	I_{ILC}	–5	—	5	µA	—
Output leakage current	I_{OL}	–5	—	5	µA	—
Input logic high voltage, DC	V_{IH}	V_{REF} + 0.15	—	V_{DDQ} + 0.3	V	[8]
Input logic low voltage, DC	V_{IL}	V_{SSQ} - 0.3	—	V_{REF} - 0.15	V	[9]
Output Levels: Matched Impedance Mode 2.5V						
High Current at V_{OUT} = V_{DDQ}-0,373V	I_{OH}	–5	—	—	mA	—
Low Current at V_{OUT} = 0.373V	I_{OL}	5	—	—	mA	—
Output Levels: SSTL2 Weak Mode 2.5V						
High Current at V_{OUT} = V_{DDQ} – 0,373V	I_{OH}	–5	—	—	mA	—
Low Current at V_{OUT} = 0.373V	I_{OL}	5	—	—	mA	—

1) T_A = 0 to 70 °C; V_{SS} = 0 V
2) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
3) The speed sorts L3.6 and –3.6 support both V_{DD} modes: 2.5V ±5% and 2.5V – 2.9V
4) V_{DDQ} = 2.5 V -/+5%
5) Typically the value of V_{REF} is expected to be 0.5 * V_{DDQ} of the transmitting device. V_{REF} is expected to track variations in V_{DDQ}
6) Peak to peak AC noise on V_{REF} may not exceed 2% V_{REF} (DC)
7) V_{TT} of the transmitting device must track V_{REF} of the receiving device
8) Overshoots of V_{IH} must be limited to a voltage < (V_{DDQ} + 1.5 V) and a pulse width < 0.33 of the clock pulse
9) Undershoots of V_{IL} must be limited to a voltage > -1.5 V and a pulse width < 0.33 of the clock pulse

Table 15 AC Operation Conditions

Parameter	Symbol	Values			Unit	Notes
		min.	typ.	max.		
Input logic high voltage	V_{IH}	V_{REF} + 0.50	—	V_{DDQ} + 0.3	V	L3.6, L4.5
		V_{REF} + 0.60	—	V_{DDQ} + 0.3	V	–5.0
		V_{REF} + 0.50	—	V_{DDQ} + 0.3	V	–3, –3.3, –3.6, –4.5
Input logic low voltage	V_{IL}	V_{SSQ} - 0.3	—	V_{REF} - 0.50	V	L3.6, L4.5
		V_{SSQ} - 0.3	—	V_{REF} - 0.60	V	–5.0
		V_{SSQ} - 0.3	—	V_{REF} - 0.50	V	–3, –3.3, –3.6, –4.5
Clock Differential Input Voltage (CLK/$\overline{\text{CLK}}$)	V_{ID}	1.2	—	V_{DDQ} + 0.6	V	L4.5
		1.0	—	V_{DDQ} + 0.6	V	L3.6
		1.2	—	V_{DDQ} + 0.6	V	–4.5, –5.0
		1.0	—	V_{DDQ} + 0.6	V	–3, –3.3, –3.6, –4.5
Clock Input Crossing Point (CLK/$\overline{\text{CLK}}$)	V_{IX}	V_{REF} - 0.2	V_{REF}	V_{REF} + 0.2	V	—
I/O Reference Voltage	V_{REF}	0.49 × V_{DDQ}	—	0.51 × V_{DDQ}	V	—
Input Slew Rate	r_I	1.0	—	—	V/ns	—

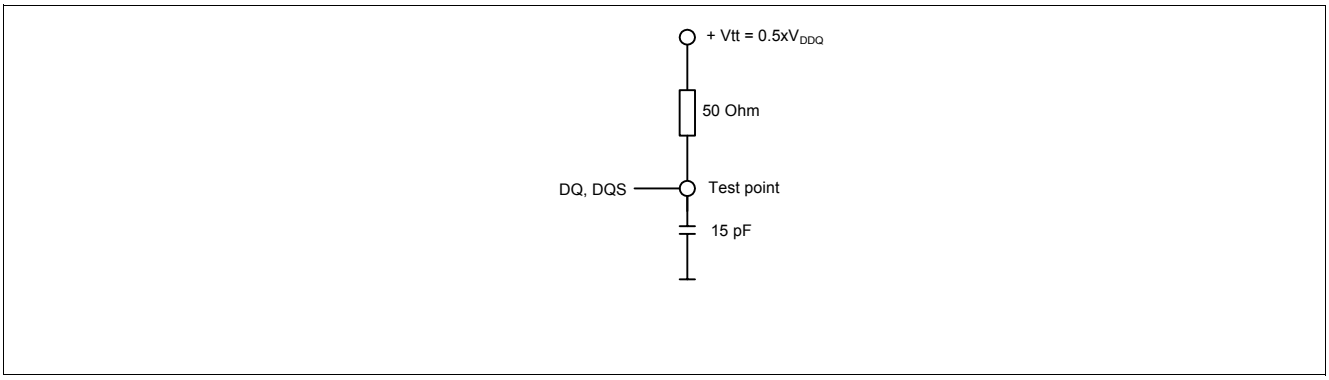

Figure 31 Output Test Circuit

Table 16 Pin Capacitances

Pin	min.	max.	Unit
A11.. A0, BA1, BA0, CKE, $\overline{\text{CS}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, $\overline{\text{WE}}$	1.0	2.5	pF
CLK, $\overline{\text{CLK}}$	1.0	2.5	pF

Table 16 Pin Capacitances

Pin	min.	max.	Unit
DQ0.. DQ31, DQS0 .. DQS3	1.0	3.0	pF
DM0.. DM3	1.0	3.0	pF

Table 17 Timing Parameters for speed sorts –3, –3.3, –3.6, –4.5, and –5

Part Number Extension		–3		–3.3		–3.6		–4.5		–5		Unit	Note[1]
Interface		MIM		MIM		MIM		WM/MIM		WM/MIM		—	[2]
Parameter	Symbol	min.	max.	min.	max.	min.	max.	min.	max.	min.	max.	—	—
Clock and Clock Enable													
Clock Cycle Time	t_{CK}	3.0	5.0	3.3	5.0	3.6	5.0	4.5	5.5	5.0	5.5	ns	CL = 4
	t_{CK}	4.0	5.0	4.0	5.0	4.2	5.0	4.5	5.5	5.0	5.5	ns	CL = 3
System frequency	f_{CK}	200	333	200	300	200	278	183	222	183	200	MHz	CL = 4
	f_{CK}	200	250	200	250	200	238	183	222	183	200	MHz	CL = 3
Clock high level width	t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	—
Clock low level width	t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	—
Minimum clock half period	t_{HP}	t_{CH}, t_{CL}	—	t_{CH}, t_{CL}	—	t_{CH}, t_{CL}	—	t_{CH}, t_{CL}	—	t_{CH}, t_{CL}	—	t_{CK}	—
Command and Address Setup and Hold Times													
Address and Command input setup time	t_{IS}	0.65	—	0.65	—	0.75	—	1.0	—	1.0	—	ns	—
Address and Command input hold time	t_{IH}	0.65	—	0.65	—	0.75	—	1.0	—	1.0	—	ns	—
Common Parameters													
Row Cycle Time	t_{RC}	39	—	42.9	—	46.8	—	54	—	60	—	ns	—
Row Cycle Time in Auto Refresh	t_{RFC}	45	—	49.5	—	54	—	63	—	70	—	ns	—
Row Active Time	t_{RAS}	27	15.7k	29.7	15.7k	32.4	15.7k	36	15.7k	40	15.7k	ns	—
ACTIVE to READ with Auto precharge command	t_{RAP}	$t_{RAS\ (min.)}$- *(burst length * t_{CK} /2)*										ns	—
Row Precharge Time	t_{RP}	12	—	13.2	—	14.4	—	18	—	20	—	ns	—
Activate(a) to Activate(b) Command period	t_{RRD}	9.0	—	9.0	—	9.0	—	9.0	—	9.0	—	ns	—
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command period	t_{CCD}	1	—	1	—	1	—	1	—	1	—	t_{CK}	—
Last data in to Active (t_{WR} + t_{RP})	t_{DAL}	6	—	6	—	6	—	6	—	6	—	t_{CK}	—

Table 17 Timing Parameters for speed sorts –3, –3.3, –3.6, –4.5, and –5 (cont'd)

Part Number Extension		–3		–3.3		–3.6		–4.5		–5		Unit	Note[1]
Interface		MIM		MIM		MIM		WM/MIM		WM/MIM		—	[2]
Parameter	Symbol	min.	max.	min.	max.	min.	max.	min.	max.	min.	max.	—	—
Read Cycle Timing Parameters for Data and Data Strobe													
Data Access Time from Clock	t_{AC}	-0.5	+0.5	-0.5	+0.5	-0.55	+0.55	-0.7	+0.7	-0.7	+0.7	ns	—
DQS edge to Clock edge skew	t_{DQSCK}	-0.5	+0.5	-0.5	+0.5	-0.55	+0.55	-0.7	+0.7	-0.7	+0.7	ns	—
DQS Read Preamble	t_{RPRE}	0.7	0.9	0.7	0.9	0.7	0.9	0.7	0.9	0.7	0.9	t_{CK}	—
DQS Read Postamble	t_{RPST}	0.8	1.1	0.8	1.1	0.8	1.1	0.8	1.1	0.8	1.1	t_{CK}	—
Row to Column Delay Time for Reads	t_{RCDDC}	4	—	4	—	4	—	4	—	4	—	t_{CK}	—
DQS edge to output data edge skew	t_{DQSQ}	—	+0.3	—	+0.3	—	+0.33	—	+0.45	—	+0.5	ns	—
Data hold skew factor	t_{QHS}	—	0.33	—	0.33	—	0.36	—	0.45	—	0.5	ns	—
Data Output Hold time from DQS	t_{QH}	t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		ns	—
Write Cycle Timing Parameters for Data and Data Strobe													
Row to Column Delay Time for Writes	t_{RCDWR}	2	—	2	—	2	—	2	—	2	—	t_{CK}	—
Clock to rising Edge DQS (Write Latency)	t_{DQSS}	0.75	1.1	0.75	1.1	0.75	1.1	0.75	1.25	0.75	1.25	t_{CK}	—
Data-in to DQS Setup Time	t_{QDQSS}	0.40	—	0.40	—	0.40	—	0.6	—	0.6	—	ns	—
Data-in to DQS Hold Time	t_{QDQSH}	0.40	—	0.40	—	0.40	—	0.6	—	0.6	—	ns	—
Data Mask to DQS Setup Time	t_{DMDQSS}	0.40	—	0.40	—	0.40	—	0.6	—	0.6	—	ns	—
Data Mask to DQS Hold Time	t_{DMDQSH}	0.40	—	0.40	—	0.40	—	0.6	—	0.6	—	ns	—
Clock to DQS Write Preamb. Setup Time	t_{WPRES}	0	—	0	—	0	—	0	—	0	—	t_{CK}	—
Clock to DQS Write Preamble Hold Time	t_{WPREH}	0.25	—	0.25	—	0.25	—	0.25	—	0.25	—	t_{CK}	—
DQS Write Postamble Hold Time	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	—
Write Recovery Time	t_{WR}	2	—	2	—	2	—	2	—	2	—	t_{CK}	[3]

Table 17 Timing Parameters for speed sorts –3, –3.3, –3.6, –4.5, and –5 (cont'd)

Part Number Extension		–3		–3.3		–3.6		–4.5		–5		Unit	Note[1]
Interface		MIM		MIM		MIM		WM/MIM		WM/MIM		—	[2]
Parameter	Symbol	min.	max.	min.	max.	min.	max.	min.	max.	min.	max.	—	—
Internal WRITE to READ command delay	t_{WTR}	1	—	1	—	1	—	1	—	1	—	t_{CK}	—
Write DQS High level Width	t_{DQSH}	0.35	0.65	0.35	0.65	0.35	0.65	0.35	0.65	0.35	0.65	t_{CK}	—
Write DQS Low level Width	t_{DQSL}	0.35	0.65	0.35	0.65	0.35	0.65	0.35	0.65	0.35	0.65	t_{CK}	—
Refresh Cycle													
Refresh Period (4096 cycles)	t_{REF}	—	32	—	32	—	32	—	32	—	32	ms	—
Average periodic refresh interval	t_{REFC}	—	7.8	—	7.8	—	7.8	—	7.8	—	7.8	us	—
Refresh to Refresh command interval	t_{REFC}	—	15.7	—	15.7	—	15.7	—	15.7	—	15.7	µs	—
Mode Setup, Power Down & Self Refresh													
Mode Register Set cycle time	t_{MRD}	2	—	2	—	2	—	2	—	2	—	t_{CK}	—
Self Refresh Exit time	t_{SREX}	200	—	200	—	200	—	200	—	200	—	t_{CK}	—
Power Down Exit time	t_{PDEX}	$2*t_{CK} + t_{IS}$	—	$2*t_{CK} + t_{IS}$	—	$2*t_{CK} + t_{IS}$	—	$1*t_{CK} + t_{IS}$	—	$1*t_{CK} + t_{IS}$	—	ns	—

1) All parameters only valid for: T_A = 0 to 70 °C; V_{SS} = 0 V; 2.5 V < V_{DD} < 2.9 V for –3 and –3.3; 2.375 V < V_{DD} < 2.9 V for –3.6; V_{DD} = 2.5 V ±0.125 V for –4.5 and –5; V_{DDQ} = 2.5 V ±0.125 V

2) Maximum clock rate is only guaranteed with the specified interface. The SSTL2-Weak Mode interface is limited to a maximum speed of 250MHz.

3) The Write Recovery Time starts at the first rising edge of clock after the last valid (falling) DQS edge of the slowest DQS signal.

Table 18 Timing Parameters for speed sorts L3.6 and L4.5

Part Number Extension		L3.6		L4.5		Unit	Note [1]
Interface		MIM		WM/MIM		—	[2]
Parameter	Symbol	min.	max.	min.	max.	—	—
Clock and Clock Enable							
Clock Cycle Time		3.6	6.0	4.5	6.0	ns	CL = 4
	t_{CK}	4.2	10	4.5	10	ns	CL = 3
System frequency	f_{CK}	166	278	166	222	MHz	CL = 4
	f_{CK}	100	238	100	222	MHz	CL = 3
Clock high level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	—

Table 18 Timing Parameters for speed sorts L3.6 and L4.5 (cont'd)

Part Number Extension		**L3.6**		**L4.5**		**Unit**	**Note [1)]**
Interface		**MIM**		**WM/MIM**		**—**	**[2)]**
Parameter	**Symbol**	**min.**	**max.**	**min.**	**max.**	**—**	**—**
Clock low level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	—
Minimum clock half period	t_{HP}	t_{CH}, t_{CL}	—	t_{CH}, t_{CL}	—	t_{CK}	—
Command and Address Setup and Hold Times							
Address and Command input setup time	t_{IS}	0.75	—	1.0	—	ns	—
Address and Command input hold time	t_{IH}	0.75	—	1.0	—	ns	—
Common Parameters							
Row Cycle Time	t_{RC}	46.8	—	54	—	ns	—
Row Cycle Time in Auto Refresh	t_{RFC}	54	—	63	—	ns	—
Row Active Time	t_{RAS}	32.4	15.7k	36	15.7k	ns	—
ACTIVE to READ with Auto precharge command	t_{RAP}	$t_{RAS\ (min.)}$- *(burst length * t_{CK} /2)*				ns	—
Row Precharge Time	t_{RP}	14.4	—	18	—	ns	—
Activate(a) to Activate(b) Command period	t_{RRD}	9.0	—	9.0	—	ns	—
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command period	t_{CCD}	1	—	1	—	t_{CK}	—
Last data in to Active ($t_{WR} + t_{RP}$)	t_{DAL}	6	—	6	—	t_{CK}	—
Read Cycle Timing Parameters for Data and Data Strobe							
Data Access Time from Clock	t_{AC}	-0.55	+0.55	-0.7	+0.7	ns	—
DQS edge to Clock edge skew	t_{DQSCK}	-0.55	+0.55	-0.7	+0.7	ns	—
DQS Read Preamble	t_{RPRE}	0.7	0.9	0.7	0.9	t_{CK}	—
DQS Read Postamble	t_{RPST}	0.8	1.1	0.8	1.1	t_{CK}	—
Row to Column Delay Time for Reads	t_{RCDDC}	4	—	4	—	t_{CK}	—
DQS edge to output data edge skew	t_{DQSQ}	—	+0.33	—	+0.45	ns	—
Data hold skew factor	t_{QHS}	—	0.36	—	0.45	ns	—
Data Output Hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$		$t_{HP} - t_{QHS}$		ns	—
Write Cycle Timing Parameters for Data and Data Strobe							
Row to Column Delay Time for Writes	t_{RCDWR}	2	—	2	—	t_{CK}	—
Clock to rising Edge DQS (Write Latency)	t_{DQSS}	0.75	1.1	0.75	1.25	t_{CK}	—
Data-in to DQS Setup Time	t_{QDQSS}	0.40	—	0.6	—	ns	—
Data-in to DQS Hold Time	t_{QDQSH}	0.40	—	0.6	—	ns	—
Data Mask to DQS Setup Time	t_{DMDQSS}	0.40	—	0.6	—	ns	—
Data Mask to DQS Hold Time	t_{DMDQSH}	0.40	—	0.6	—	ns	—
Clock to DQS Write Preamb. Setup Time	t_{WPRES}	0	—	0	—	t_{CK}	—
Clock to DQS Write Preamble Hold Time	t_{WPREH}	0.25	—	0.25	—	t_{CK}	—
DQS Write Postamble Hold Time	t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}	—
Write Recovery Time	t_{WR}	2	—	2	—	t_{CK}	[3)]

Table 18 Timing Parameters for speed sorts L3.6 and L4.5 (cont'd)

Part Number Extension		L3.6		L4.5		Unit	Note [1]
Interface		**MIM**		**WM/MIM**		—	[2]
Parameter	**Symbol**	**min.**	**max.**	**min.**	**max.**	—	—
Internal WRITE to READ command delay	t_{WTR}	1	—	1	—	t_{CK}	—
Write DQS High level Width	t_{DQSH}	0.35	0.65	0.35	0.65	t_{CK}	—
Write DQS Low level Width	t_{DQSL}	0.35	0.65	0.35	0.65	t_{CK}	—
Refresh Cycle							
Refresh Period (4096 cycles)	t_{REF}	—	32	—	32	ms	—
Average periodic refresh interval	t_{REFC}	—	7.8	—	7.8	us	—
Refresh to Refresh command interval	t_{REFC}	—	15.7	—	15.7	us	—
Mode Setup, Power Down & Self Refresh							
Mode Register Set cycle time	t_{MRD}	2	—	2	—	t_{CK}	—
Self Refresh Exit time	t_{SREX}	200	—	200	—	t_{CK}	—
Power Down Exit time	t_{PDEX}	$2*t_{CK}+t_{IS}$	—	$1*t_{CK}+t_{IS}$	—	ns	—

1) All parameters only valid for: T_A = 0 to 70 °C; V_{SS} = 0 V; 2.375 V < V_{DD} < 2.9 V for L3.6; V_{DD} = 2.5 V ± 0.125 V for L4.5; V_{DDQ} = 2.5 V ± 0.125 V

2) Maximum clock rate is only guaranteed with the specified interface. The SSTL2-Weak Mode interface is limited to a maximum speed of 250MHz.

3) The Write Recovery Time starts at the first rising edge of clock after the last valid (falling) DQS edge of the slowest DQS signal.

Table 19 HYB25D128323C–3

Frequency / t_{CK}	CAS latency	t_{RC}	t_{RFC}	t_{RAS}	t_{RP}	t_{WR}	t_{RRD}	t_{DAL}	t_{RCDRD}	t_{RCDWR}	Units
333 MHz / 3.0 ns	4	13	15	9	4	2	3	6	4	2	t_{CK}
300 MHz / 3.3 ns	4	13	15	9	4	2	3	6	4	2	t_{CK}
278 MHz / 3.6 ns	4	13	15	9	4	2	3	6	4	2	t_{CK}
250 MHz / 4.0 ns	3	12	14	8	4	2	3	6	3	2	t_{CK}
222 MHz / 4.5 ns	3	10	12	7	3	2	2	5	3	2	t_{CK}
200 MHz / 5.0 ns	3	9	11	6	3	2	2	5	3	2	t_{CK}

Table 20 HYB25D128323C–3.3

Frequency / t_{CK}	CAS latency	t_{RC}	t_{RFC}	t_{RAS}	t_{RP}	t_{WR}	t_{RRD}	t_{DAL}	t_{RCDRD}	t_{RCDWR}	Units
300 MHz / 3.3 ns	4	13	15	9	4	2	3	6	4	2	t_{CK}
278 MHz / 3.6 ns	4	13	15	9	4	2	3	6	4	2	t_{CK}
250 MHz / 4.0 ns	3	12	14	8	4	2	3	6	3	2	t_{CK}
222 MHz / 4.5 ns	3	10	12	7	3	2	2	5	3	2	t_{CK}
200 MHz / 5.0 ns	3	9	11	6	3	2	2	5	3	2	t_{CK}

Table 21 HYB25D128323C–3.6

Frequency / t_{CK}	CAS latency	t_{RC}	t_{RFC}	t_{RAS}	t_{RP}	t_{WR}	t_{RRD}	t_{DAL}	t_{RCDRD}	t_{RCDWR}	Units
278 MHz / 3.6 ns	4	13	15	9	4	2	3	6	4	2	t_{CK}
250 MHz / 4.0 ns	4	13	15	9	4	2	3	6	4	2	t_{CK}
222 MHz / 4.5 ns	3	12	14	8	4	2	2	6	4	2	t_{CK}
200 MHz / 5.0 ns	3	10	12	7	3	2	2	5	3	2	t_{CK}

Table 22 HYB25D128323C–4.5

Frequency / t_{CK}	CAS latency	t_{RC}	t_{RFC}	t_{RAS}	t_{RP}	t_{WR}	t_{RRD}	t_{DAL}	t_{RCDRD}	t_{RCDWR}	Units
222 MHz / 4.5 ns	3	12	14	8	4	2	2	6	4	2	t_{CK}
200 MHz / 5.0 ns	3	12	14	8	4	2	2	6	4	2	t_{CK}
183 MHz / 5.5 ns	3	12	14	8	4	2	2	6	4	2	t_{CK}

Table 23 HYB25D128323C–5

Frequency / t_{CK}	CAS latency	t_{RC}	t_{RFC}	t_{RAS}	t_{RP}	t_{WR}	t_{RRD}	t_{DAL}	t_{RCDRD}	t_{RCDWR}	Units
200 MHz / 5.0 ns	3	12	14	8	4	2	2	6	4	2	t_{CK}
183 MHz / 5.5 ns	3	12	14	8	4	2	2	6	4	2	t_{CK}

Table 24 HYB25D128323CL3.6

Frequency / t_{CK}	CAS latency	t_{RC}	t_{RFC}	t_{RAS}	t_{RP}	t_{WR}	t_{RRD}	t_{DAL}	t_{RCDRD}	t_{RCDWR}	Units
278 MHz / 3.6 ns	4	13	15	9	4	2	3	6	4	2	t_{CK}
250 MHz / 4.0 ns	4	13	15	9	4	2	3	6	4	2	t_{CK}
222 MHz / 4.5 ns	3	12	14	8	4	2	2	6	4	2	t_{CK}
200 MHz / 5.0 ns	3	10	12	7	3	2	2	5	3	2	t_{CK}
166 MHz / 6.0 ns	3	9	11	6	3	2	2	5	3	2	t_{CK}

Table 25 HYB25D128323CL4.5

Frequency / t_{CK}	CAS latency	t_{RC}	t_{RFC}	t_{RAS}	t_{RP}	t_{WR}	t_{RRD}	t_{DAL}	t_{RCDRD}	t_{RCDWR}	Units
222 MHz / 4.5 ns	3	12	14	8	4	2	2	6	4	2	t_{CK}
200 MHz / 5.0 ns	3	12	14	8	4	2	2	6	4	2	t_{CK}
183 MHz / 5.5 ns	3	12	14	8	4	2	2	6	4	2	t_{CK}
166 MHz / 6.0 ns	3	10	12	7	3	2	2	5	3	2	t_{CK}
143 MHz / 7.0 ns	3	9	11	6	3	2	2	5	3	2	t_{CK}

Table 26 Operating Currents

Parameter & Test Condition	Symbol	–3	–3.3	–3.6	–4.5	–5.0	L3.6	L4.5	Unit	Notes
		max.					typ.	typ.		
OPERATING CURRENT: One bank; Active-Precharge; $t_{RC} = t_{RC(min.)}$; $t_{CK} = t_{CK(min.)}$; DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I_{DD0}	200	190	180	160	150			mA	1)
OPERATING CURRENT: One bank; Active-Read-Precharge; BL=4; CL=4; $t_{RCDDC} = 4*t_{CK}$; $t_{RC} = t_{RC(min.)}$; $t_{CK} = t_{CK(min.)}$; I_{OUT} = 0mA; Address and control inputs changing once per clock cycle	I_{DD1}	230	220	110	190	180			mA	
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; power-down mode; $t_{CK} = t_{CK(min.)}$; CKE=LOW	I_{DD2P}	26	22	22	14	14	10	7	mA	

Table 26 Operating Currents (cont'd)

Parameter & Test Condition	Symbol	–3	–3.3	–3.6	–4.5	–5.0	L3.6	L4.5	Unit	Notes
		max.					typ.	typ.		
IDLE STANDBY CURRENT: CKE=HIGH; CS#=HIGH (DESELECT); All banks idle; $t_{CK} = t_{CK(min.)}$; Address and control inputs changing once per clock cycle; $V_{IN} = V_{REF}$ for DQ, DQS and DM	I_{DD2F}	130	120	110	100	100			mA	
ACTIVE POWER-DOWN STANDBY CURRENT: one bank active; power-down mode; CKE=LOW; $t_{CK} = t_{CK(min.)}$;	I_{DD3P}	65	60	55	50	50			mA	
ACTIVE STANDBY CURRENT: CS#=HIGH; CKE=HIGH; one bank active; $t_{RC} = t_{RC(max.)}$; $t_{CK} = t_{CK(min.)}$; Address and control inputs changing once per clock cycle; DQ, DQS, and DM inputs changing twice per clock cycle	I_{DD3N}	130	120	110	100	100			mA	
OPERATING CURRENT BURST READ: BL=2; READS; Continuous burst; one bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK(min.)}$; Iout=0mA; 50% of data changing on every transfer	I_{DD4R}	370	350	330	290	280	190	160	mA	
OPERATING CURRENT BURST WRITE: BL=2; WRITES; Continuous burst; one bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK(min.)}$; DQ, DQS, and DM changing twice per clock cycle; 50% of data changing on every transfer	I_{DD4W}	370	350	330	290	280	200	175	mA	
AUTO REFRESH CURRENT: $t_{RC} = t_{RFC(min.)}$; $t_{CK} = t_{CK(min.)}$	I_{DD5}	320	300	280	240	230			mA	
SELF REFRESH CURRENT: Self Refresh Mode; CKE<=0.2V; $t_{CK} = t_{CK(min.)}$	I_{DD6}	20	16	16	10	10	4	3	mA	
BURST OPERATING CURRENT 4 bank operation: Four bank interleaving READs; BL=4; with Auto Precharge; $t_{RC} = t_{RC(min.)}$; $t_{CK} = t_{CK(min.)}$; Address and control inputs change only during Active, READ, or WRITE commands	I_{DD7}	430	400	370	320	300			mA	1)

1) Measured with output open.

5 Package Outlines

Module Package
The package is conforming with JEDEC MO-205 Variation BD
General Tolerances according to ISO 8015
The inner matrix of 4 × 4 balls is reserved for thermal contacts

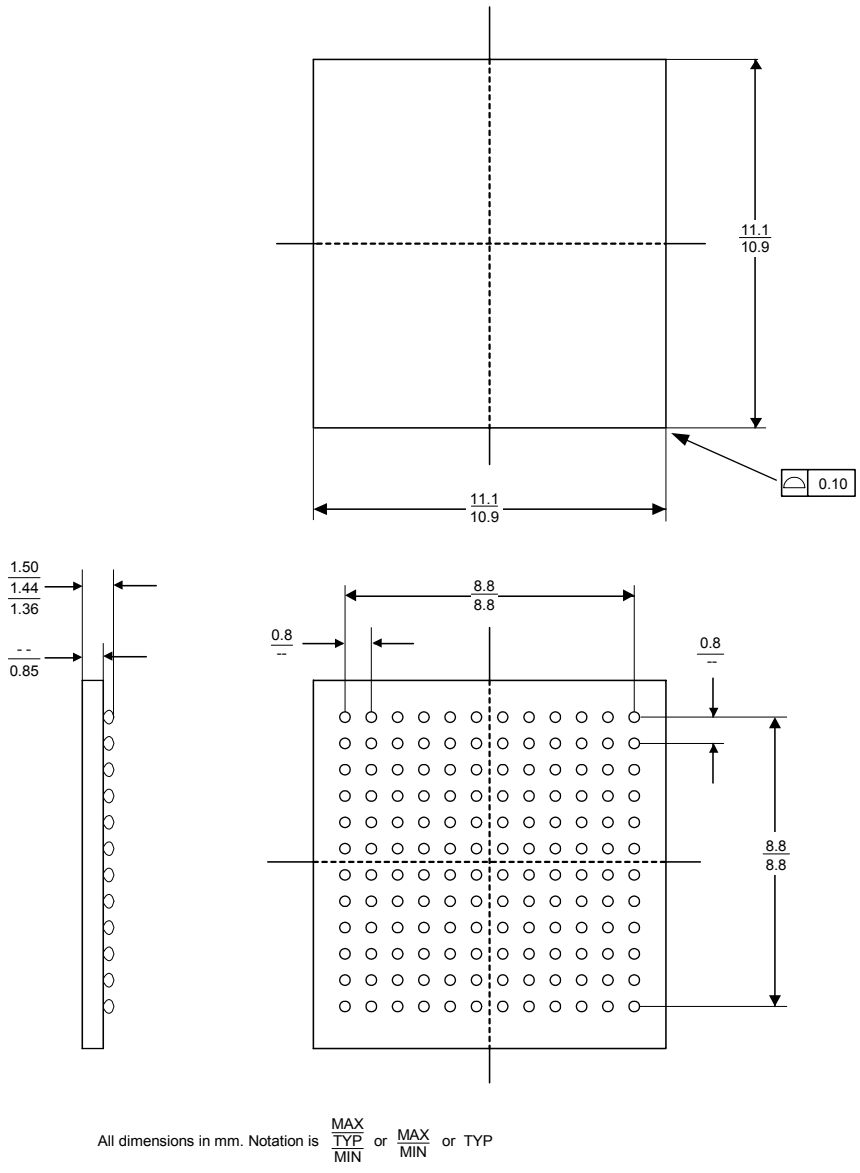

Figure 32 Package Outlines

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