



FPF1203 / FPF1203L / FPF1204 / FPF12045

IntelliMAX™ Ultra-Small, Slew-Rate-Controlled Load Switch

Features

- 1.2 V to 5.5 V Input Voltage Operating Range
- Typical R_{ON} :
 - 45 m Ω at $V_{IN}=5.5$ V
 - 55 m Ω at $V_{IN}=3.3$ V
 - 90 m Ω at $V_{IN}=1.8$ V
 - 185 m Ω at $V_{IN}=1.2$ V
- Slew Rate Control with t_R :
 - FPF1203/FPF1203L/FPF1204: 100 μ s
 - FPF12045: 2 μ s
- Output Discharge Function on FPF1204 / 45
- Low <1.5 μ A Quiescent Current
- ESD Protected: Above 7 kV HBM, 2 kV CDM
- GPIO / CMOS-Compatible Enable Circuitry
- 4-Bump, WLCSP 0.76 mm x 0.76 mm, 0.4 mm Pitch

Description

The FPF1203 / 03L / 04 / 45 are ultra-small integrated IntelliMAX™ load switches with integrated P-channel switch and analog control features. Integrated slew-rate control prevents inrush current and the resulting excessive voltage drop on the power rail. The input voltage range operates from 1.2 V to 5.5 V to provide power-disconnect capability for post-regulated power rails in portable and consumer products. The low shut-off current of 1 μ A (maximum) allows power designs to meet standby and off-power drain specifications.

The FPF1203 / 03L / 04 / 45 are controlled by a logic input (ON pin) compatible with standard CMOS GPIO circuitry found on Field Programmable Gate Array (FPGA) embedded processors. The FPF1203 / 03L / 04 / 45 are available in 0.76 mm x 0.76 mm 4-bump WLCSP.

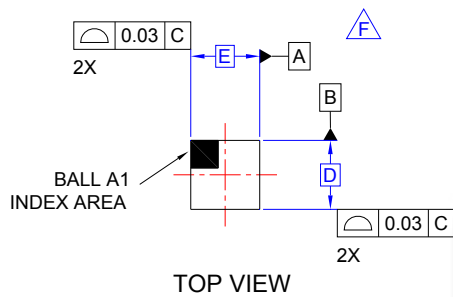
Applications

- Mobile Devices and Smart Phones
- Portable Media Devices
- Tablet PCs
- Advanced Notebook, UMPC, MID
- Portable Medical Devices
- GPS and Navigation Equipment

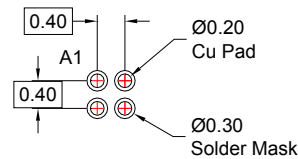
Ordering Information

Part Number	Top Mark	Switch (Typical) at 3.3V _{IN}	Output Discharge	ON Pin Activity	t _R	Package
FPF1203UCX	QL	55 m Ω	NA	Active HIGH	100 μ s	4-Bump, Wafer-Level Chip-Scale Package (WLCSP), 0.76 mm x 0.76 mm, 0.4 mm Pitch
FPF1204UCX	QM	55 m Ω	65 Ω	Active HIGH	100 μ s	
FPF1204BUCX (Backside Laminate)	QM	55 m Ω	65 Ω	Active HIGH	100 μ s	
FPF12045UCX	NC	55 m Ω	65 Ω	Active HIGH	2 μ s	
FPF1203LUCX (Preliminary)	QP	55 m Ω	n/a	Active LOW	100 μ s	

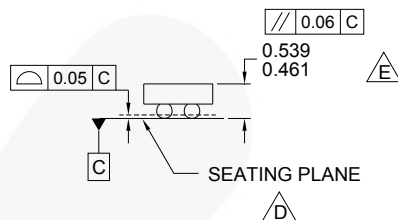
Physical Dimensions



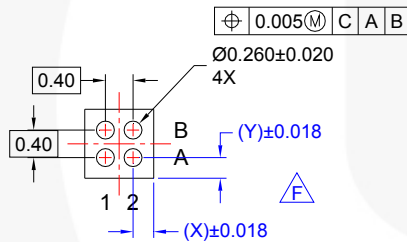
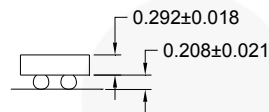
TOP VIEW



RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)



SIDE VIEWS



BOTTOM VIEW

NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. PACKAGE NOMINAL HEIGHT IS 500 MICRONS ±39 MICRONS (461-539 MICRONS).
- F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
- G. DRAWING FILNAME: MKT-UC004AFrev1.

Figure 24. 4-Bump, 0.76 x 0.76 mm, Wafer-Level Chip-Scale Packaging

Product-Specific Dimensions

Product	D	E	X	Y
FPF1203UCX	760 μm ± 30 μm	760 μm ± 30 μm	0.180 mm ± 0.018 μm	0.180 mm ± 0.018 μm
FPF1204UCX	760 μm ± 30 μm	760 μm ± 30 μm	0.180 mm ± 0.018 μm	0.180 mm ± 0.018 μm
FPF1204BUCX	760 μm ± 30 μm	760 μm ± 30 μm	0.180 mm ± 0.018 μm	0.180 mm ± 0.018 μm
FPF12045UCX	760 μm ± 30 μm	760 μm ± 30 μm	0.180 mm ± 0.018 μm	0.180 mm ± 0.018 μm
FPF1203LUCX	760 μm ± 30 μm	760 μm ± 30 μm	0.180 mm ± 0.018 μm	0.180 mm ± 0.018 μm

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.



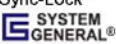
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