

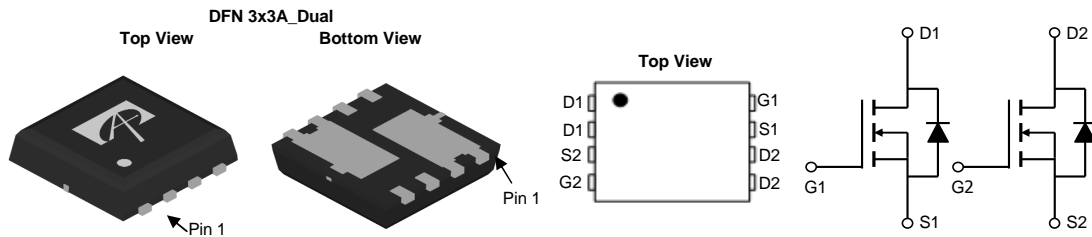
**General Description**

The AON7826 is designed to provide a high efficiency synchronous buck power stage with optimal layout and board space utilization. It includes two low  $R_{DS(ON)}$  MOSFETs in a dual DFN3x3 package. The AON7826 is well suited for use in compact DC/DC converter applications.

**Product Summary**

$V_{DS}$	20V
$I_D$ (at $V_{GS}=10V$ )	22A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 23m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=4.5V$ )	< 26m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=2.5V$ )	< 34m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=1.8V$ )	< 52m $\Omega$

100% UIS Tested  
100%  $R_g$  Tested



**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	22
		$T_C=100^\circ\text{C}$	14
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	50	A
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ\text{C}$	9
		$T_A=70^\circ\text{C}$	7
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	8	A
Avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AS}, E_{AR}$	3	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	16.7
		$T_C=100^\circ\text{C}$	6.7
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	30	40	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Ambient <sup>A D</sup>		Steady-State	60	75
Maximum Junction-to-Case	$R_{\theta JC}$	6.2	7.5	$^\circ\text{C}/\text{W}$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	20			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V			100	±nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	0.4	0.75	1.1	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	50			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =9A T <sub>J</sub> =125°C		19 25.5	23 32	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =7A		21	26	
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =6A		26	34	
		V <sub>GS</sub> =1.8V, I <sub>D</sub> =2A		34	52	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =9A		20		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				15	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =10V, f=1MHz	420	525	630	pF
C <sub>oss</sub>	Output Capacitance		65	95	125	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		45	75	105	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.8	1.7	2.6	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =10V, I <sub>D</sub> =9A	10	12.5	15	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge		4.5	6	7.5	nC
Q <sub>gs</sub>	Gate Source Charge			1		nC
Q <sub>gd</sub>	Gate Drain Charge			2		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =10V, R <sub>L</sub> =1.1Ω, R <sub>GEN</sub> =3Ω		3		ns
t <sub>r</sub>	Turn-On Rise Time			7.5		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			20		ns
t <sub>f</sub>	Turn-Off Fall Time			6		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =9A, dI/dt=500A/μs		14		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =9A, dI/dt=500A/μs		6		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> t ≤ 10s value and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

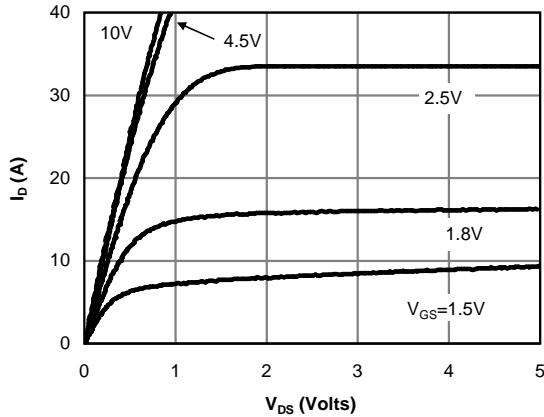
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

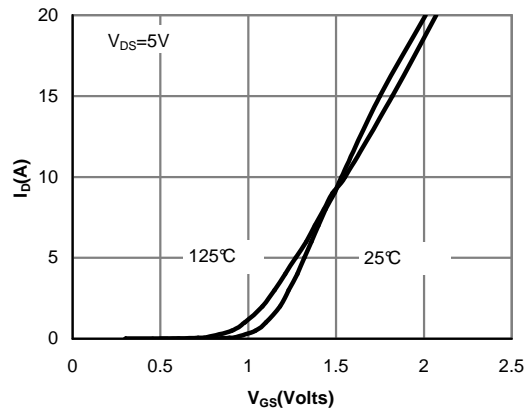
H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

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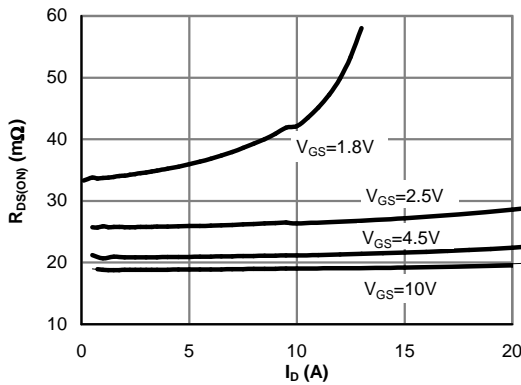
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



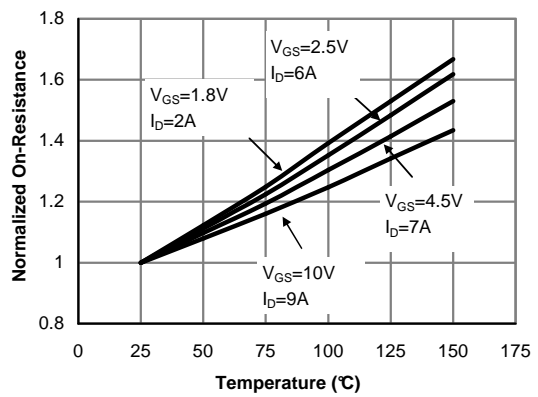
**Figure 1: On-Region Characteristics (Note E)**



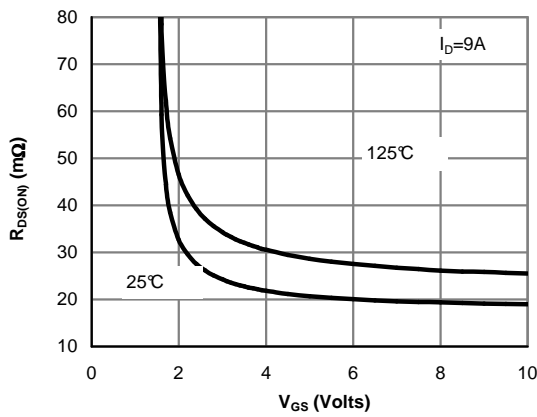
**Figure 2: Transfer Characteristics (Note E)**



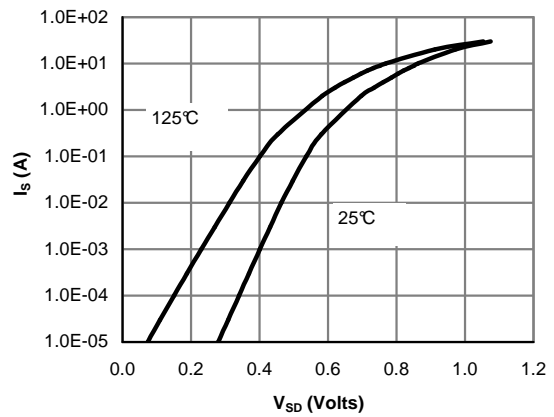
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

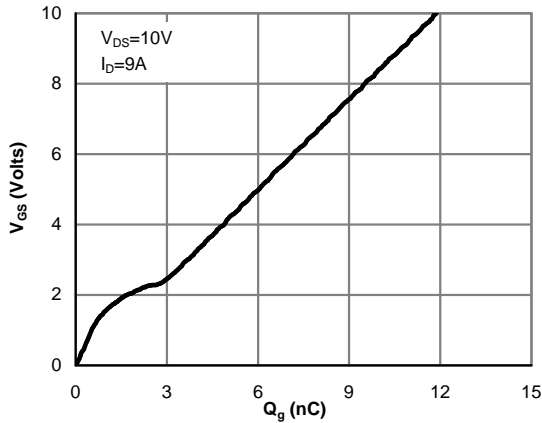


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

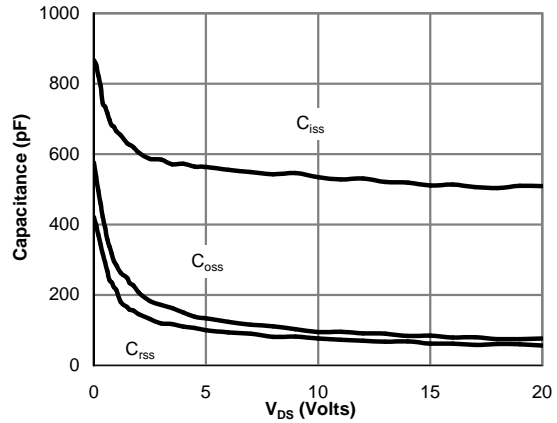


**Figure 6: Body-Diode Characteristics (Note E)**

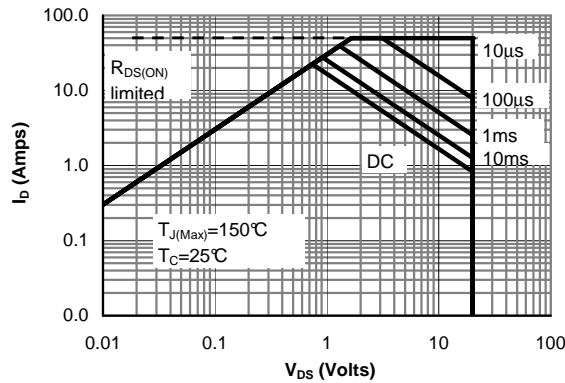
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



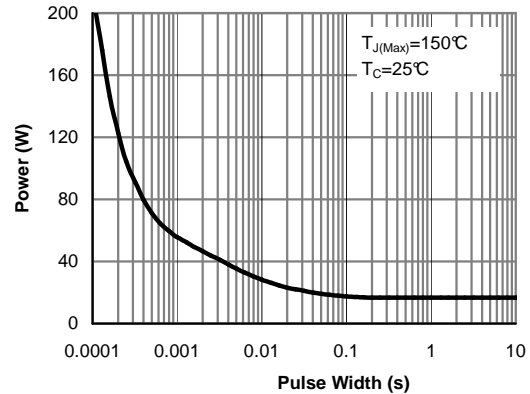
**Figure 7: Gate-Charge Characteristics**



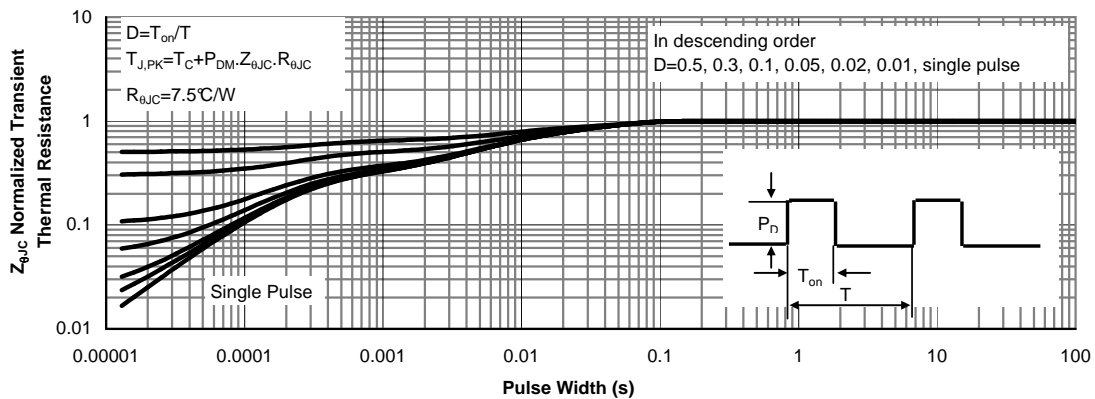
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

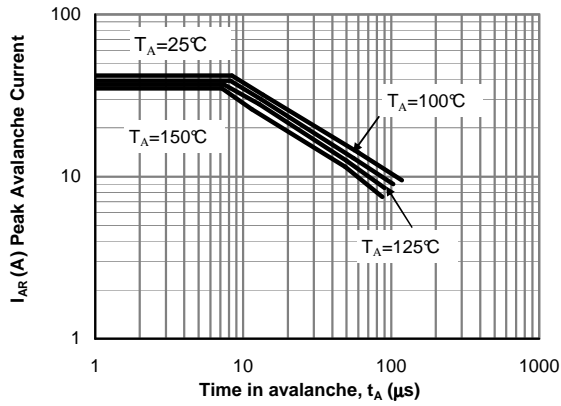


**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**

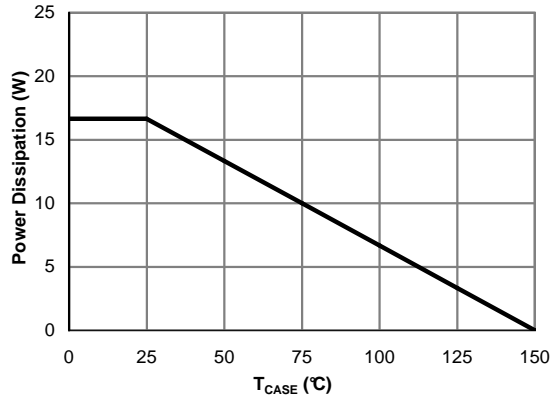


**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

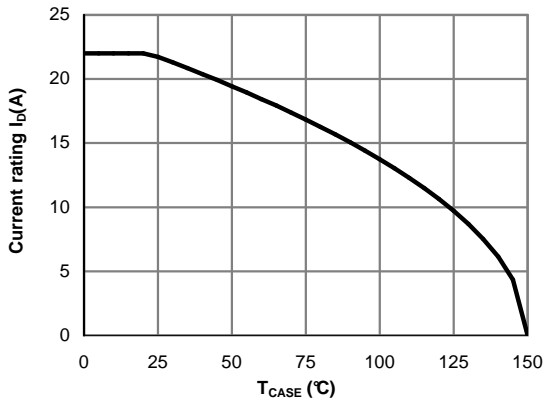
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



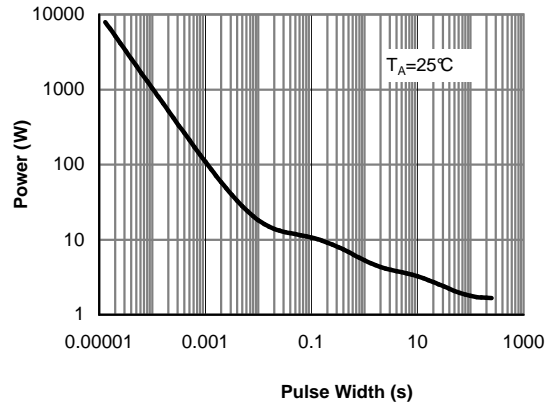
**Figure 12: Single Pulse Avalanche capability (Note C)**



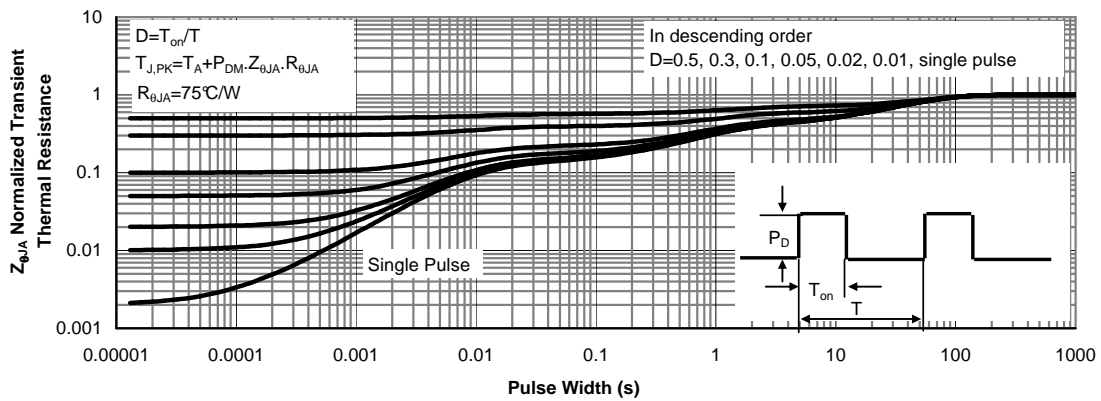
**Figure 13: Power De-rating (Note F)**



**Figure 14: Current De-rating (Note F)**

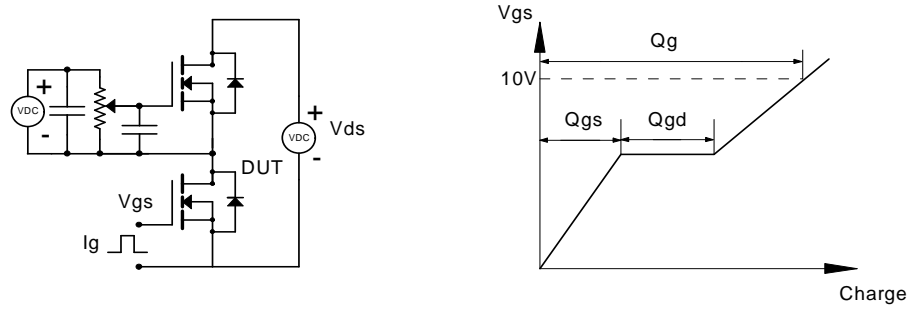


**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**

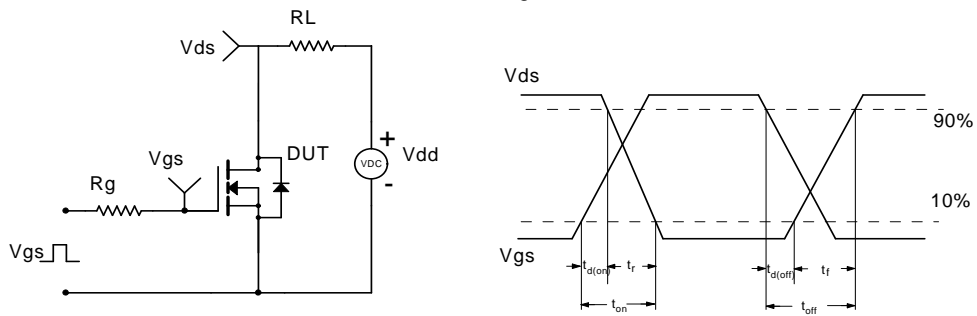


**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

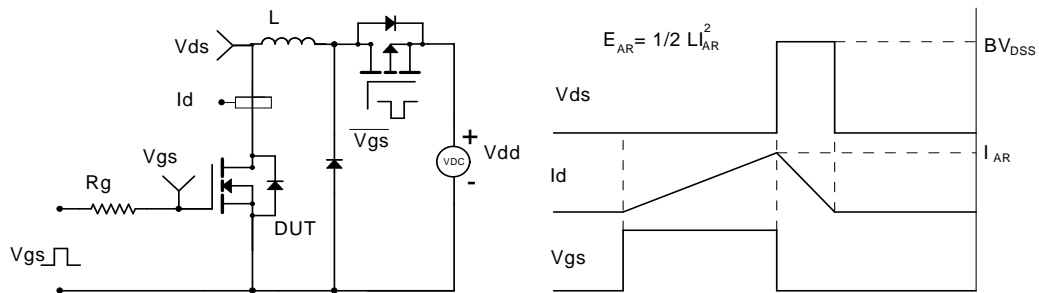
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

