

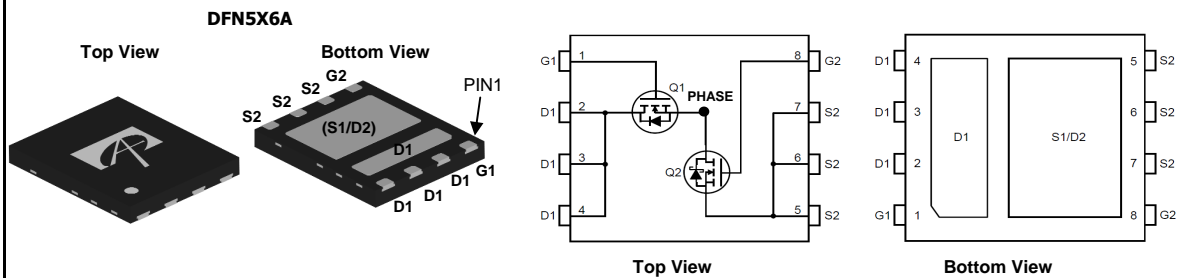
### General Description

The AON6924 is designed to provide a high efficiency synchronous buck power stage with optimal layout and board space utilization. It includes two specialized MOSFETs in a dual Power DFN5x6A package. The Q1 "High Side" MOSFET and the Q2 "Low Side" MOSFET with integrated Schottky have been designed for optimal power efficiency. The AON6924 is well suited for use in compact DC/DC converter applications.

### Product Summary

	Q1	Q2
$V_{DS}$	30V	30V
$I_D$ (at $V_{GS}=10V$ )	60A	85A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	<5.2m $\Omega$	<1.6m $\Omega$
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$ )	<7.8m $\Omega$	<1.9m $\Omega$

100% UIS Tested  
 100% Rg Tested



### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Max Q1	Max Q2	Units	
Drain-Source Voltage	$V_{DS}$	30		V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 12$	V	
Continuous Drain Current	$I_D$	$T_C=25^\circ C$	60	85	A
		$T_C=100^\circ C$	38		
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	200	510		
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ C$	15	28	A
		$T_A=70^\circ C$	12		
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	40	68	A	
Avalanche Energy $L=0.1mH$ <sup>C</sup>	$E_{AS}, E_{AR}$	80	231	mJ	
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ C$	31	104	W
		$T_C=100^\circ C$	12.5		
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ C$	2	2.2	W
		$T_A=70^\circ C$	1.3		
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150		$^\circ C$	

### Thermal Characteristics

Parameter	Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	25	20	30	25	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	50	45	60	55
Maximum Junction-to-Case	$R_{\theta JC}$	3.1	0.9	4	1.2	$^\circ C/W$

**Q1 Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.7	2.3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	200			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		4.3	5.2	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		6.2	7.8	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		70		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				30	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz	1040	1300	1560	pF
C <sub>oss</sub>	Output Capacitance		370	530	690	pF
C <sub>riss</sub>	Reverse Transfer Capacitance		10	35	60	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.8	1.7	2.6	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A	13	17	21.0	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge				7.2	nC
Q <sub>gs</sub>	Gate Source Charge				3.9	nC
Q <sub>gd</sub>	Gate Drain Charge				1.8	nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		5		ns
t <sub>r</sub>	Turn-On Rise Time			16		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			20		ns
t <sub>f</sub>	Turn-Off Fall Time			4		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs	16	21	26	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs	31	39	47	nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

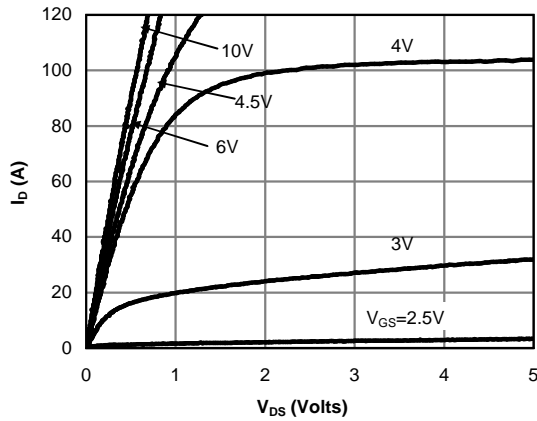
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating g.

G. The maximum current rating is package limited.

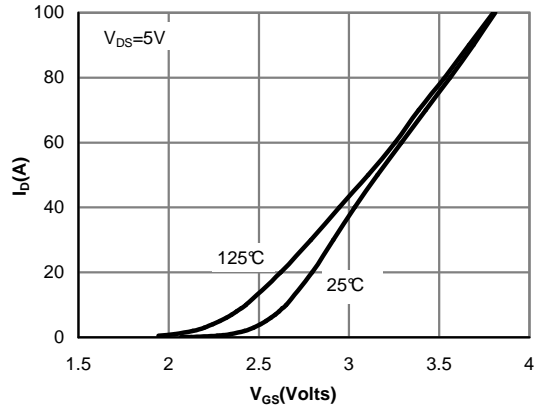
H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

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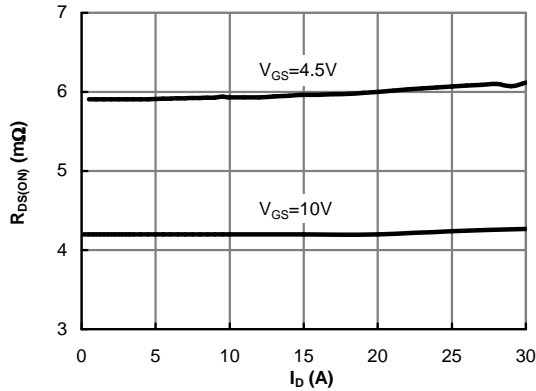
**Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



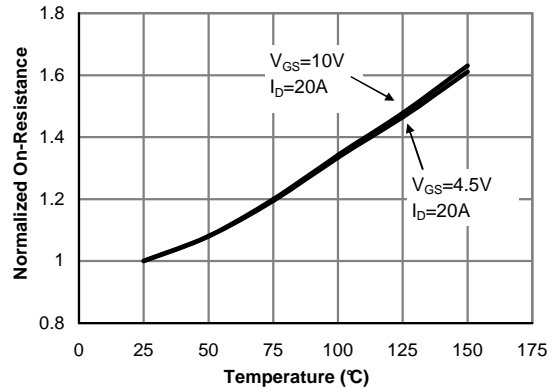
**Fig 1: On-Region Characteristics (Note E)**



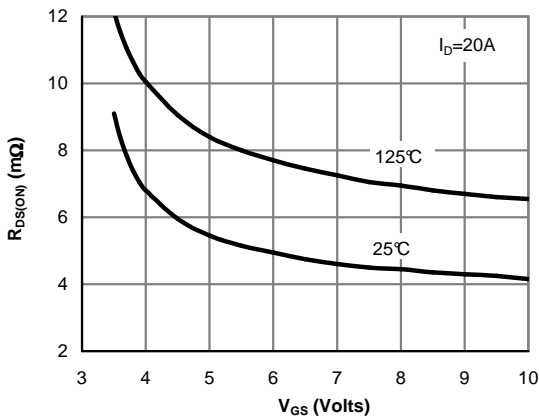
**Figure 2: Transfer Characteristics (Note E)**



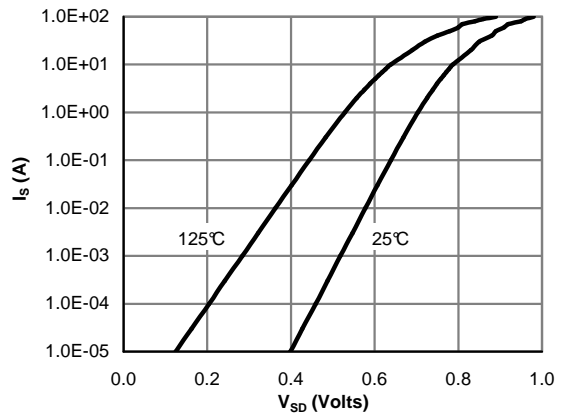
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**



**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**



**Figure 6: Body-Diode Characteristics (Note E)**

**Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

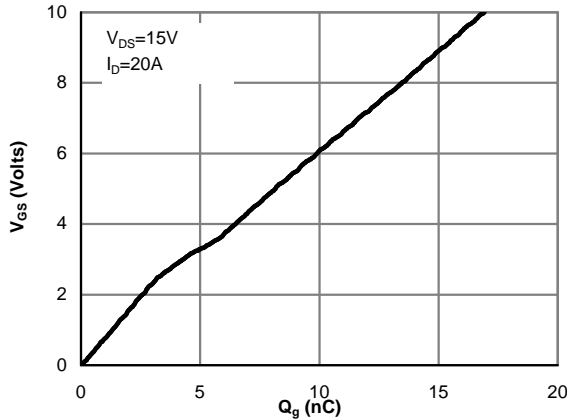


Figure 7: Gate-Charge Characteristics

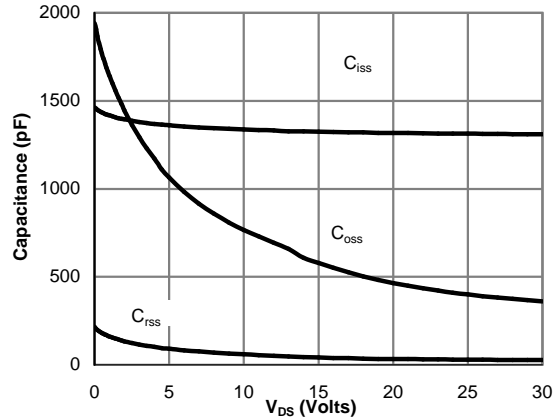


Figure 8: Capacitance Characteristics

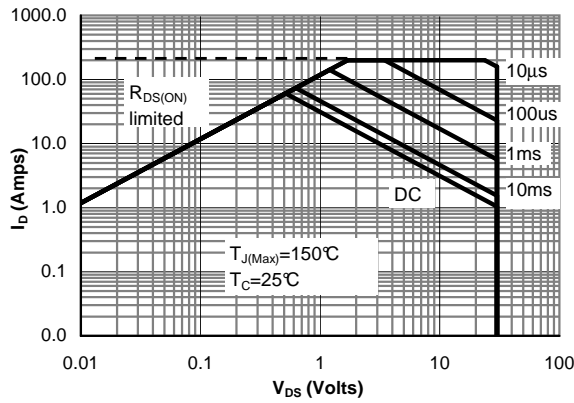


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

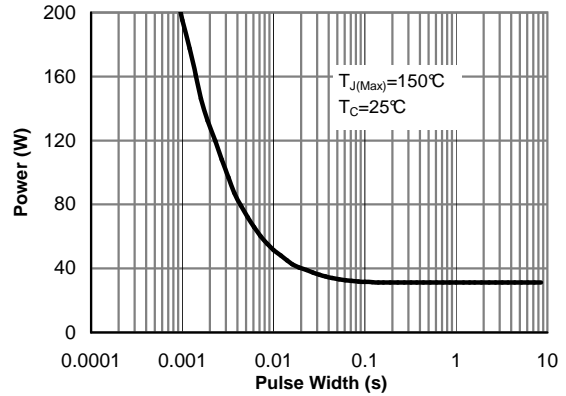


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

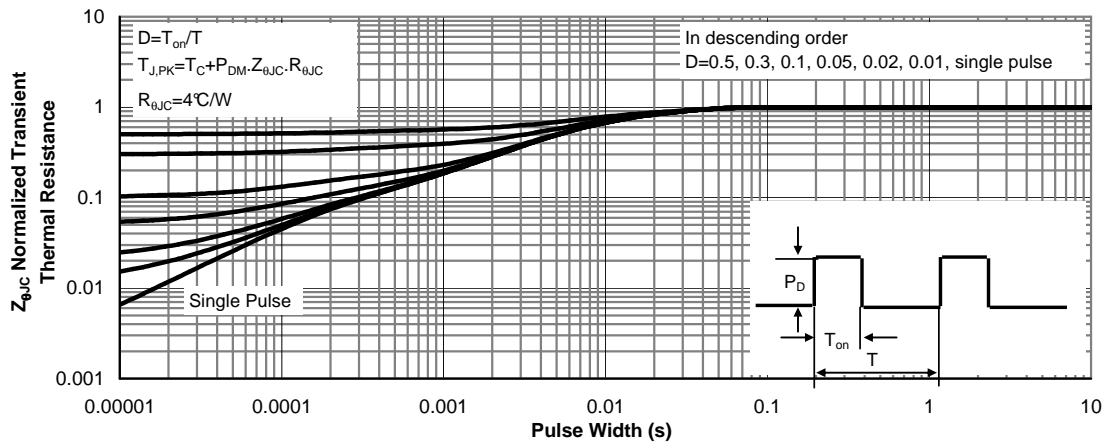
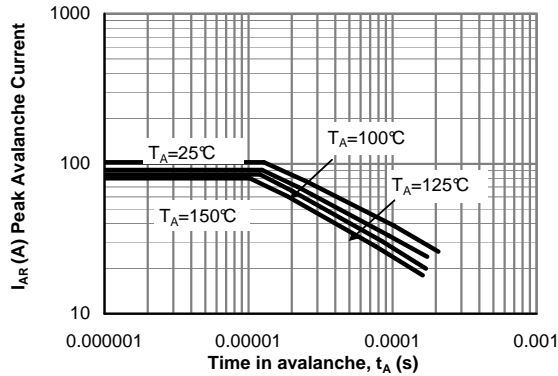
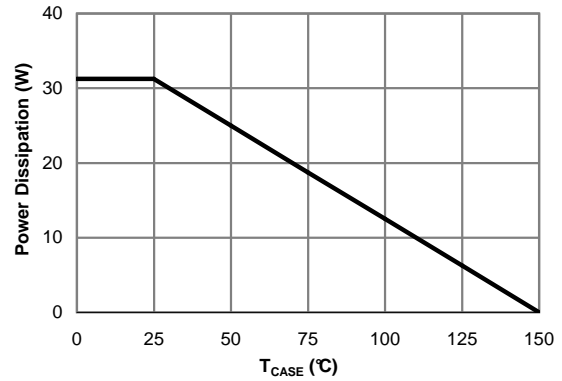


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

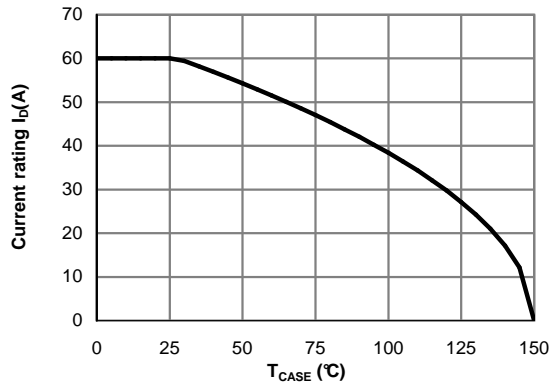
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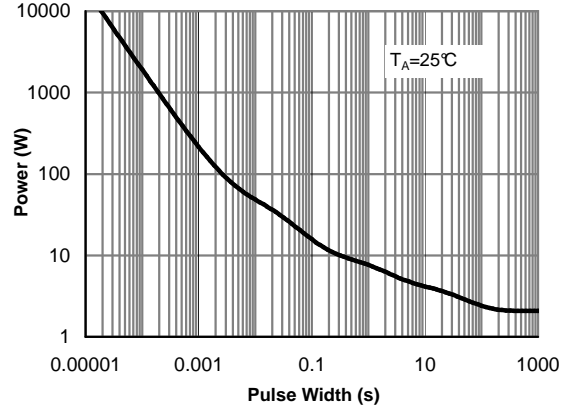
**Figure 12: Single Pulse Avalanche capability (Note C)**



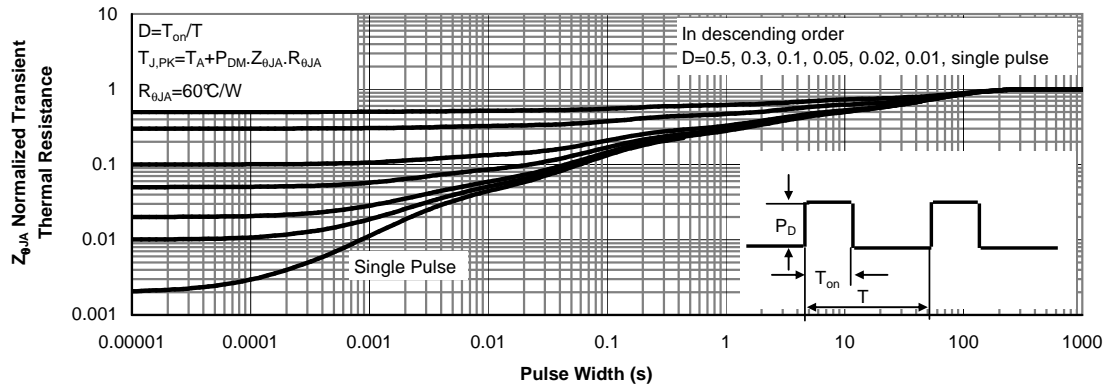
**Figure 13: Power De-rating (Note F)**



**Figure 14: Current De-rating (Note F)**



**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)**



**Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)**

**Q2 Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =10mA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			0.5 100	mA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±12V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.5	2.1	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	510			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		1.2	1.6	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		1.5	1.9	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		180		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.36		V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>6</sup>				85	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz	6550	8190	9830	pF
C <sub>oss</sub>	Output Capacitance		630	900	1170	pF
C <sub>riss</sub>	Reverse Transfer Capacitance		400	670	950	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.3	0.65	1.0	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A	110	140	170	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge		48	60	72	nC
Q <sub>gs</sub>	Gate Source Charge			17		nC
Q <sub>gd</sub>	Gate Drain Charge			20		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		15		ns
t <sub>r</sub>	Turn-On Rise Time			17		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			103		ns
t <sub>f</sub>	Turn-Off Fall Time			18		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs	12.5	16	20	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs	27	34	41	nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal impedance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

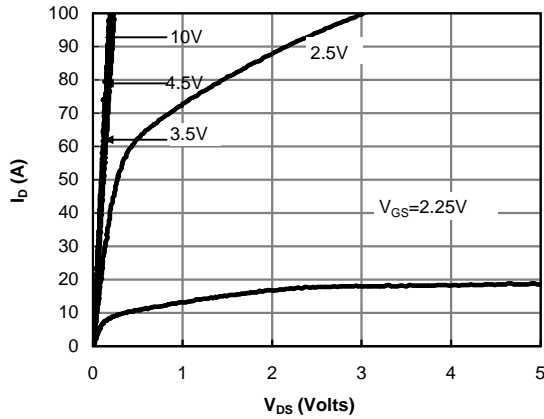
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

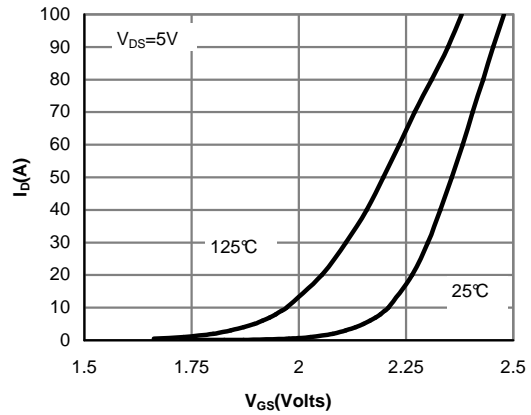
G. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

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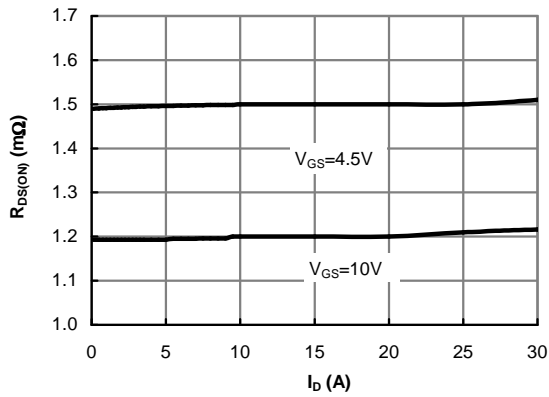
**Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



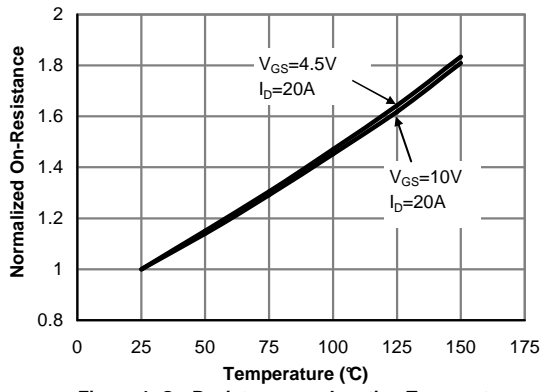
**Fig 1: On-Region Characteristics (Note E)**



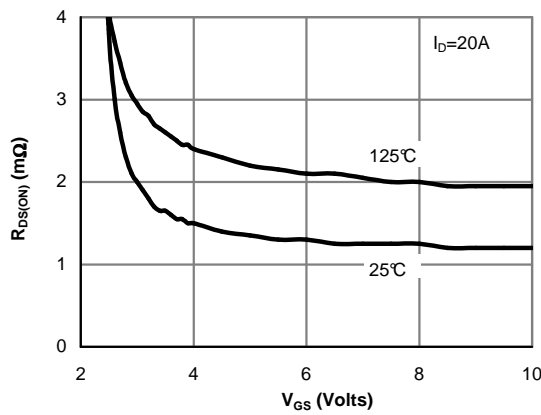
**Figure 2: Transfer Characteristics (Note E)**



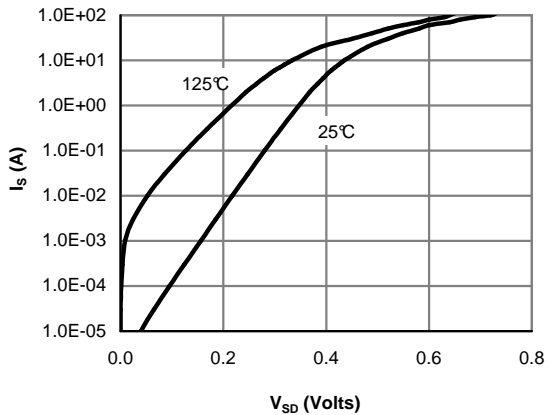
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

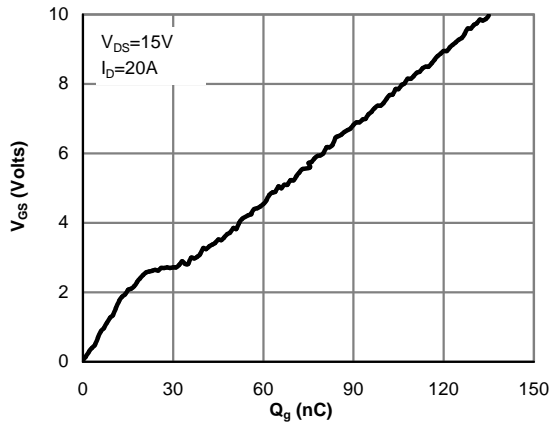


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

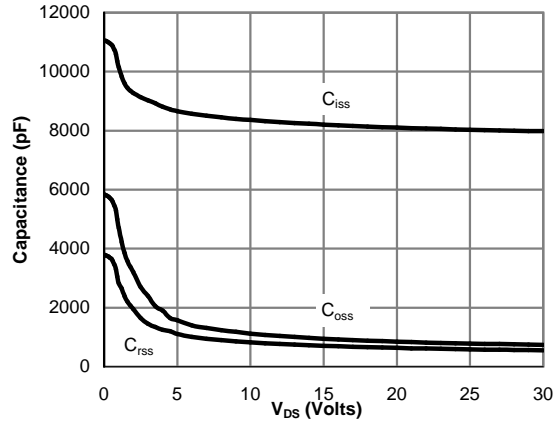


**Figure 6: Body-Diode Characteristics (Note E)**

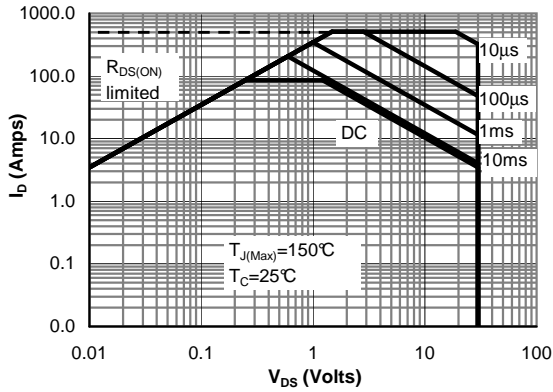
**Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



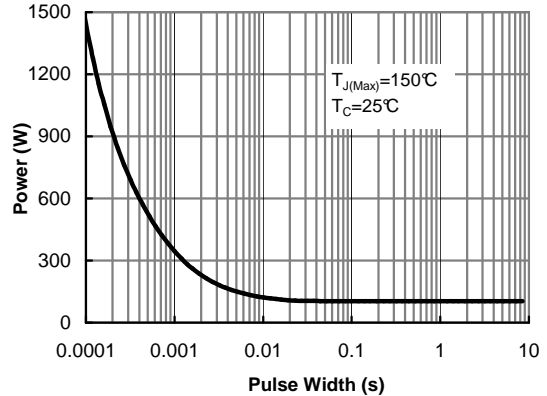
**Figure 7: Gate-Charge Characteristics**



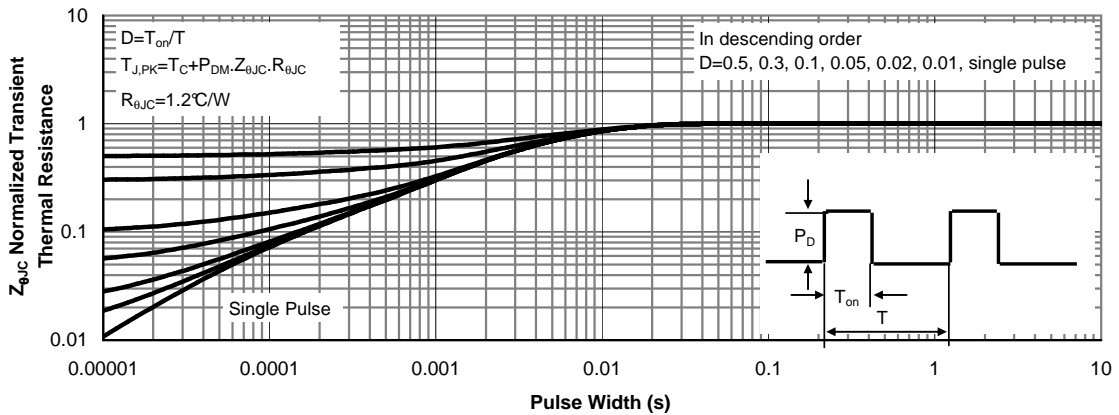
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



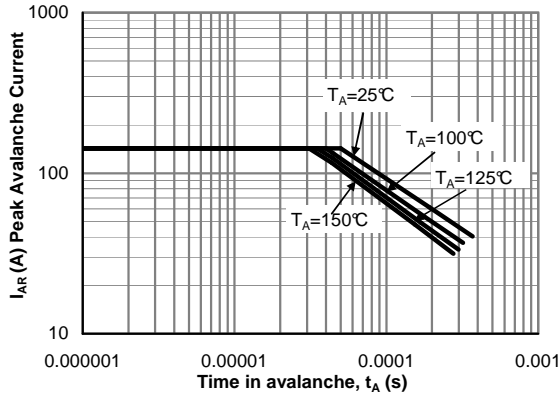
**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



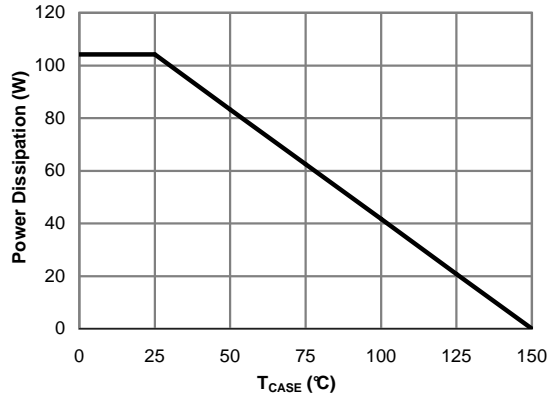
**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**



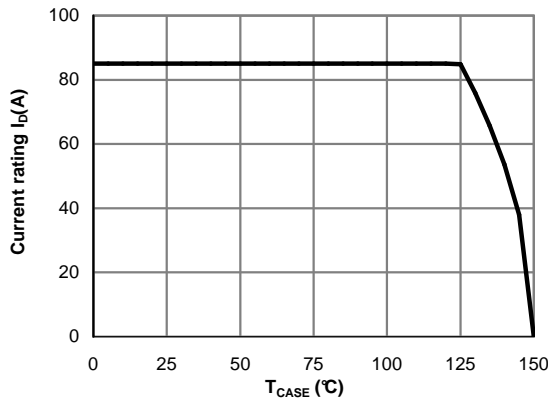
**Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



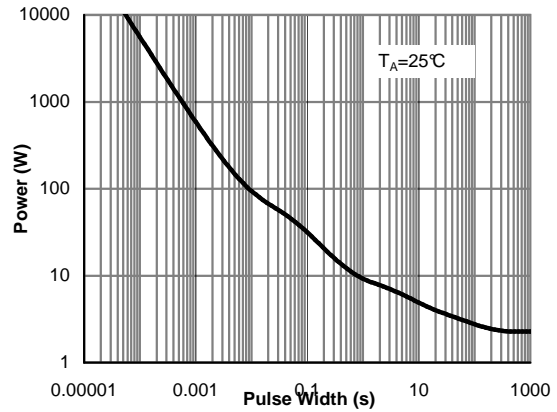
**Figure 12: Single Pulse Avalanche capability (Note C)**



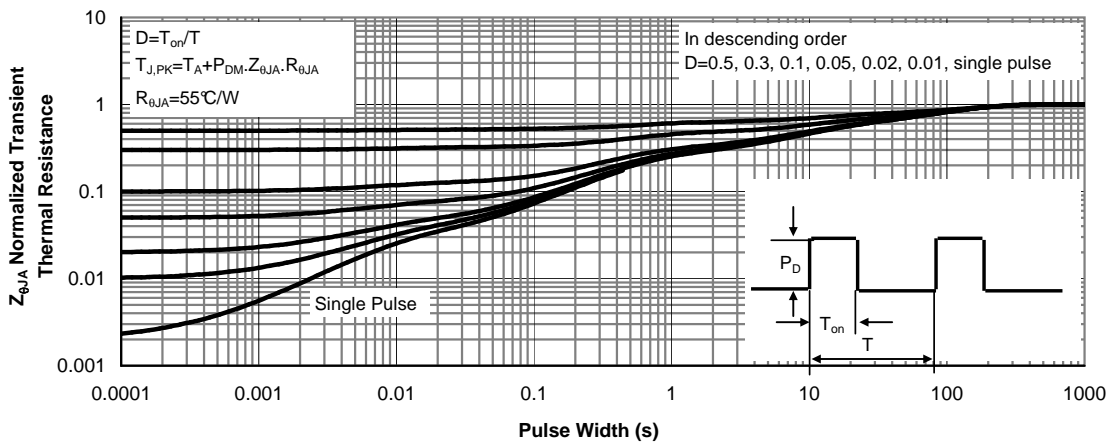
**Figure 13: Power De-rating (Note F)**



**Figure 14: Current De-rating (Note F)**

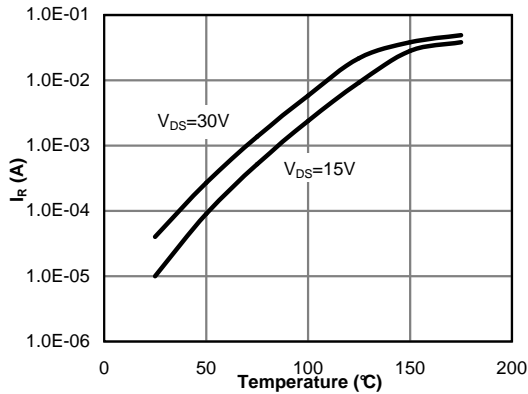


**Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)**

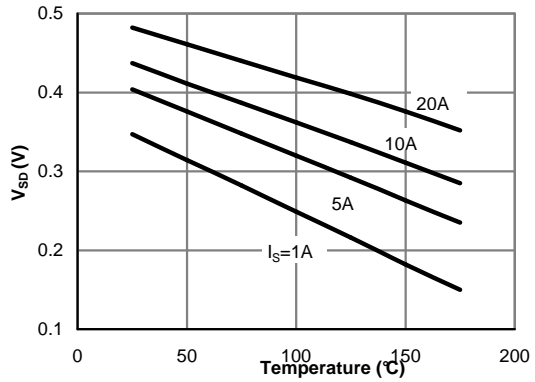


**Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)**

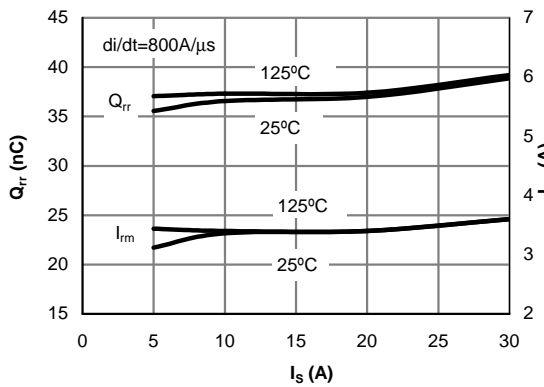
**Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



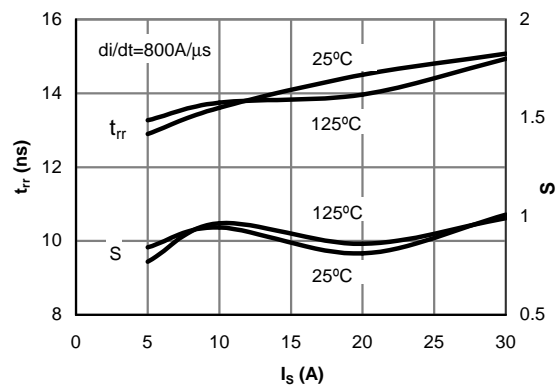
**Figure 17: Diode Reverse Leakage Current vs. Junction Temperature**



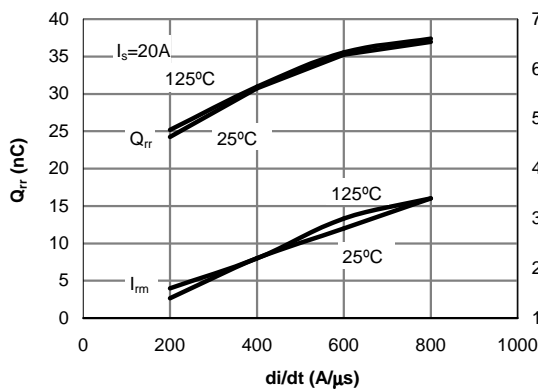
**Figure 18: Diode Forward voltage vs. Junction Temperature**



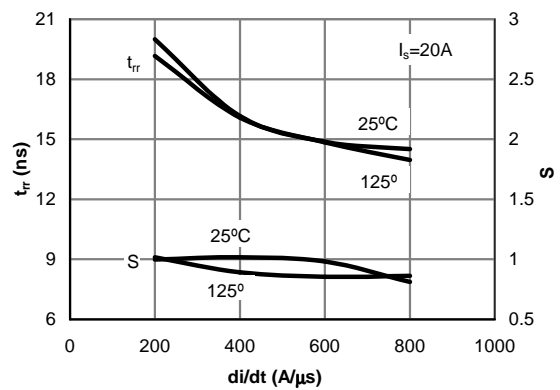
**Figure 19: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current**



**Figure 20: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current**

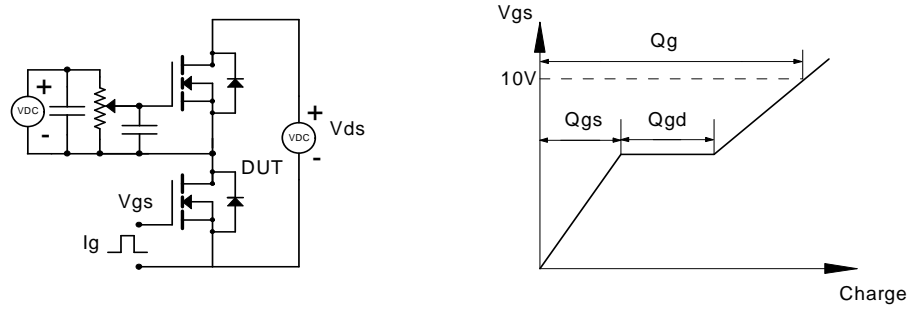


**Figure 21: Diode Reverse Recovery Charge and Peak Current vs. di/dt**

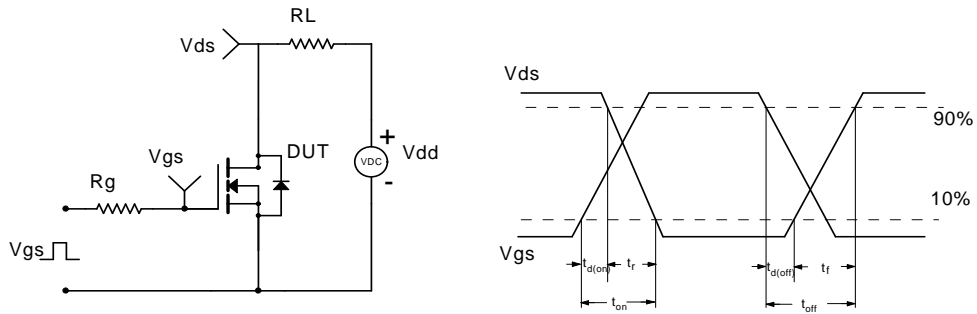


**Figure 22: Diode Reverse Recovery Time and Softness Factor vs. di/dt**

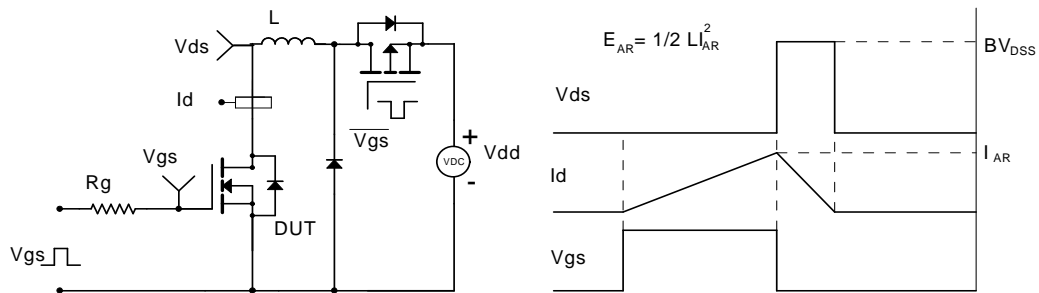
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**

