PI74FCT162Q374T

Fast Low Noise CMOS 16-Bit Registers (3-State)

Product Features

- V_{CC} = 5V ±10%
- Balanced output drivers: ±12 mA
- Output impedance: 35Ω (typical)
- Typical V_{OLP} (Output Ground Bounce) < 0.5V at V_{CC} = 5V, TA = 25°C
- Bus Hold retains last active bus state during tri-state
- Hysteresis on all inputs
- Packages available:
  - 48-pin 240 mil wide plastic TSSOP (A)
  - 48-pin 300 mil wide plastic SSOP (V)
  - 48-pin 150 mil wide plastic BQSOP (B)
- Device models available on request

Product Description

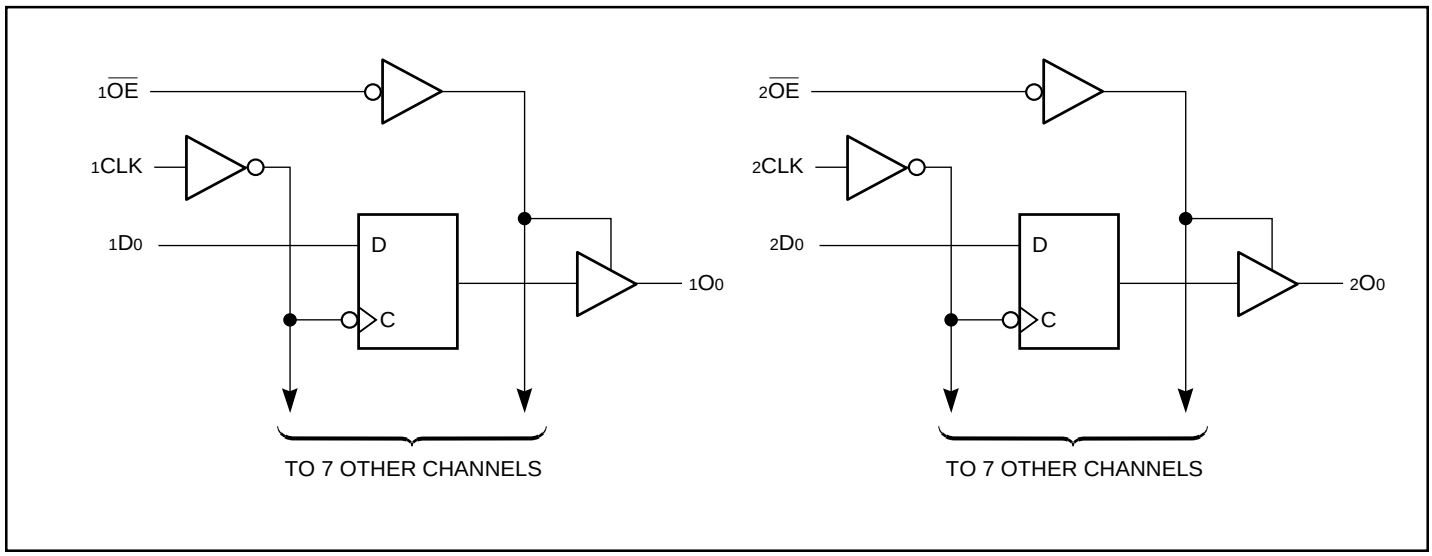
Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT162Q374T is a 16-bit octal register designed with 16 D-type flip-flops with a buffered common clock and 3-state outputs. The Output Enable ($x\overline{OE}$) and clock (xCLK) controls are organized to operate as two 8-bit registers or one 16-bit register. When $\overline{OE}$ is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the xOx outputs on the LOW-to-HIGH transition of the clock input.

The PI74FCT162Q374T is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This device features a typical output impedance of 35Ω eliminating the need for external terminating resistors for most bus interface applications. This noise suppression benefit is designated by the letter "Q" (for quiet) in the part number.

The PI74FCT162Q374T has "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors.

Logic Block Diagram



Product Pin Description

Pin Name	Description
x$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
xCLK	Clock Inputs
xDx	Inputs[1]
xOx	3-State Outputs
GND	Ground
VCC	Power

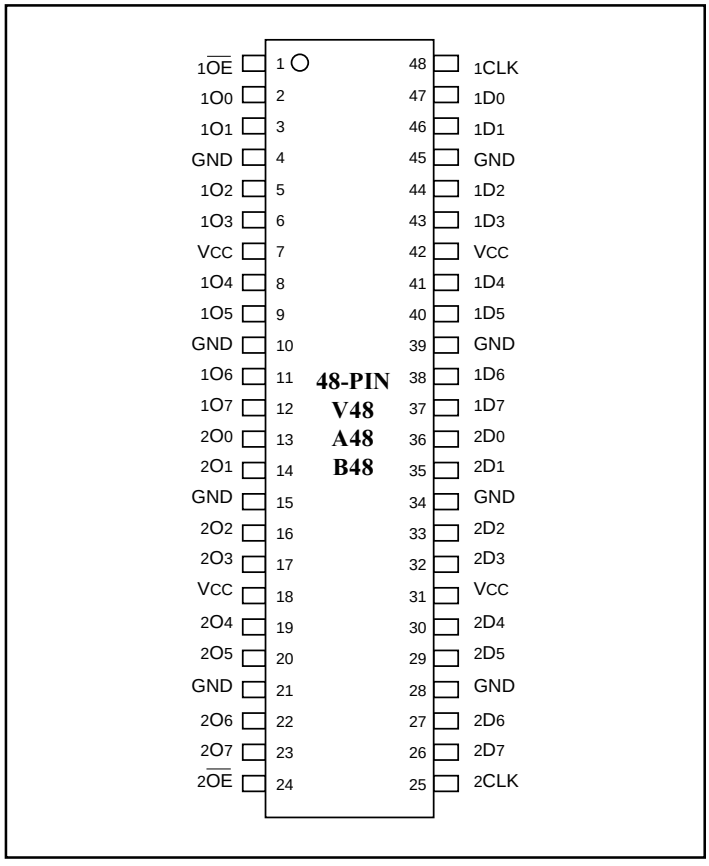
Note: 1. For the PI74FCT162Q374T, these pins have "Bus Hold". All other pins are standard, outputs, or I/Os.

Truth Table[1]

	Inputs			Outputs
Function	**xDx**	**xCLK**	**x$\overline{OE}$**	**xOx**
High-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

Note:
1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH transition

Product Pin Configuration



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	Standard Input[4], V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IH}	Input HIGH Current	Bus Hold Input[5], V_{CC} = Max.	V_{IN} = V_{CC}			±100	µA
I_{IL}	Input LOW Current	Standard Input[4], V_{CC} = Min.	V_{IN} = GND			–1	µA
I_{IL}	Input LOW Current	Bus Hold Input[5], V_{CC} = Min.	V_{IN} = GND			±100	µA
I_{BHH}	Bus Hold	Bus Hold Input[5], V_{CC} = Min.	V_{IN} = 2.0V	–50			µA
I_{BHL}	Sustain Current		V_{IN} = 0.8V	+50			
I_{OZH}	High Impedance	V_{CC} = Max.	V_{OUT} = 2.7V			1	µA
I_{OZL}	Output Current	V_{CC} = Max.	V_{OUT} = 0.5V			–1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_O	Output Drive Current	V_{CC} = Max.[3], V_{OUT} = 2.5V		–50		–180	mA
V_H	Input Hysteresis				100		mV

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is ± 5 µA at T_A = –55°C.
5. Pins with Bus Hold are identified in the pin description.
6. This specification does not apply to bi-directional functionalities with Bus Hold.

Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]	Min.	Typ[2]	Max.	Units
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} OR V_{IL}, V_{OUT} = 1.5V[3]	36	—	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} OR V_{IL}, V_{OUT} = 1.5V[3]	–100	–166	–200	mA

Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12.0 mA	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA	—	0.3	0.55	V

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]		0.5	1.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open x$\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10 MHz 50% Duty Cycle x$\overline{OE}$ = GND f_i = 5 MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND		0.6	1.5[5]	mA
			V_{IN} = 3.4V V_{IN} = GND		1.1	3.0[5]	
		V_{CC} = Max., Outputs Open fcp = 10 MHz 50% Duty Cycle x$\overline{OE}$ = GND 16 Bits Toggling f_i = 2.5 MHz 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND		3.0	5.5[5]	
			V_{IN} = 3.4V V_{IN} = GND		7.5	19.0[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_I = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics over Operating Range

Parameters	Description	Conditions	162Q374T		162Q374AT		162Q374CT		162Q374DT		162Q374ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay xCLK to xOx	C_L = 50pF R1 = 500	2.0	10	2.0	6.5	2.0	5.2	2.0	4.2	1.5	3.7	ns
t_{PZH} t_{PZL}	Output Enable Time $x\overline{OE}$ to xOx		1.5	12.5	1.5	6.5	1.5	5.5	1.5	4.8	1.5	4.4	
t_{PHZ} t_{PLZ}	Output Disable Time $x\overline{OE}$ to xOx		1.5	8.0	1.5	5.5	1.5	5.0	1.5	4.0	1.5	4.0	
t_{SU}	Setup time HIGH or LOW, xDx to xCLK		2.0	-	2.0	-	2.0	-	2.0	-	1.5	-	
t_H	Hold time HIGH or LOW, xDx to xCLK		1.5	-	1.5	-	1.5	-	1.0	-	0.0	-	
t_W	CLK Pulse Width HIGH[3]		7.0	-	5.0	-	5.0	-	3.0	-	3.0	-	
$t_{SK(O)}$	Outout Skew[4]		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.