

CMOS MICROCONTROLLER FOR TELEPHONE SETS

GENERAL DESCRIPTION

The PCD3315 is a single-chip 8-bit microcontroller fabricated in CMOS and is a member of the PCD33XX family. It has special on-chip features for application in telephone sets. For further detailed information, see PCD33XX family specification.

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 1536 ROM bytes
- 160 RAM bytes
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input (CE/ $\overline{T0}$)
- Single-level vectored interrupts: external, timer/event counter
- 8-bit programmable timer/event counter
- Over 80 instructions (based on MAB8048)
- All instructions 1 or 2 cycles
- Clock frequency 100 kHz to 10 MHz
- Single supply voltage from 1,8 V to 6 V
- Low standby voltage and current
- STOP and IDLE mode
- On-chip oscillator with output drive capability for peripherals
- Configuration of all I/O port lines individually selected by mask: pull-up, open drain or push-pull
- Power-on-reset circuit and low supply voltage detection
- Reset state of all ports individually selected by mask
- Operating temperature range: -25 to $+70$ °C

PACKAGE OUTLINES

PCD3315P: 28-lead DIL; plastic (SOT117).

PCD3315T: 28-lead mini-pack; plastic (SO28; SOT136A).

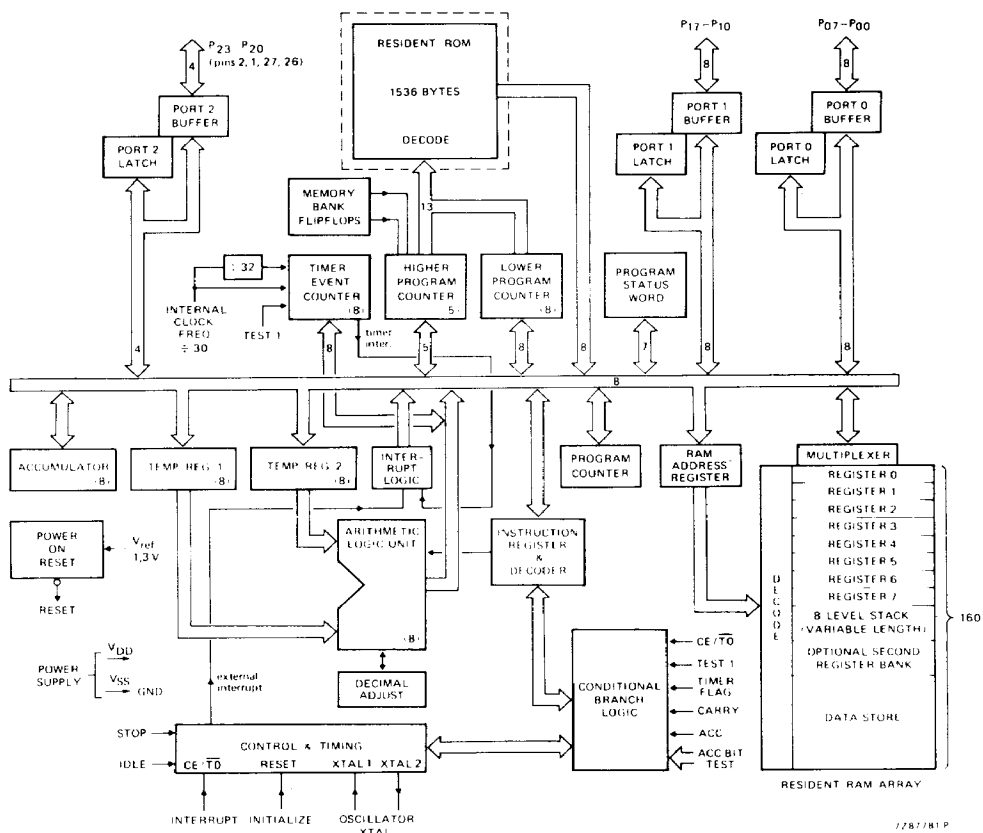


Fig. 1 Block diagram; PCD3315.

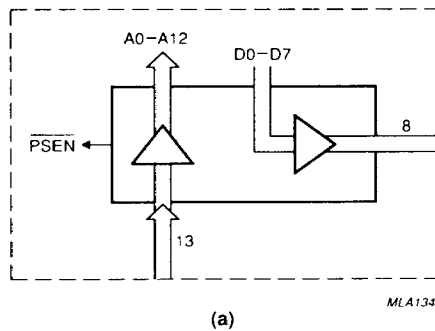


Fig. 1a Replacement of dotted part in Fig. 1, for the PCD3301B 'Piggy-back' version.

PINNING

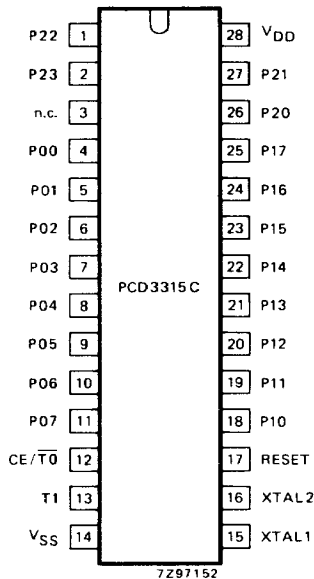


Fig. 2 Pinning diagram: PCD3315.

DEVELOPMENT DATA

PIN DESIGNATION

3	n.c.	not connected
4-11	P00-P07	Port 0: 8-bit quasi-bidirectional I/O port.
12	CE/ $\overline{T0}$	Interrupt/Test 0: external interrupt input (sensitive to positive-going edge)/test input pin; when used as a test input directly tested by conditional branch instructions JT0 and JNT0.
13	T1	Test 1: test input pin, directly tested by conditional branch instructions JT1 and JNT1. T1 also functions as an input to the 8-bit timer/event counter, using the STRT CNT instruction.
14	VSS	Ground: circuit earth potential.
15	XTAL 1	Crystal input: connection to timing component (crystal) which determines the frequency of the internal oscillator; also the input for an external clock source.
16	XTAL 2	connection to the other side of the timing component.
17	RESET	Reset input: used to initialize the processor (active HIGH), or output of power-on-reset circuit.
18-25	P10-P17	Port 1: 8-bit quasi-bidirectional I/O port.
26, 27, 1, 2	P20-P23	Port 2: 4-bit quasi-bidirectional I/O port.
28	VDD	Power supply: 1,8 V to 6 V.

D.C. CHARACTERISTICS

$V_{DD} = 2,5$ to 6 V; $V_{SS} = 0$ V; $T_{amb} = -25$ to $+70$ °C; all voltages with respect to V_{SS} ; $f = 3,58$ MHz with $R_S = 50$ Ω ; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage operating	V_{DD}	1,8	—	6	V
STOP mode for RAM retention	V_{DD}	1,0	—	6	V
Supply current operating at $V_{DD} = 3$ V	I_{DD}	—	350	—	μ A
IDLE mode at $V_{DD} = 3$ V	I_{DD}	—	150	—	μ A
STOP mode (note 1) at $V_{DD} = 1,8$ V; $T_{amb} = 25$ °C	I_{DD}	—	1,2	2,5	μ A
at $V_{DD} = 1,8$ V; $T_{amb} = 55$ °C	I_{DD}	—	—	5	μ A
at $V_{DD} = 1,8$ V; $T_{amb} = 70$ °C	I_{DD}	—	—	10	μ A
RESET I/O					
Switching level	V_{RESET}	—	1,2	—	V
Sink current at $V_{DD} > V_{RESET}$	I_{OL}	—	7	—	μ A
Inputs					
Input voltage LOW	V_{IL}	0	—	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	—	V_{DD}	V
Input leakage current at $V_{SS} < V_I < V_{DD}$	$\pm I_{IL}$	—	—	1	μ A
Outputs					
Output voltage LOW at $V_I = V_{SS}$ or V_{DD} ; $ I_O < 1$ μ A	V_{OL}	—	—	0,05	V
Output sink current LOW at $V_{DD} = 3$ V; $V_O = 0,4$ V	I_{OL}	0,6	1,5	—	mA
Pull-up output source current HIGH at $V_{DD} = 3$ V; $V_O = 0,9V_{DD}$	$-I_{OH}$	10	—	—	μ A
at $V_{DD} = 3$ V; $V_O = V_{SS}$	$-I_{OH}$	—	—	200	μ A
Push-pull output source current HIGH at $V_{DD} = 3$ V; $V_O = V_{DD} - 0,4$ V	$-I_{OH}$	0,6	1,5	—	mA

Note 1

Crystal connected between XTAL 1 and XTAL 2; pin 2 pulled to V_{DD} via 5,6 k Ω resistor; CE and T1 at V_{SS} .