



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LV8094CT — Bi-CMOS IC Piezo Actuator Driver IC

Overview

The LV8094CT is a piezoelectric actuator driver IC. It internally generates drive waveforms and this makes it possible to control piezoelectric actuators with simple instructions.

Features

- Actuators using piezoelectric elements can be driven and controlled simply by I²C communication.
- The piezoelectric drive waveforms are set externally by serial input signals using the I²C interface.
The rising and falling timings are determined with clock count.
- ENIN input that controls the startup/stop of the IC.
- The time for which the actuator is driven is determined with the drive frequency setting based on I²C communication.
- Provides a busy signal output during periods when the actuator is being driven by OUT pin output so that applications can be aware of the actuator operating/stopped state.
- Built-in undervoltage protection circuits, and register power-on reset function.

Specifications

Absolute Maximum Ratings at Ta = 25°C, GND = 0V

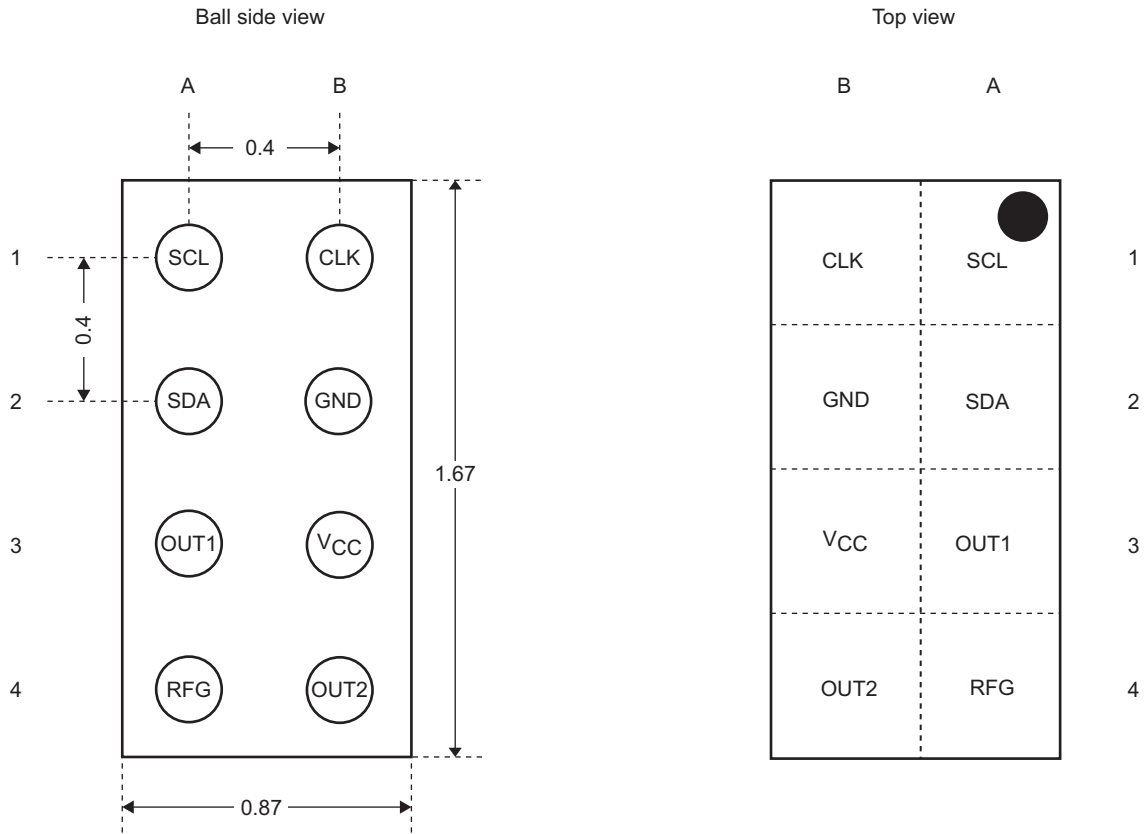
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC} max		-0.5 to 5.0	V
Output current	I _O max		300	mA
Peak output current	I _O peak1	t ≤ 1ms	750	mA
	I _O peak2	t ≤ 10μs	1200	mA
Input signal voltage	V _{IN} max		-0.5 to V _{CC} +0.5	V
Allowable power dissipation	P _d max	*Mounted on a specified board.	350	mW
Operating temperature	T _{opr}		-30 to +85	°C
Storage temperature	T _{stg}		-55 to +125	°C

* Specified board : 40mm×40mm×1.6mm, glass epoxy board.

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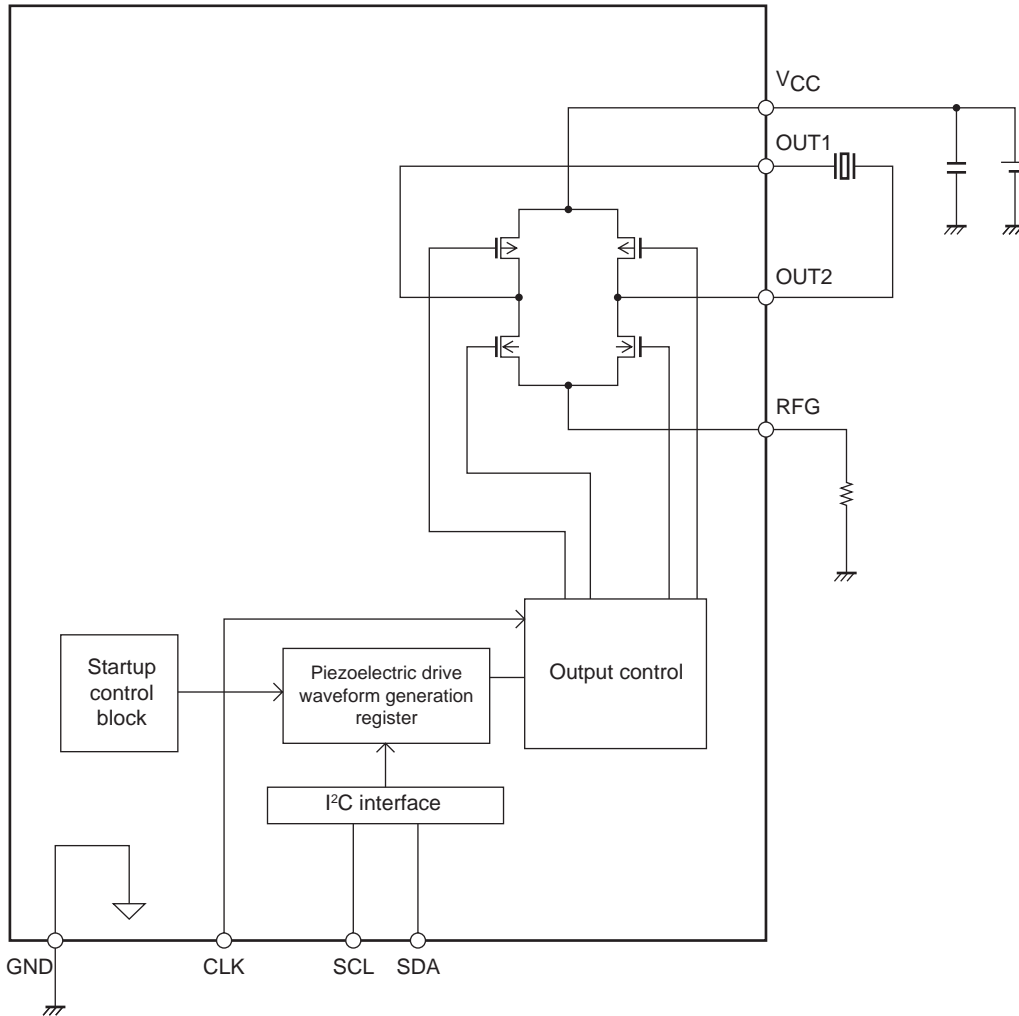
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Pin Assignment



- A1:SCL
- A2:SDA
- A3:OUT1
- A4:RFG
- B1:CLK
- B2:GND
- B3:VCC
- B4:OUT2

Block Diagram



Value of the resistor connected to the RFG pin

Inrush current flowing to the piezoelectric elements can be controlled in the LV8094CT by inserting a resistor between the RFG pin and GND potential.

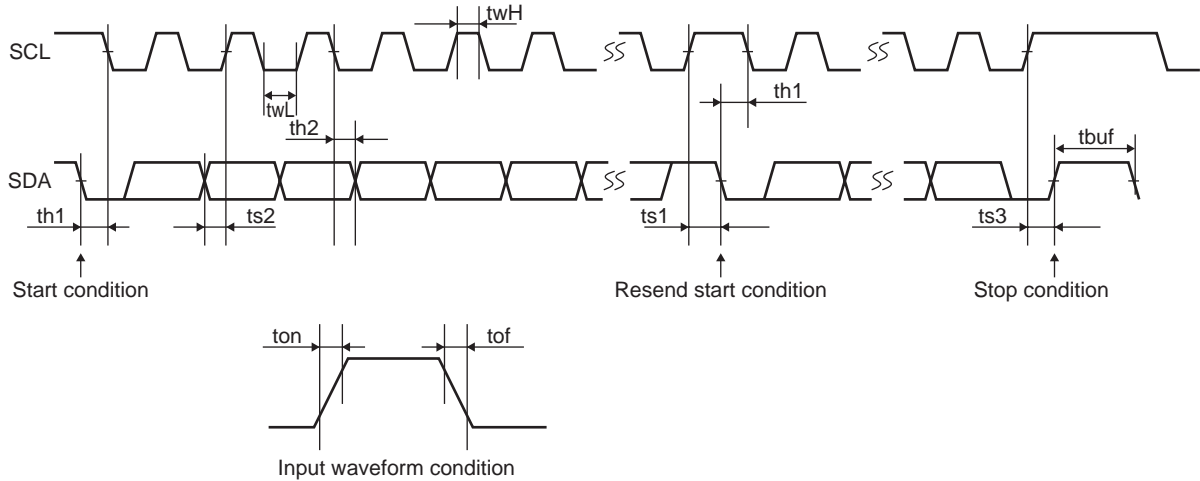
Since the resistance affects the actuator operation, the constant must be determined in a range from 0 to 3.3Ω while monitoring the operation of the actuator.

Capacitor on the VCC line

Piezoelectric actuators are capacitive loads in electrical terms, and they operate units by charging and discharging the charges. Since the charge between the capacitor on the VCC line and piezoelectric elements is transferred, the capacitor must be mounted near the VCC pin. The capacitance of the capacitor required is determined by the capacitance of the piezoelectric element. A capacitance within a range that does not affect operation must be selected.

Serial Bus Communication Specifications

I²C serial transfer timing conditions



Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	f _{scl}	SCL clock frequency	0		100	kHz
Data setup time	ts ₁	Setup time of SCL with respect to the falling edge of SDA	4.7			μs
	ts ₂	Setup time of SDA with respect to the rising edge of SCL	250			ns
	ts ₃	Setup time of SCL with respect to the rising edge of SDA	4.0			μs
Data hold time	th ₁	Hold time of SCL with respect to the rising edge of SDA	4.0			μs
	th ₂	Hold time of SDA with respect to the falling edge of SCL	0.06			μs
Pulse width	tw _L	SCL low period pulse width	4.7			μs
	tw _H	SCL high period pulse width	4.0			μs
Input waveform conditions	ton	SCL/SDA (input) rising time			1000	ns
	tof	SCL/SDA (input) falling time			300	ns
Bus free time	t _{buf}	Interval between stop condition and start condition	4.7			μs

High-speed mode

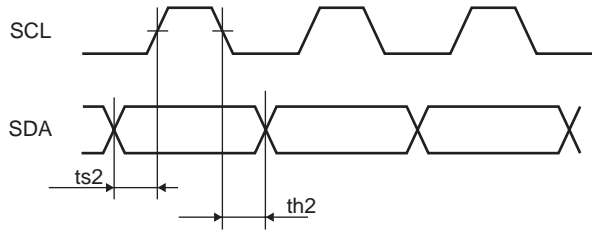
Parameter	Symbol	Conditions	min	typ	max	unit
SCL clock frequency	f _{scl}	Clock frequency of SCL	0		400	kHz
Data setup time	ts ₁	Setup time of SCL with respect to the falling edge of SDA	0.6			μs
	ts ₂	Setup time of SDA with respect to the rising edge of SCL	100			ns
	ts ₃	Setup time of SCL with respect to the rising edge of SDA	0.6			μs
Data hold time	th ₁	Hold time of SCL with respect to the rising edge of SDA	0.6			μs
	th ₂	Hold time of SDA with respect to the falling edge of SCL	0.06			μs
Pulse width	tw _L	SCL low period pulse width	1.3			μs
	tw _H	SCL high period pulse width	0.6			μs
Input waveform conditions	ton	SCL/SDA (input) rise time			300	ns
	tof	SCL/SDA (input) fall time			300	ns
Bus free time	t _{buf}	Interval between the stop condition and the start condition	1.3			μs

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I²C bus transfer method

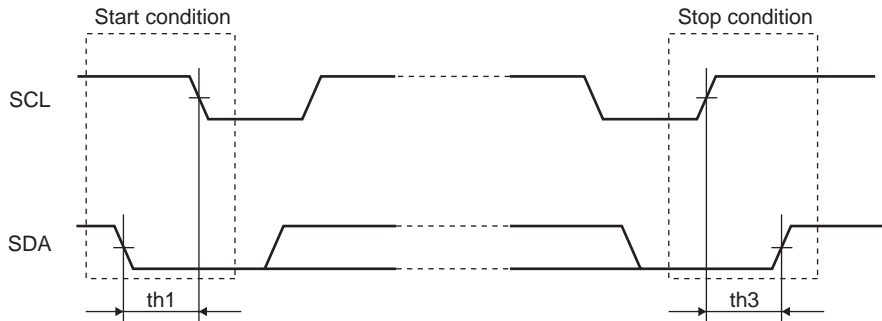
Start and stop conditions

The I²C bus requires that the state of SDA be preserved while SCL is high as shown in the timing diagram below during a data transfer operation.



When data is not being transferred, both SCL and SDA are in the high state. The start condition is generated and access is started when SDA is changed from high to low while SCL and SDA are high.

Conversely, the stop condition is generated and access is ended when SDA is changed from low to high while SCL is high.



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Data transfer and acknowledgement response

After the start condition is generated, data is transferred one byte (8 bits) at a time. Any number of data bytes can be transferred consecutively.

An ACK signal is sent to the sending side from the receiving side every time 8 bits of data are transferred. The transmission of an ACK signal is performed by setting the receiving side SDA to low after SDA at the sending side is released immediately after the clock pulse of SCL bit 8 in the data transferred has fallen low.

After the receiving side has sent the ACK signal, if the next byte transfer operation is to receive only the byte, the receiving side releases SDA on the falling edge of the 9th clock of SCL.

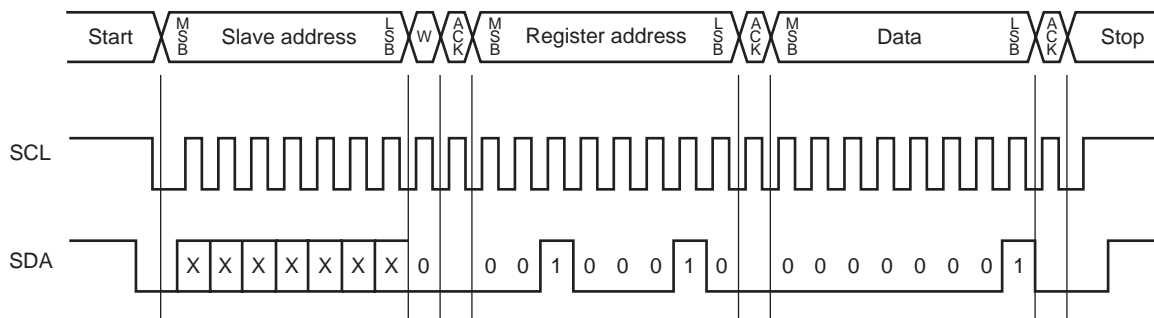
There are no CE signals in the I²C bus ; instead, a 7-bit slave address is assigned to each device, and the first byte of the transfer data is allocated to the 7-bit slave address and to the command (R/W) which specifies the direction of subsequent data transfer.

The READ function of the LV8094CT provides only the functionality to test the BUSY state.

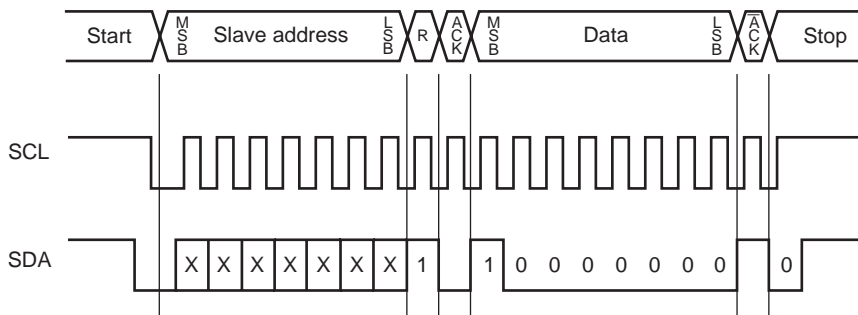
7-bit address data is transferred sequentially starting at the MSB and the second and subsequent bytes are written if the state of the 8th bit is low and read if the state is high.

In the LV8094CT, the slave address is stipulated to be “1110010.”.

WRITE mode timing



READ mode timing



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Data transfer write format

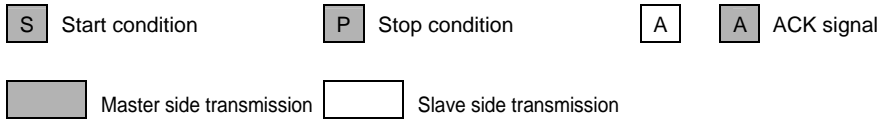
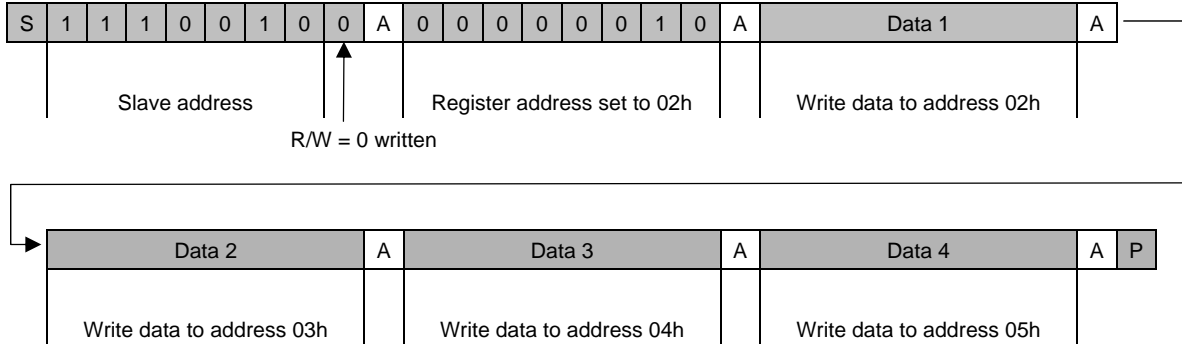
The slave address and Write command must be allocated to the first byte and the register address in the serial map must be designated in the second byte.

For the third byte, data transfer is carried out to the address designated by the register address which is written in the second byte. Subsequently, if data continues, the register address value is automatically incremented for the fourth and subsequent bytes.

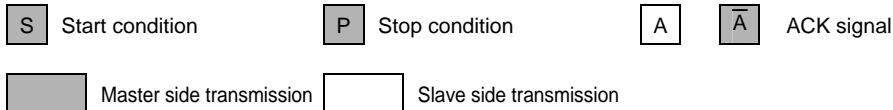
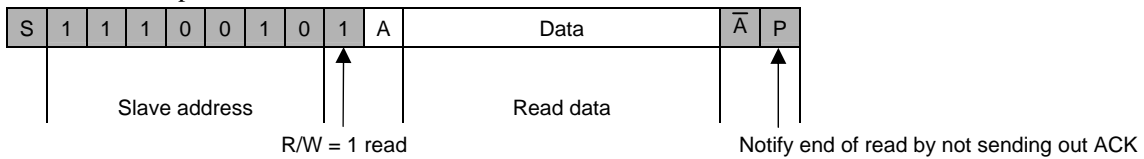
Thus, continuous data transfer starting at the designated address is made possible.

After the register address reaches 07h, the transfer address for the next byte is set to 00h.

Data write example



Data read example



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Serial Map

		Register Address								Data							
		A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0		0	0	0	0	0	0	0	0	M/I	DRVULSE [6 : 0]						
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1		0	0	0	0	0	0	0	1	GATE	x	ENIN	CKSEL [1 : 0]		RET [1 : 0]		INIT
		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
2		0	0	0	0	0	0	1	0	RST [7 : 0]							
		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
3		0	0	0	0	0	0	1	1	GTAS [7 : 0]							
		0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
4		0	0	0	0	0	1	0	0	GTBR [7 : 0]							
		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
5		0	0	0	0	0	1	0	1	GTBS [7 : 0]							
		0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
6		0	0	0	0	0	1	1	0	STP [7 : 0]							
		0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0
7		0	0	0	0	0	1	1	1	x	x	x	x	INITMOV [7 : 4]			
		0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
8		READ mode only register								BUSY	x	x	x	x	x	x	x
		READ mode only register								0	0	0	0	0	0	0	0

Upper : Register name Lower : Default value

Serial Mode Settings

0	0	0	0	0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0
---	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----	----	----

D0 to D6: DRVULSE [6 : 0]

Operation count setting register. Specify a number from 0 to 127.

The number of cyclic operations determined by <DRVPLUSE setting> × <STP setting> are performed.

Additional data can be input and data is added up to the equivalent of total of 512 pulses.

However, if the EN pin is set low or the ENIN register is set to 0, the DRVULSE input is not accepted because the DRVULSE counter is in the reset state.

Since the output operation is carried out at the time the DRVULSE input is recognized, the generation of the OUT signal is started at the time an ACK signal is generated after the execution of the instruction at address 00H according to the value of the waveform setup register established at that time.

D7	M/I
0	∞
1	macro

Operation direction switching

*Default

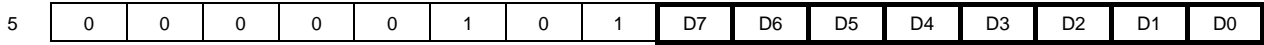
Infinity distance direction

Macro direction

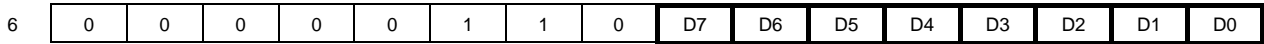
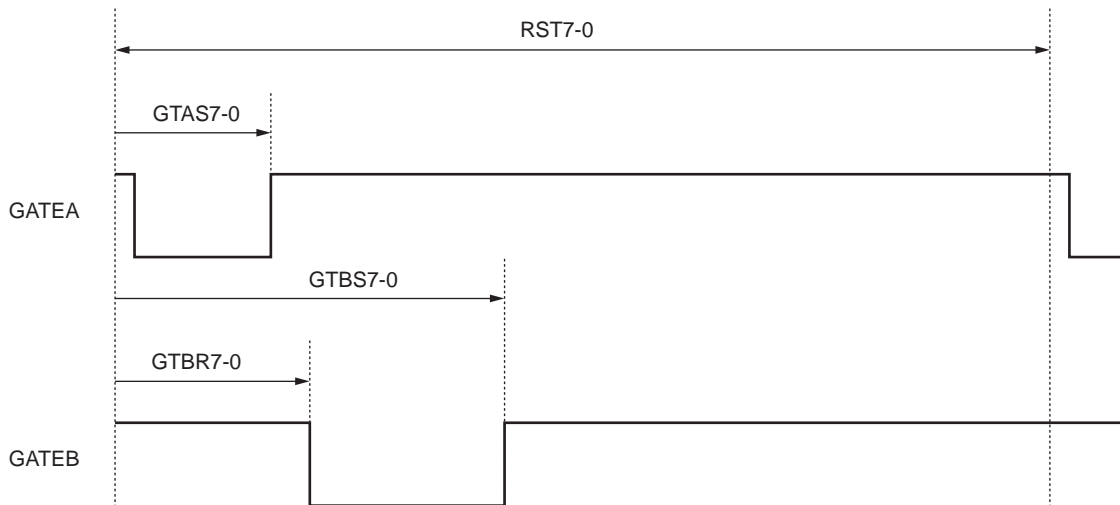
Operation direction switching register

The operation count setting register is reset when the register is switched. To stop the operation of the unit, switch the M/I register and set DRVULSE to 0 for input. This register is also used to set the direction of operation when the initialization sequence is to be performed.

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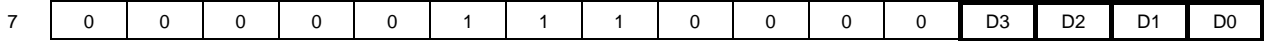
GTBS7 to GTBS0 : Sets the GATE_B pulse set value (0 to 255). Default = 0



STP7 to STP0 : Specifies the number of output pulse steps with regard to DRIVE input (1 to 256). Default = 1

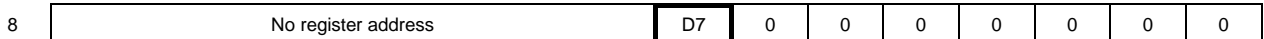
The setting value range is handled as the data value plus 1.

When data is input in 8-bit units (0 to 255), it is handled as an STP period of 1 to 256.



INITMOV7 to INITMOV4 : Sets the number of swing back of the initialization sequence to be performed (16 to 256). Default = 16

D3	D2	D1	D0	INIT7 to 4	16 to 256
0	0	0	0	0	16
0	0	0	1	1	32
0	0	1	0	2	48
0	0	1	1	3	64
0	1	0	0	4	80
0	1	0	1	5	96
0	1	1	0	6	112
0	1	1	1	7	128
1	0	0	0	8	144
1	0	0	1	9	160
1	0	1	0	10	176
1	0	1	1	11	192
1	1	0	0	12	208
1	1	0	1	13	224
1	1	1	0	14	240
1	1	1	1	15	256



READ only register line.

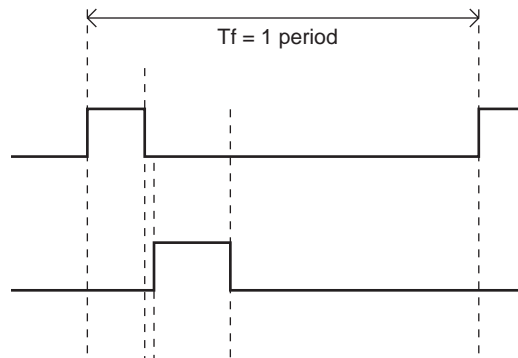
D7 : BUSY register Set to 1 when the IC is performing the output operation.

Set to 0 when the IC stops the output operation.

Functional Description

1 period :

One period of OUT waveform operation is equivalent to one output operation.



Initialization sequence (on or off and direction can be set by I²C) :

This is an internal sequence in which the actuator is moved to the initial position when the IC is started up.

Switching the value of the ENIN register from 0 to 1 when the EN pin is set high starts the IC (conversely, the IC is also started by switching the state of the EN pin from low to high when the ENIN is set to 1).

The presence or absence of the initialization operation can be set using the initialization mode select register (INIT). If the initialization operation is specified, the direction of the initialization sequence can be set using the M/I register.

- M/I register = 0 : Initialization processing in infinity direction

The IC performs the number of operations determined by STP setting period \times INIT setting times in the infinite direction, then waits for the period equivalent to STP setting period \times 4 times, and performs the number of swing back operations equal to STP setting period \times RET setting times in the macro direction.

- M/I register = 1 : Auto macro operation in macro direction

The IC performs the number of operations determined by STP setting period \times INIT setting times in the macro direction, then waits for the period equivalent to STP periods \times 4, and performs the number of swing back operations equal to STP period setting period \times RET setting times in the infinity direction.

CLK input :

The pin for the external CLK input that provides the reference time for generating drive waveforms.

The frequency division ratio for I²C communication can be selected from 1/4, 1/2, and 1/1. Drive waveforms are generated by counting this frequency-divided clk pulses as the basic count unit. The LV8093CS supports frequency from 10MHz to 60MHz depending on the frequency division ratio and counter settings.

Register setup sequence :

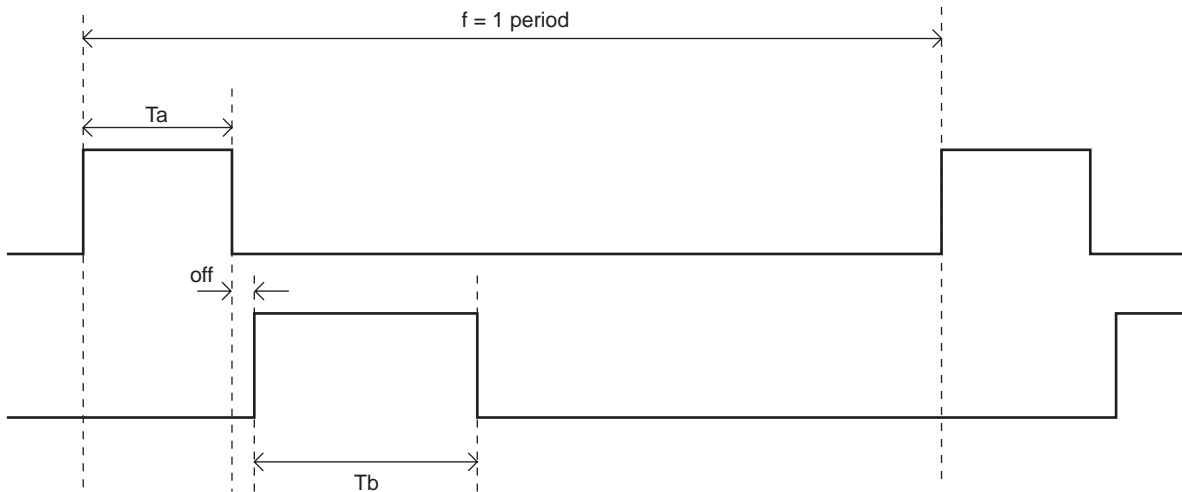
- (1) Apply VCC.
- (2) Set register addresses x01 to 0x07 (set the waveform and drive conditions).
- (3) Set the ENIN register to 1 (invoke initialization procedures if initialization is enabled or start up the IC).
- (4) Set up M/I and DRVPULSE to start the AF operation (actuator operation instruction).

I²C communication during output operation :

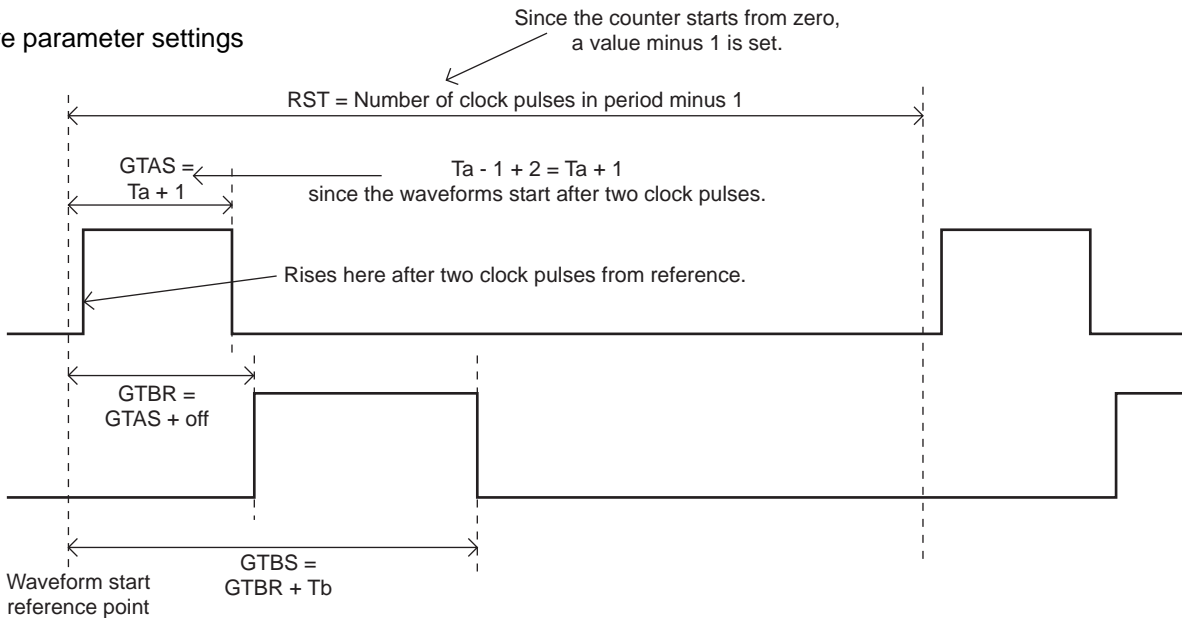
I²C communication with all the registers is possible even when the IC is in operation (OUT processing or BUSY is held high).

Actuator drive waveform settings :

Configuration of piezoelectric actuator drive waveform



Drive parameter settings



The drive waveforms are set using four parameters: RST, GTAS, GTBR and GTBS.

- RST** : Parameter determines the period, and sets the reference clock pulse count minus 1.
- GTAS** : Parameter determines the time taken for the gate signal A to the falling edge from the reference point. Since the signal raises after two clock pulses from the reference, the T_a reference clock cycle count plus 1 is set.
- GTBR** : Parameter determines the time taken for the gate signal B to the rising edge from the reference point. It sets the value obtained by adding the reference clock pulse count during the time from GTAS to "off."
- GTBS** : Parameter determines the time taken for the gate signal B to the falling edge from the reference point. It sets the value obtained by adding the reference clock pulse count during the time from GTBR to "Tb."

[Example of settings] When setting reference clock to 10MHz, period to $13\mu\text{s}$, T_a to $2.0\mu\text{s}$, off to $0.3\mu\text{s}$, and T_b to $3.0\mu\text{s}$
 Since the reference clock time is $0.1\mu\text{s}$:

The period is 130 clks. → Specify 129 (RST value of $130 - 1$).

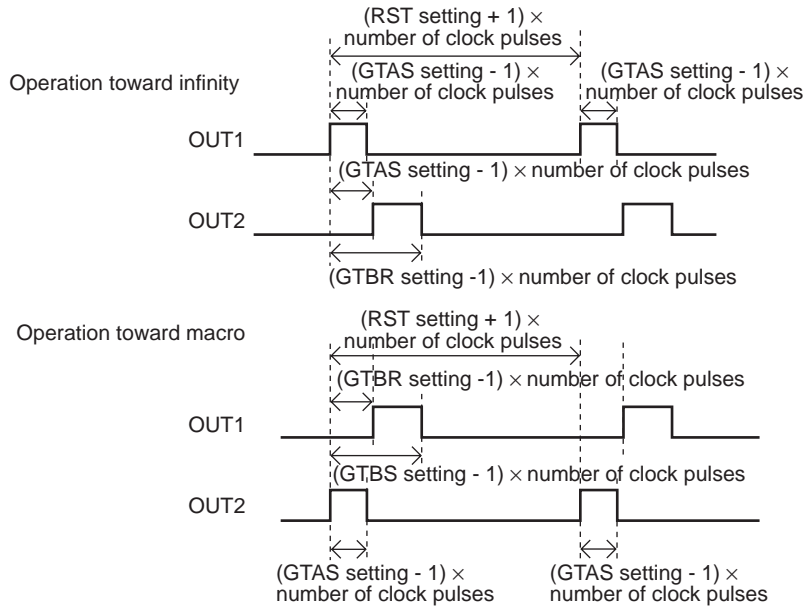
T_a is 20 clks. → Specify 21 (GTAS value of $20 + 1$).

off is 3 clks. → Specify 24 (GTBR value of $21 + 3$).

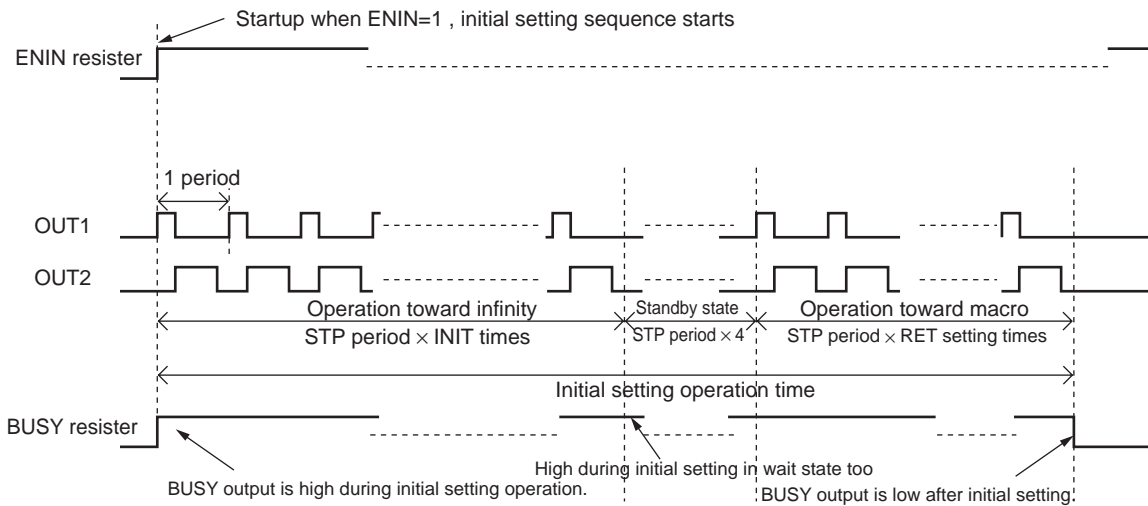
T_b is 30 clks. → Specify 54 (GTBS value of $24 + 30$).

Timing charts

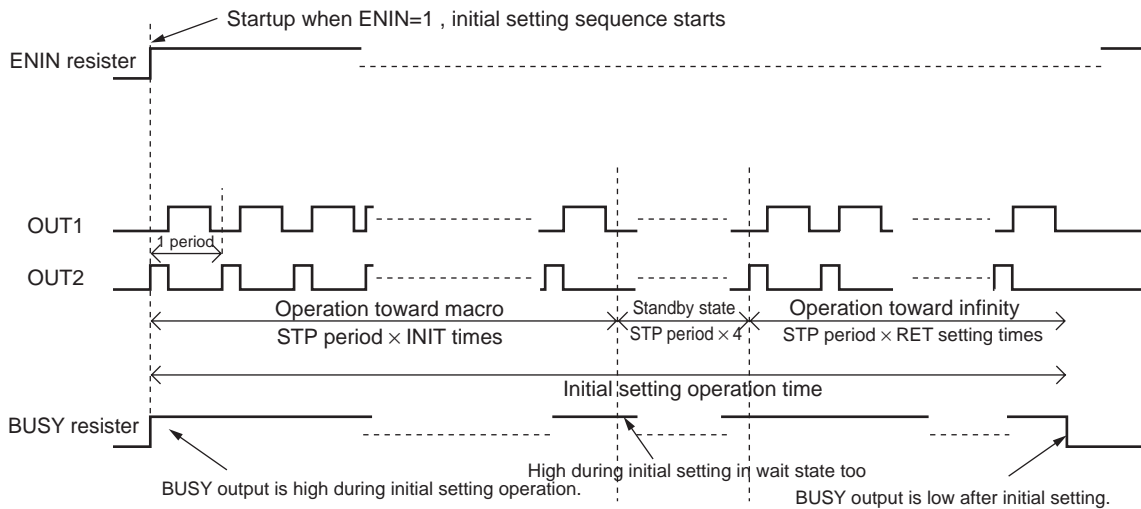
Enlarged view of the sequence of output signals



Sequence of initial setting operation (“on” or “off” can be set by the I²C settings.)
When M/I register = 00 → Movement toward infinity position

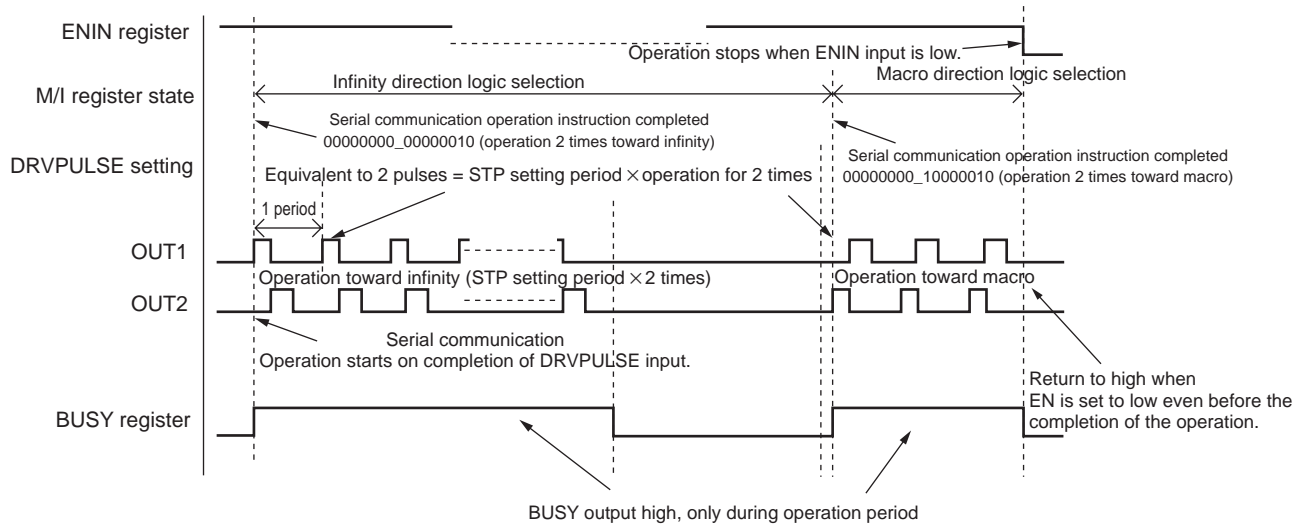


When M/I register = 01 → Movement toward macro position

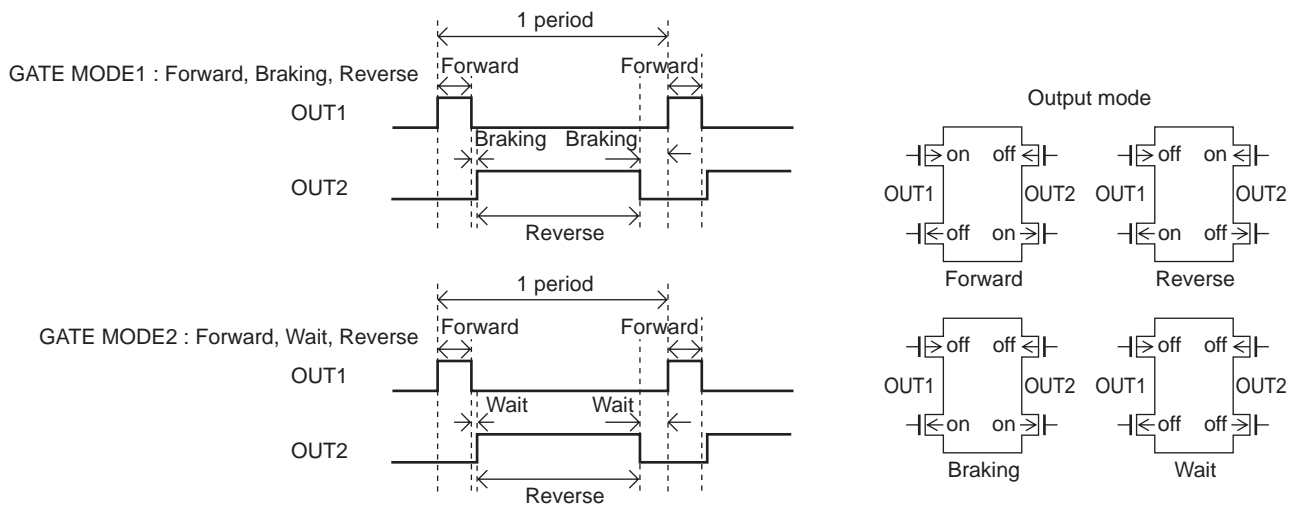


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Sequence of operations triggered by DRVPULSE input



Gate setting output logic



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