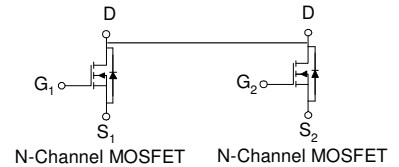
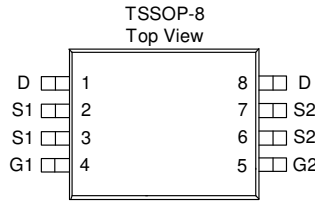


Dual N-Channel Logical Level MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (OHM)	I_D (A)
20	0.018 @ $V_{GS} = 4.5$ V	6.7
	0.024 @ $V_{GS} = 2.5$ V	5.8
	0.034 @ $V_{GS} = 1.8$ V	4.9

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe TSSOP-8 saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current ^a	$T_A=25^\circ\text{C}$	I_D	6.7	A
	$T_A=70^\circ\text{C}$		5.5	
Pulsed Drain Current ^b		I_{DM}	± 30	
Continuous Source Current (Diode Conduction) ^a		I_S	1.5	A
Power Dissipation ^a	$T_A=25^\circ\text{C}$	P_D	1.2	W
	$T_A=70^\circ\text{C}$		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typ	Max	
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	72	83	$^\circ\text{C/W}$
	Steady State		100	120	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions				Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 μA	0.4			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V			±10	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16 V, V _{GS} = 0 V			1	μA
		V _{DS} = 16 V, V _{GS} = 0 V, T _J = 55°C			10	μA
On-State Drain Current ^A	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	30			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 1 A			0.018	Ω
		V _{GS} = 2.5 V, I _D = 1 A			0.024	
		V _{GS} = 1.8 V, I _D = 1 A			0.034	
Forward Transconductance ^A	g _{fs}	V _{DS} = 10 V, I _D = 1 A		25		S
Diode Forward Voltage ^A	V _{SD}	I _S = 1 A, V _{GS} = 0 V		0.7		V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} =10V, V _{GS} =4.5V, I _D =1A		6.2		nC
Gate-Source Charge	Q _{gs}			1.0		
Gate-Drain Charge	Q _{gd}			1.9		
Turn-On Delay Time	t _{d(on)}	V _{DD} =10V, V _{GS} =4.5V, I _D =1A , R _{GEN} =10Ω		12		nS
Rise Time	t _r			15		
Turn-Off Delay Time	t _{d(off)}			56		
Fall-Time	t _f			17		

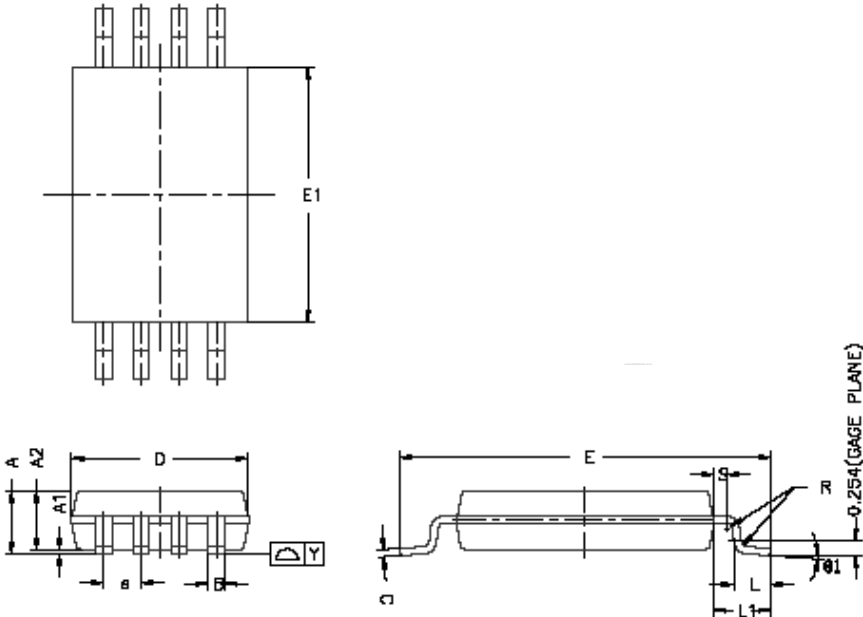
Notes

- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

Analog Power (APL) reserves the right to make changes without further notice to any products herein. APL makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does APL assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in APL data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. APL does not convey any license under its patent rights nor the rights of others. APL products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the APL product could create a situation where personal injury or death may occur. Should Buyer purchase or use APL products for any such unintended or unauthorized application, Buyer shall indemnify and hold APL and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that APL was negligent regarding the design or manufacture of the part. APL is an Equal Opportunity/Affirmative Action Employer.

Package Information

TSSOP-8: 8LEAD



DIM.	MILLIMETERS		
	MIN.	NDM.	MAX.
A	1.05	1.10	1.20
A(1)	0.05	0.10	0.15
A(2)	0.99	1.02	1.05
B	0.19	0.25	0.30
C	---	0.127	---
D	2.90	3.00	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
B	0.6595C		
L	0.45	0.60	0.75
L1	0.90	1.00	1.10
Y	---	---	0.10
Ø1	D'	4'	B'
R	0.09	---	---
S	0.20	---	---