Features

- Input Voltage: 36 V to 75 V
- Designed for AC6 ADSL Line-Interface Driver/Receivers
- Powers up to 32 Channels
- Quad Outputs (±8 V, ±3.75 V)
- Dual Logic On/Off Control
- Output Current Limit
- Unbalanced Load Protection
- Fixed Frequency Operation
- Over-Temperature Shutdown
- Under-Voltage Lockout
- 1500 VDC Isolation
- Space-Saving Solderable Case 1.2 sq. in. PCB Area (suffix N)
- Surface Mountable
- IPC Lead Free 2
- Safety Approvals: (Pending)
  UL60950
  CSA 22.2 950

Description

The PT4701 Excalibur™ power module is a 35-watt quad-output DC/DC converter that is designed to meet the power requirements of Texas Instruments' TNETD7112. The TNETD7112 is a dual-channel line-interface driver/receiver that compliments the AC6 ADSL chipset for use in POTS (plain old telephone service) applications. To conserve power, the TNETD7112 line drivers require two pairs of complimentary power supply voltages. These are ±8 V and ±3.75 V respectively.

The PT4701 module operates from a standard (–48 V) telecom central office supply and provides all four supply voltages as two complimentary balanced loads. *(This product is not suitable for unbalanced load applications.)* The load capacity allows the PT4701 to operate up to 16 line-driver ICs, representing 32 ADSL channels.

The PT4701 incorporates many features to simplify system integration. These include a flexible On/Off enable control, input under-voltage lock-out, and over-temperature protection. All outputs are short-circuit protected, and internally sequenced to meet the TNETD7112 power-up and power-down requirements.

The module is packaged in a space-saving solderable copper case, requires no heat sink, and can occupy as little as 1.2 in² of PCB area.

Ordering Information

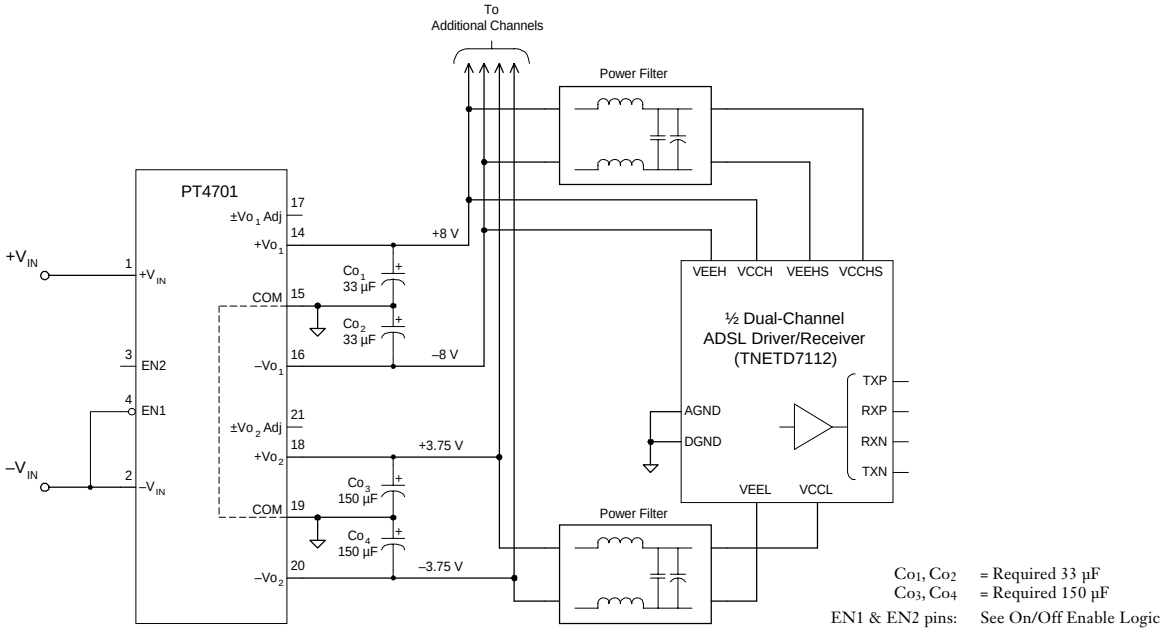
PT4701❑ = ±8.0/±3.75 V

PT Series Suffix (PT1234x)

Case/Pin Configuration	Order Suffix	Package Code
Vertical	**N**	(ENM)
Horizontal	**A**	(ENN)
SMD	**C**	(ENP)

(Reference the applicable package code drawing for the dimensions and PC layout)

Typical Application



Environmental Specifications

Characteristics	Symbols	Conditions		Min	Typ	Max	Units
Operating Temperature Range	T_a	Over V_{in} Range		–40	—	85 (i)	°C
Solder Reflow Temperature	T_{reflow}	Surface temperature of module pins or case		—	—	215 (ii)	°C
Storage Temperature	T_s	—		–40	—	125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted		—	500	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2 20-2000 Hz	Suffix A Suffix N, C	— —	15 (iii) 20 (iii)	— —	G's
Weight	—	Vertical/Horizontal		—	50	—	grams
Shutdown Temperature	OTP				115	125	°C
Flammability	—	Meets UL 94V-O					

Notes: *(i) See SOA curves or consult factory for appropriate derating.*
(ii) During solder reflow of SMD package version, do not elevate the module case, pins, or internal component temperatures above a peak of 215 °C. For further guidance refer to the application note, "Reflow Soldering Requirements for Plug-in Power Surface Mount Products," (SLTA051).
(iii) Only the case pins on through-hole pin configurations (N & A) must be soldered. For more information see the applicable package outline drawing.

Pin Configuration

Pin	Function
1	+Vin
2	–Vin
3	EN 2
4	EN 1
5	Do Not Connect
6	Do Not Connect
7	Do Not Connect

Pin	Function
8	Pin Not Present
9	Pin Not Present
10	Pin Not Present
11	Pin Not Present
12	Pin Not Present
13	Pin Not Present
14	$+Vo_1$

Pin	Function
15	COM
16	$–Vo_1$
17	$±Vo_1$ Adjust
18	$+Vo_2$
19	COM
20	$–Vo_2$
21	$±Vo_2$ Adjust

Note: Shaded functions indicates those pins that are at primary-side potential. All other pins are referenced to the secondary.

On/Off Enable Logic

Pin 3	Pin 4	Output Status
×	1	Off
1	0	On
0	×	Off

Notes:
Logic 1 =Open collector
Logic 0 = –Vin (pin 2) potential

For positive Enable function, connect pin 4 to pin 2 and use pin 3.

For negative Enable function, leave pin 3 open and use pin 4.

Pin Descriptions

+Vin: The positive input supply for the module with respect to $–V_{in}$. When powering the module from a –48V telecom central office supply, this input is connected to the primary system ground.

–Vin: The negative input supply for the module, and the 0VDC reference for the EN 1, and EN 2 inputs. When powering the module from a +48-V supply, this input is connected to the 48-V(Return).

EN 1: The negative logic input that activates the module output. This pin must be connected to $–V_{in}$ to enable the module's outputs. A high impedance disables the module's outputs.

EN 2: The positive logic input that activates the module output. If not used, this pin should be left open circuit. Connecting this input to $–V_{in}$ disables the module's outputs.

+Vo 1: This is the positive high-output voltage. It is the balanced compliment of ($–Vo_1$) and referenced to the secondary COM node.

–Vo 1: The negative high-output voltage, which is the balanced compliment of ($+Vo_1$) with respect to COM.

+Vo 2: This is the positive low-output voltage. It is the balanced complement of ($–Vo_2$) and referenced to the secondary COM node.

–Vo 2: The negative low-output voltage, which is the balanced compliment of ($+Vo_2$) with respect to COM.

COM: This is the common node and the secondary reference for all four regulated output voltages. It provides a return for any unbalanced load current, and is DC isolated from the input supply pins.

$±Vo_1$ Adjust: Using a single resistor, this pin allows the simultaneous adjustment of both $+Vo_1$ and $-Vo_1$ magnitude with respect to the COM node. Adjustment can be higher or lower than the preset value. If not used this pin should be left open circuit.

$±Vo_2$ Adjust: Using a single resistor, this pin allows the simultaneous adjustment of both $+Vo_2$ and $-Vo_2$ magnitudes with respect to the COM node. Adjustment can be higher or lower than the preset value. If not used this pin should be left open circuit.

PT4701 Electrical Specifications

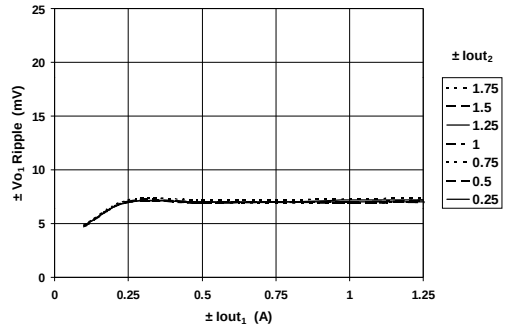
(Unless otherwise stated, the operating conditions are:- T_a =25 °C, V_{in} =48 V, and I_o =$I_o$max)

Characteristics	Symbols	Conditions		PT4701 Min	PT4701 Typ	PT4701 Max	Units
Output Current	Io_1, Io_2	Balanced load	±Vo_1 (8.0 V) ±Vo_2 (3.75 V)	0 0	— —	1.25 (1) 1.75 (1)	A
		Load imbalance	±Vo_1 ±Vo_2	— —	— —	±100 (2) ±100 (2)	mA
		Transient imbalance (<1 ms)	±Vo_1 ±Vo_2	— —	— —	±150 ±150	mA
Input Voltage Range	V_{in}	Continuous Surge (1 minute)		36 —	— —	75 80	V
Set-Point Voltage	Vo_1, Vo_2	Either output to COM	±Vo_1 ±Vo_2	7.76 3.82	8.0 3.94	8.24 4.06 (3)	V
Temperature Variation	Reg_{temp}	–40 °C≤T_a≤+85 °C, I_o =$I_o$min	±Vo_1 ±Vo_2	— —	±0.5 ±0.5	— —	%V_o
Line Regulation	Reg_{line}	All outputs, Over V_{in} range		—	±0.05	±0.25	%V_o
Load Regulation	Reg_{load}	All outputs, 0≤I_o≤$I_o$max		—	±0.2	±0.5	%V_o
Total Output Voltage Variation	ΔV_o tot	Includes set-point, line, load, –40 °C≤T_a≤+85 °C	±Vo_1 (8.0 V) ±Vo_2 (3.75 V)	7.6 3.75	— —	8.4 4.13 (3)	V
Efficiency	η			—	85	—	%
V_o Ripple (pk-pk)	V_n	Measured from each output to COM, 0 to 20 MHz bandwidth	±Vo_1 ±Vo_2	— —	10 5	— —	mV_{pp}
Transient Response	t_{tr} V_{os}	0.1 A/µs load step, 50 % to 75 % $I_o$max V_o over/undershoot		— —	100 2	— —	µSec %V_o
Output Adjust Range	Vo_x adj	Each ±V_o adjusted as pair		—	±10	—	%V_o
Balanced Load Current Limit Threshold	Io_{LIM}	Shutdown, auto restart	±Vo_1 ±Vo_2	— —	1.5 (1) 2.5 (1)	— —	A
Unbalanced Load Shutdown Threshold	$Io com_{sc}$	Shutdown & latch off (within 1 ms)		—	200 (2)	—	mA
Switching Frequency	f_s	Over V_{in} and I_o ranges		550	600	650	kHz
Under Voltage Lockout	V_{on} V_{off}	V_{in} increasing V_{in} decreasing		— —	34 32	— —	V
Enable Control (pins 3 & 4) High-Level Input Voltage Low-Level Input Voltage	 V_{IH} V_{IL}	Referenced to –V_{in} (pin 2)		 4 –0.2	 — —	 Open (4) 0.8 (4)	V
Low-Level Input Current	I_{IL}	Pin connected to –V_{in} (pin 2)		—	–0.16	–0.27	mA
Standby Input Current	I_{in} standby	pins 3 & 4 open circuit		—	5	20	mA
Internal Input Capacitance	C_{int}			—	1	—	µF
External Output Capacitance	C_o	Each output to COM	±Vo_1 ±Vo_2	33 150	— —	1,000 (5) 1,000 (5)	µF
Primary/Secondary Isolation	V_{iso} C_{iso} R_{iso}			1500 — 10	— 2,200 —	— — —	V pF MΩ

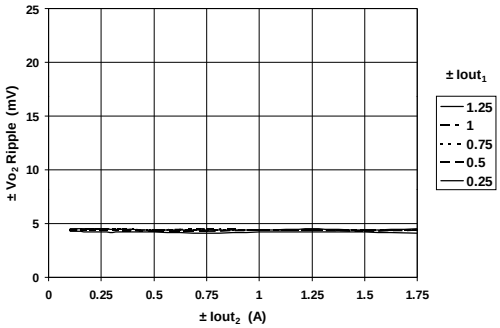
Notes: *(1) A balanced load is defined as the current flowing out of (+Vo_x) being to equal that flowing into (–Vo_x). The current flowing in the COM termnal is zero.*
(2) The load imbalance is the difference between the current flowing out of (+Vo_x) and flowing into (–Vo_x). The difference flows in the COM terminal.
(3) The nominal output voltage of ±Vo_2 is 3.94 V. The output voltage and tolerance is defined as 3.75 V, –0%, +10%.
(4) The Enable inputs (pins 3 & 4) have internal pull-ups. Leaving pin 3 open-circuit and connecting pin 4 to –V_{in} allows the the converter to operate when input power is applied. The maximum open-circuit voltage is 5V.
(5) Capacitance added to each pair of complimentary output voltages (±Vo_x) must be divided equally between (+Vo_x) and (–Vo_x) with respect to the COM termnial. E.g. Co_1 must equal Co_2, and Co_3 must equal Co_4.

Performance Characteristics; V_{in} =48 V (See Note A)

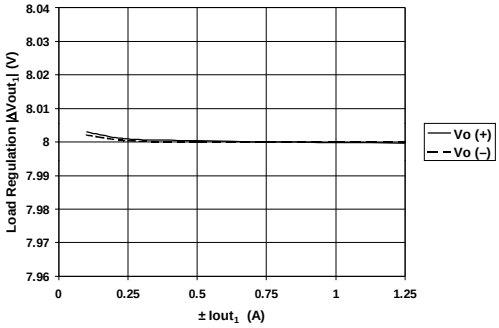
Output Ripple $Vout_1$ vs $\pm Iout_1$ & $\pm Iout_2$



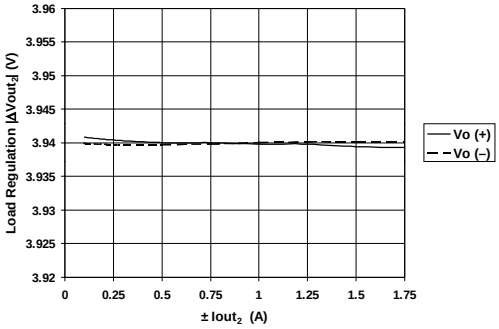
Output Ripple $\pm Vout_2$ vs $\pm Iout_1$ & $\pm Iout_2$



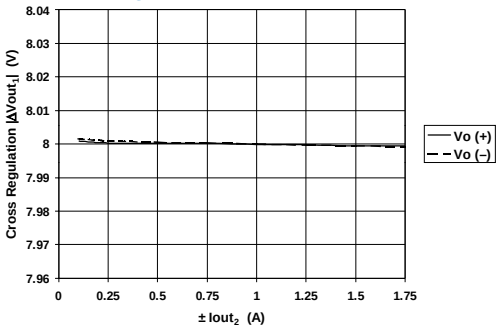
Load Regulation $\pm Vout_1$ vs $\pm Iout_1$



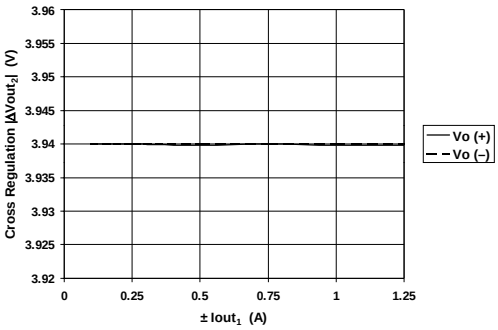
Load Regulation $\pm Vout_2$ vs $\pm Iout_2$



Cross Regulation $\pm Vout_1$ vs $\pm Iout_2$



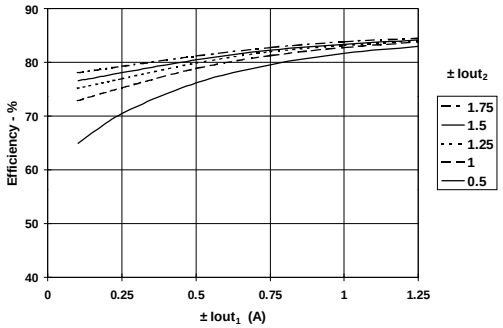
Cross Regulation $\pm Vout_2$ vs $\pm Iout_1$



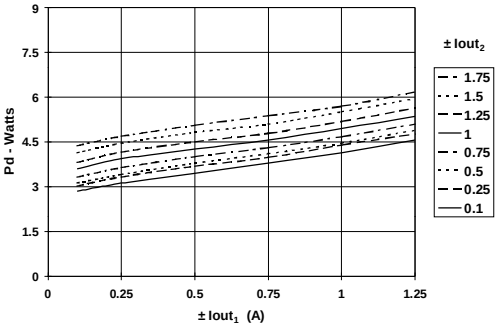
Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*

Performance Characteristics; V_{in} =48 V (See Note A)

Efficiency vs ±$Iout_1$ & ±$Iout_2$



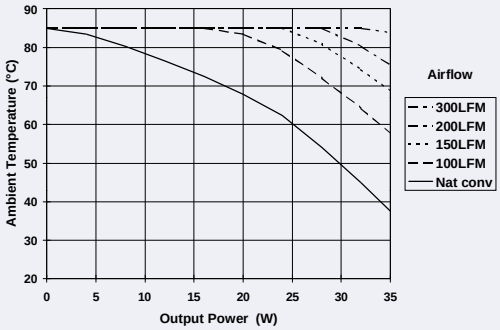
Power Dissipation vs ±$Iout_1$ & ±$Iout_2$



PT4701 Safe Operating Area (SOA) (See Note B)

(All outputs proportionally loaded from 0 to 100 % of full load)

SOA vs Total Output Power; V_{in} =48 V



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.*
Note B: *SOA curves represent operating conditions at which the internal components are at or below the manufacturer's maximum rated operating temperatures.*

Operating Features of the PT4701 Quad-Output DC/DC Converter for DSL Line Drivers

Balanced Load Fault Protection

A balanced load fault is the result of excess current flowing from one $+V_o$ output directly to the corresponding $-V_o$ output. The current flowing in or out of the COM node (pins 15 & 19) under this condition is within normal operating limits. Both (±)dual outputs from the PT4701 DC/DC converter incorporate protection against this type of load fault. This includes an absolute current limit in combination with a fault timeout period. When the balanced fault current from either ±dual output exceeds the "Balanced Load Current Limit Threshold" (see data sheet specifications), the converter initially limits the fault current to approximately 150 % of the maximum output current rating. If the fault persists for more than 20 ms the converter shuts down, forcing the voltage at all four regulated outputs to simultaneously fall to zero. Following shutdown the converter will periodically attempt to recover by executing a soft-start power-up. The converter will continually cycle through successive over-current shutdowns and restarts until the fault is removed.

Imbalanced Load Fault Protection

An imbalanced load fault is the result of excess current flowing between any one of the $+V_o$ (or the $-V_o$) outputs, and the COM node (pins 15 & 19). When the current sensed in the COM node exceeds the "Unbalanced Load Shutdown Threshold" (see data sheet specifications), the PT4701 shuts down and latches off within 1ms. Once latched off, the module must be reset by momentarily interrupting the input power source.

Over-Temperature Protection

The PT4701 DC/DC converter has an internal temperature sensor, which monitors the temperature of the module's internal components. If the sensed temperature exceeds a nominal 115 °C, the converter will shut down. The converter will automatically restart when the sensed temperature returns to about 100 °C.

Under-Voltage Lock-Out

The Under-Voltage Lock-Out (UVLO) circuit prevents operation of the converter whenever the input voltage to the module is insufficient to maintain output regulation. The UVLO has approximately 2 V of hysterisis. This is to prevent oscillation with a slowly changing input voltage. Below the UVLO threshold the module is off and the enable control inputs, EN1 and EN2 are inoperative.

Primary-Secondary Isolation

The PT4701 DC/DC converter incorporates electrical isolation between the input terminals (primary) and the output terminals (secondary). All converters are production tested to a withstand voltage of 1500 VDC. The isolation complies with UL60950 and EN60950, and the requirements for operational isolation. This allows the converter to be configured for either a positive or negative input voltage source.

The regulation control circuitry for these modules is located on the secondary (output) side of the isolation barrier. Control signals are passed between the primary and secondary sides of the converter. The data sheet 'Pin Descriptions' and 'Pin-Out Information' provides guidance as to which reference (primary or secondary) that must be used for each of the external control signals.

Input Current Limiting

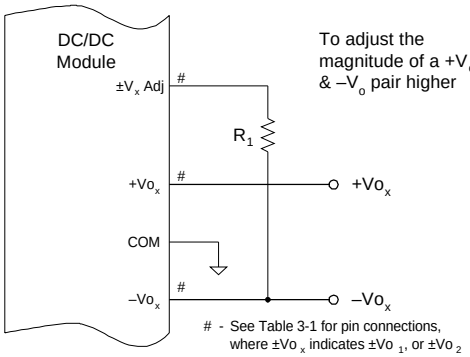
The converter is not internally fused. For safety and overall system protection, the maximum input current to the converter must be limited. Active or passive current limiting can be used. Passive current limiting can be a fast acting fuse. A 125-V fuse, rated no more than 5 A, is recommended. Active current limiting can be implemented with a current limited "Hot-Swap" controller.

Adjusting the Output Voltages of the PT4701 Quad-Output DC/DC Converters

The PT4701 quad-output DC/DC converter produces two pairs of balanced ±V_o complimentary output voltages. The magnitude of each balanced pair of outputs may be adjusted higher or lower by up to ±10 %. The adjustment method uses a single external resistor [1], which adjusts the magnitude of the respective +V_o and –V_o simultaneously. The value of the resistor determines the magnitude of adjustment, and the placement of the resistor determines the direction of adjustment (increase or decrease). The resistor values can be calculated using the appropriate formula (see below). The formula constants are provided in Table 3-2. Alternatively the resistor value may be selected directly from Table 3-3 and Table 3-4, for ±Vo_1 and ±Vo_2 respectively. The placement of each resistor is as follows.

Adjust Up: To increase the magnitude of the complimentary output voltages, add a resistor R_1 between the appropriate ±*Vo_x Adj* ('±Vo_1 Adj' or '±Vo_2 Adj') and the -*Vo_x* voltage rail. See Figure 3-1(a) and Table 3-1 for the resistor placement and pin connections.

Figure 3-1a



Notes:

1. Use only a single 1 % (or better) tolerance resistor in either the R_1 or (R_2) location to adjust a specific output. Place the resistor as close to the ISR as possible.
2. Never connect capacitors to any of the 'Vo_x Adj' pins. Any capacitance added to these control pins will affect the stability of the respective regulated output.

Adjust Down: To decrease the magnitude of the complimentary output voltages, add a resistor (R_2), between the appropriate *Vo_x Adj* (Vo_1 Adj or Vo_2 Adj,) and the *+Vo_x* voltage rail. See Figure 3-1(b) and Table 3-1 for the resistor placement and pin connections.

Figure 3-1b

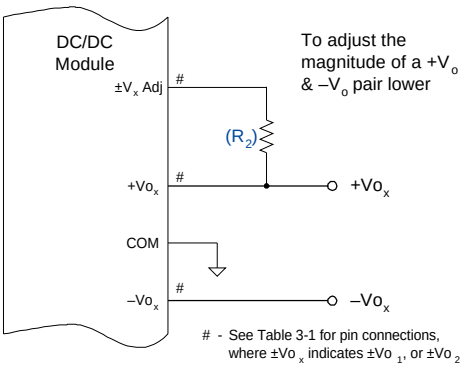


Table 3-1; Adjust Resistor Pin Connections

	To Adjust Up Connect R_1		To Adjust Down Connect (R_2)	
	from ±Vo_x Adj	to –Vo_x	from ±Vo_x Adj	to +Vo_x
±Vo_1	17	16	17	14
±Vo_2	21	20	21	18

Calculation of Resistor Adjust Values

The adjust resistor value may also be calculated using an equation. Note that the equation for R_1 [Adjust Up] is different to that for (R_2) [Adjust Down].

$$R_1 \text{ [Adjust Up]} = \frac{V_r R_o}{2 (V_a - V_o)} - R_s \quad k\Omega$$

$$(R_2) \text{ [Adjust Down]} = \frac{R_o (2 V_a - V_r)}{2 (V_o - V_a)} - R_s \quad k\Omega$$

Where: V_o = Original output voltage (±Vo_x)
V_a = Adjusted output voltage (±Va_x)
V_r = The reference voltage from Table 3-2
R_o = The resistance value in Table 3-2
R_s = The series resistance from Table 3-2

Table 3-2

ADJUSTMENT RANGE AND FORMULA PARAMETERS

	$\pm Vo_1$ Bus	$\pm Vo_2$ Bus
V_o(nom)	8.0 V	3.94 V
V_a(min)	7.2 V	3.55 V
V_a(max)	8.8 V	4.33 V
V_r	2.5 V	1.24 V
R_o (kΩ)	14.3	13.0
R_s (kΩ)	20.0	16.2

Table 3-3

ADJUSTMENT RESISTOR VALUES FOR $\pm Vo_1$

Adj. Resistor		R_1/(R_2)
% Adjust	$\pm V_a$(req'd)	
–10 %	7.20 V	(86.4) kΩ
– 9 %	7.28 V	(99.8) kΩ
– 8 %	7.36 V	(117.0) kΩ
– 7 %	7.44 V	(138.0) kΩ
– 6 %	7.52 V	(167.0) kΩ
– 5 %	7.60 V	(207.0) kΩ
– 4 %	7.68 V	(267.0) kΩ
– 3 %	7.76 V	(368.0) kΩ
– 2 %	7.84 V	(569.0) kΩ
– 1 %	7.92 V	(1.17) MΩ
0 %	8.00 V	
+ 1 %	8.08 V	203.0 kΩ
+ 2 %	8.16 V	91.7 kΩ
+ 3 %	8.24 V	54.5 kΩ
+ 4 %	8.32 V	35.9 kΩ
+ 5 %	8.40 V	24.7 kΩ
+ 6 %	8.48 V	17.2 kΩ
+ 7 %	8.56 V	11.9 kΩ
+ 8 %	8.64 V	7.9 kΩ
+ 9 %	8.72 V	4.8 kΩ
+10 %	8.80 V	2.3 kΩ

R_1 = Black, R_2 = (Blue)

Table 3-4

ADJUSTMENT RESISTOR VALUES FOR Vo_2

Adj. Resistor	R_1/(R_2)
$\pm V_a$(req'd)	
3.546 V	(80.3) kΩ
3.585 V	(92.5) kΩ
3.625 V	(108.0) kΩ
3.664 V	(127.0) kΩ
3.704 V	(153.0) kΩ
3.743 V	(190.0) kΩ
3.782 V	(245.0) kΩ
3.822 V	(336.0) kΩ
3.861 V	(519.0) kΩ
3.900 V	(1.07)MΩ
3.940 V	
3.979 V	188.0 kΩ
4.019 V	86.1 kΩ
4.058 V	52.0 kΩ
4.098 V	34.9 kΩ
4.137 V	24.7 kΩ
4.176 V	17.9 kΩ
4.216 V	13.0 kΩ
4.255 V	9.4 kΩ
4.295 V	6.5 kΩ
4.334 V	4.3 kΩ

R_1 = Black, R_2 = (Blue)

Using the On/Off Enable Controls on the PT4701 Quad-Output DC/DC Converter

The PT4701 is a quad-output DC/DC converter that is specifically designed for powering DSL line driver ICs. The converter incorporates two output enable controls. EN1 (pin 4) is the *Negative Enable* input, and EN2 (pin 3) is the *Positive Enable* input. Both inputs are electrically referenced to $-V_{in}$ (pin 2) on the primary or input side of the converter. A pull-up resistor is not required, but may be added if desired. Voltages of up to 70 V can be safely applied to the either of the *Enable* pins.

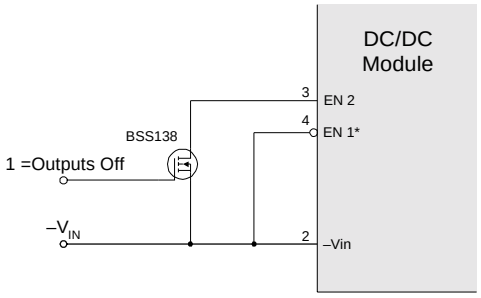
Automatic (UVLO) Power-Up

Connecting EN1 (pin 4) to $-V_{in}$ (pin 2) and leaving EN2 (pin 3) open-circuit configures the converter for automatic power up. (See data sheet "Typical Application"). The converter control circuitry incorporates an "Under Voltage Lockout" (UVLO) function, which disables the converter until the minimum specified input voltage is present at $\pm V_{in}$. (See data sheet Specifications). The UVLO circuitry ensures a clean transition during power-up and power-down, allowing the converter to tolerate a slow-rising input voltage. For most applications EN1 and EN2, can be configured for automatic power-up.

Positive Output Enable (Negative Inhibit)

To configure the converter for a positive enable function, connect EN1 (pin 4) to $-V_{in}$ (pin 2), and apply the system On/Off control signal to EN2 (pin 3). In this configuration, a low-level input voltage ($-V_{in}$ potential) applied to pin 3 disables the converter outputs. Figure 1 is an example of this configuration.

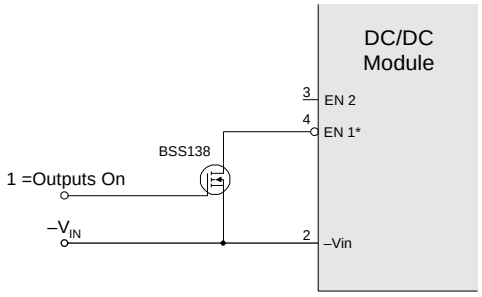
Figure 1; Positive Enable Configuration



Negative Output Enable (Positive Inhibit)

To configure the converter for a negative enable function, EN2 (pin 3) is left open circuit, and the system On/Off control signal is applied to EN1 (pin 4). A low-level input voltage ($-V_{in}$ potential) must then be applied to pin 4 in order to enable the outputs of the converter. An example of this configuration is detailed in Figure 2. *Note: The converter will only produce and output voltage if a valid input voltage is applied to* $\pm V_{in}$.

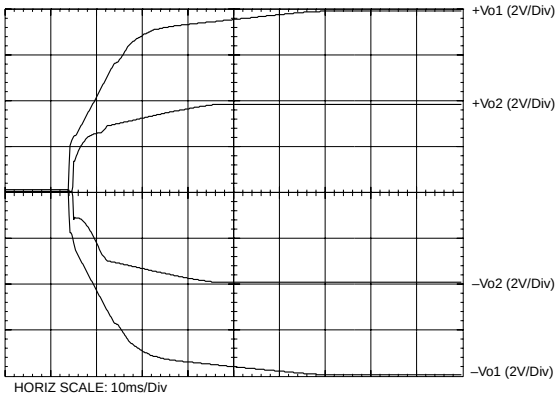
Figure 2; Negative Enable Configuration



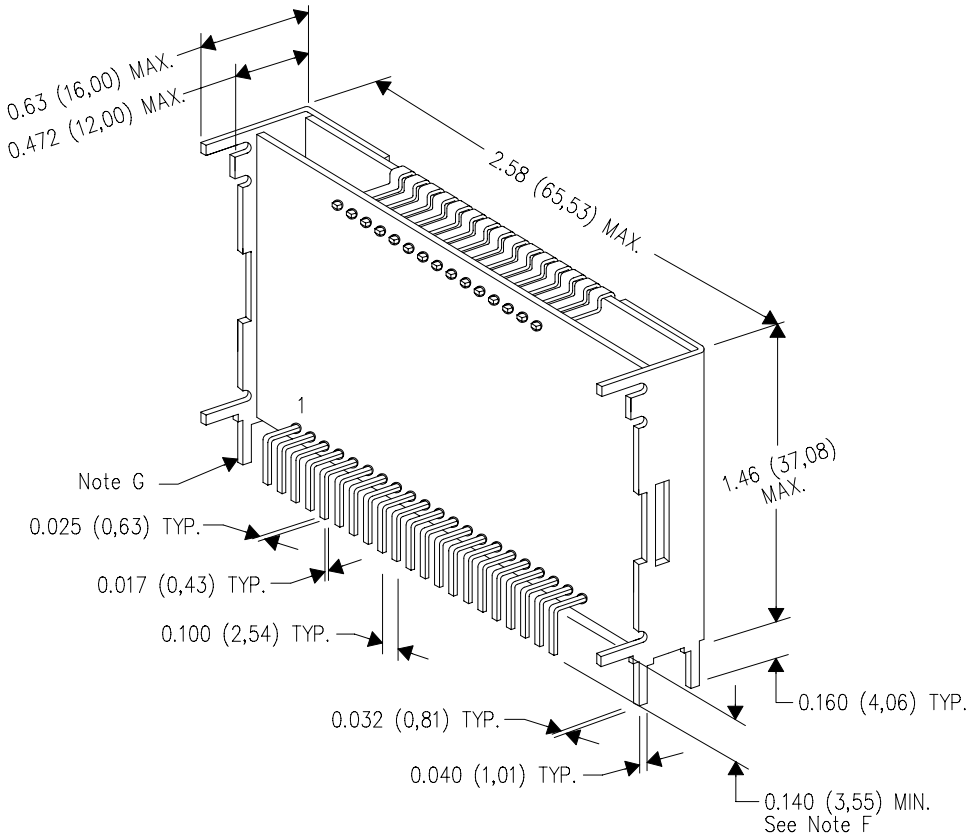
On/Off Output Voltage Sequencing

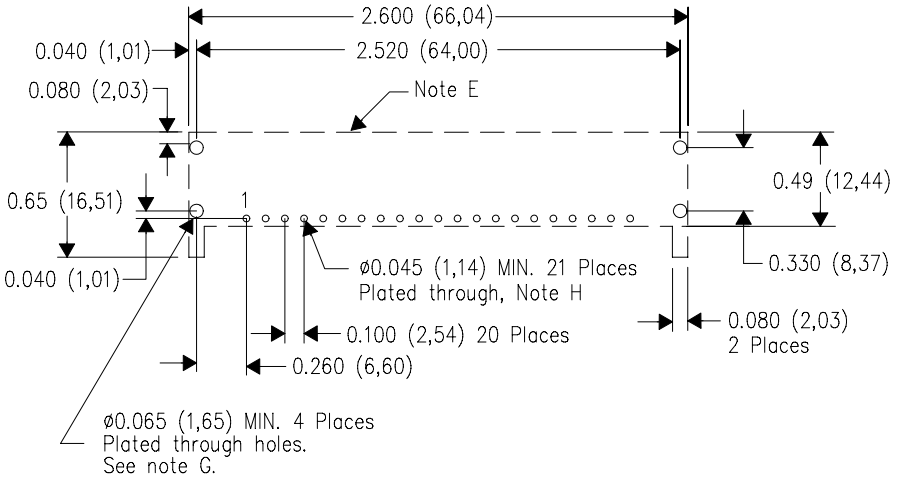
The PT4701 converter power-up characteristics meet the requirements of Texas Instruments' TNETD7112 dual-channel line-interface driver/receiver ICs. All four outputs from the converter are internally sequenced to power up in unison. Figure 3 shows the waveforms from a PT4701 following the application of power. There is a delay of appoximately 25 ms from the application power to the point that the output voltages begin to rise. The converter typically produces a fully regulated output within 75 ms.The waveforms of Figure 3 were measured with loads of approximately 50% on each output, with an input source of 48 VDC.

Figure 3; PT4701 Power-up Sequence



Suffix N





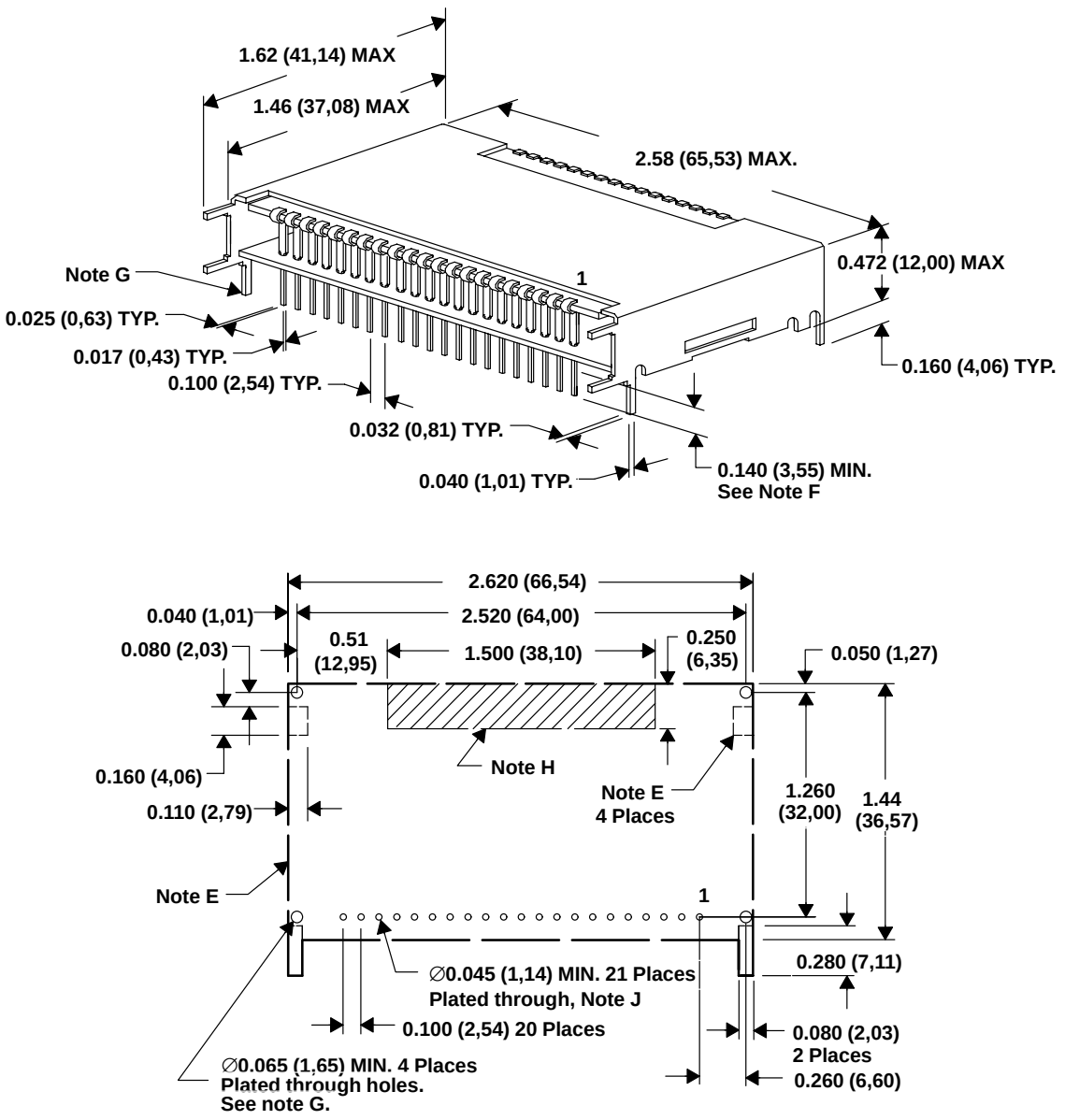
PC LAYOUT

4203486/B 02/03

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended mechanical keep out area.
F. Electrical pin length mounted on printed circuit board, from seating plane to pin end.
G. The case is electrically uncommitted. The recommended connection is to secondary ground.
H. Some pins may not be present, see product specifications.

ENN (R–MSIP–T21) **METAL SINGLE–IN-LINE MODULE**

Suffix A

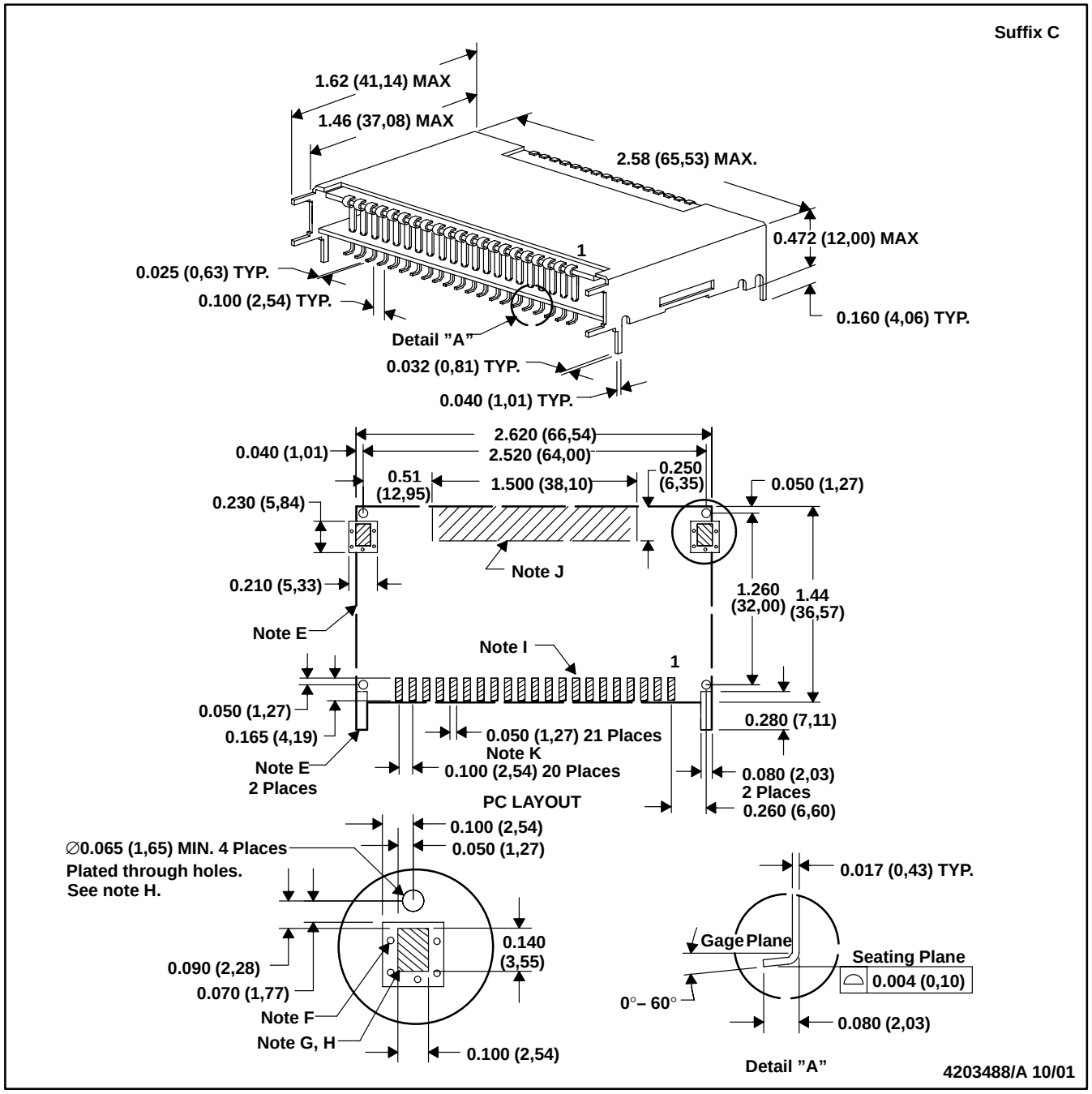


PC LAYOUT

4203487/A 10/01

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended mechanical keep out area.
F. Electrical pin length mounted on printed circuit board, from seating plane to pin end.
G. The case is electrically uncommitted. The recommended connection is to secondary ground.
H. No copper, power or signal traces in this area.
J. Some pins may not be present, see product specifications.

ENP (R–MSIP–G21) **METAL SINGLE–IN-LINE MODULE**



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended mechanical keep out area.
F. Vias are recommended to improve copper adhesion.
G. Solder mask openings to copper island for solder joints to mechanical pins.
H. The case is electrically uncommitted. The recommended connection is to secondary ground.
I. Power pin connections should utilize two or more vias per input, ground and output pin.
J. No copper, power or signal traces in this area.
K. Some pins may not be present, see product specifications.

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