

# MC44603A

## Enhanced Mixed Frequency Mode GreenLine™ PWM Controller:

### Fixed Frequency, Variable Frequency, Standby Mode

The MC44603A is an enhanced high performance controller that is specifically designed for off-line and dc-to-dc converter applications. This device has the unique ability of automatically changing operating modes if the converter output is overloaded, unloaded, or shorted, offering the designer additional protection for increased system reliability. The MC44603A has several distinguishing features when compared to conventional SMPS controllers. These features consist of a foldback facility for overload protection, a standby mode when the converter output is slightly loaded, a demagnetization detection for reduced switching stresses on transistor and diodes, and a high current totem pole output ideally suited for driving a power MOSFET. It can also be used for driving a bipolar transistor in low power converters (< 150 W). It is optimized to operate in discontinuous mode but can also operate in continuous mode. Its advanced design allows use in current mode or voltage mode control applications.

#### Features

- Pb-Free Package is Available\*
- **Current or Voltage Mode Controller**
- Operation up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle-by-Cycle Current Limiting
- Oscillator with Precise Frequency Control

#### High Flexibility

- Externally Programmable Reference Current
- Secondary or Primary Sensing<sup>7</sup>
- Synchronization Facility
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis

#### Safety/Protection Features

- Overvoltage Protection Against Open Current and Open Voltage Loop
- Protection Against Short Circuit on Oscillator Pin
- Fully Programmable Foldback
- Soft-Start Feature
- Accurate Maximum Duty Cycle Setting
- Demagnetization (Zero Current Detection) Protection
- Internally Trimmed Reference
- Enhanced Output Drive

#### GreenLine Controller: Low Power Consumption in Standby Mode

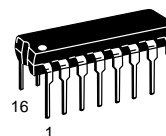
- Low Startup and Operating Current
- Fully Programmable Standby Mode
- Controlled Frequency Reduction in Standby Mode
- Low dV/dT for Low EMI Radiations



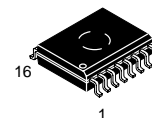
ON Semiconductor®

<http://onsemi.com>

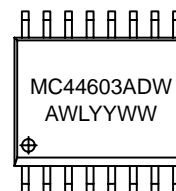
#### MARKING DIAGRAMS



PDIP-16  
P SUFFIX  
CASE 648

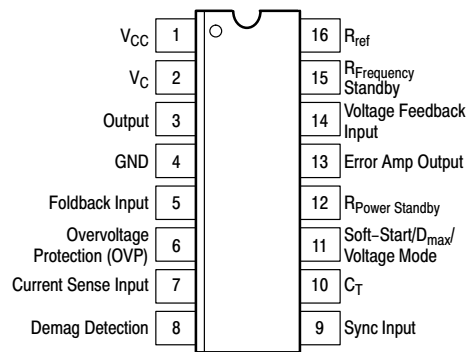


SOIC-16  
DW SUFFIX  
CASE 751G



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week

#### PIN CONNECTIONS



(Top View)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 21 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC44603A

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Supply Voltage with Respect to Ground (Pin 4)	$V_C$ $V_{CC}$	18	V
Output Current (Note 1)			mA
Source	$I_{O(\text{Source})}$	-750	
Sink	$I_{O(\text{Sink})}$	750	
Output Energy (Capacitive Load per Cycle)	$W$	5.0	$\mu\text{J}$
$R_F$ Stby, $C_T$ , Soft-Start, $R_{\text{ref}}$ , $R_P$ Stby Inputs	$V_{\text{in}}$	-0.3 to 5.5	V
Foldback Input, Current Sense Input, E/A Output, Voltage Feedback Input, Overvoltage Protection, Synchronization Input	$V_{\text{in}}$	-0.3 to $V_{CC} + 0.3$	V
Synchronization Input			
High State Voltage	$V_{\text{IH}}$	$V_{CC} + 0.3$	V
Low State Reverse Current	$V_{\text{IL}}$	-20	mA
Demagnetization Detection Input Current			mA
Source	$I_{\text{demag-ib (Source)}}$	-4.0	
Sink	$I_{\text{demag-ib (Sink)}}$	10	
Error Amplifier Output Sink Current	$I_{\text{E/A (Sink)}}$	20	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Dual-In-Line, Case 648			
Maximum Power Dissipation at $T_A = 85^\circ\text{C}$	$P_D$	0.6	W
Thermal Resistance, Junction-to-Air	$R_{\theta\text{JA}}$	100	$^\circ\text{C/W}$
DW Suffix, Surface Mount, Case 751G			
Maximum Power Dissipation at $T_A = 85^\circ\text{C}$	$P_D$	0.45	W
Thermal Resistance, Junction-to-Air	$R_{\theta\text{JA}}$	145	$^\circ\text{C/W}$
Operating Junction Temperature	$T_J$	150	$^\circ\text{C}$
Operating Ambient Temperature	$T_A$	-25 to +85	$^\circ\text{C}$

1. Maximum package power dissipation limits must be observed.
2. ESD data available upon request.

# MC44603A

**ELECTRICAL CHARACTERISTICS** ( $V_{CC}$  and  $V_C = 12$  V, (Note 3),  $R_{ref} = 10$  k $\Omega$ ,  $C_T = 820$  pF, for typical values  $T_A = 25^\circ\text{C}$ , for min/max values  $T_A = -25^\circ$  to  $+85^\circ\text{C}$  (Note 4), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

## OUTPUT SECTION

Output Voltage (Note 5)					V
Low State ( $I_{Sink} = 100$ mA) ( $I_{Sink} = 500$ mA)	$V_{OL}$	–	1.0 1.4	1.2 2.0	
High State ( $I_{Source} = 200$ mA) ( $I_{Source} = 500$ mA)	$V_{OH}$	–	1.5 2.0	2.0 2.7	
Output Voltage During Initialization Phase $V_{CC} = 0$ to $1.0$ V, $I_{Sink} = 10$ $\mu\text{A}$ $V_{CC} = 1.0$ to $5.0$ V, $I_{Sink} = 100$ $\mu\text{A}$ $V_{CC} = 5.0$ to $13$ V, $I_{Sink} = 1.0$ mA	$V_{OL}$	–	–	1.0	V
Output Voltage Rising Edge Slew-Rate ( $C_L = 1.0$ nF, $T_J = 25^\circ\text{C}$ )	$dV_o/dT$	–	300	–	V/ $\mu\text{s}$
Output Voltage Falling Edge Slew-Rate ( $C_L = 1.0$ nF, $T_J = 25^\circ\text{C}$ )	$dV_o/dT$	–	–300	–	V/ $\mu\text{s}$

## ERROR AMPLIFIER SECTION

Voltage Feedback Input ( $V_{E/A\ out} = 2.5$ V)	$V_{FB}$	2.42	2.5	2.58	V
Input Bias Current ( $V_{FB} = 2.5$ V)	$I_{FB-ib}$	–2.0	–0.6	–	$\mu\text{A}$
Open Loop Voltage Gain ( $V_{E/A\ out} = 2.0$ to $4.0$ V)	$A_{VOL}$	65	70	–	dB

## ERROR AMPLIFIER SECTION (continued)

Unity Gain Bandwidth $T_J = 25^\circ\text{C}$ $T_J = -25^\circ$ to $+85^\circ\text{C}$	BW	–	4.0	–	MHz
Voltage Feedback Input Line Regulation ( $V_{CC} = 10$ to $15$ V)	$V_{FBline-reg}$	–10	–	10	mV
Output Current Sink ( $V_{E/A\ out} = 1.5$ V, $V_{FB} = 2.7$ V) $T_A = -25^\circ$ to $+85^\circ\text{C}$ Source ( $V_{E/A\ out} = 5.0$ V, $V_{FB} = 2.3$ V) $T_A = -25^\circ$ to $+85^\circ\text{C}$	$I_{Sink}$ $I_{Source}$	2.0 –2.0	12 –	– –0.2	mA
Output Voltage Swing High State ( $I_{E/A\ out (source)} = 0.5$ mA, $V_{FB} = 2.3$ V) Low State ( $I_{E/A\ out (sink)} = 0.33$ mA, $V_{FB} = 2.7$ V)	$V_{OH}$ $V_{OL}$	5.5 –	6.5 1.0	7.5 1.1	V

## REFERENCE SECTION

Reference Output Voltage ( $V_{CC} = 10$ to $15$ V)	$V_{ref}$	2.4	2.5	2.6	V
Reference Current Range ( $I_{ref} = V_{ref}/R_{ref}$ , $R = 5.0$ k to $25$ k $\Omega$ )	$I_{ref}$	–500	–	–100	$\mu\text{A}$
Reference Voltage Over $I_{ref}$ Range	$\Delta V_{ref}$	–40	–	40	mV

## OSCILLATOR AND SYNCHRONIZATION SECTION

Frequency $T_A = 0^\circ$ to $+70^\circ\text{C}$ $T_A = -25^\circ$ to $+85^\circ\text{C}$	$f_{OSC}$	44.5 44	48 –	51.5 52	kHz
Frequency Change with Voltage ( $V_{CC} = 10$ to $15$ V)	$\Delta f_{OSC}/\Delta V$	–	0.05	–	%/V

- Adjust  $V_{CC}$  above the startup threshold before setting to  $12$  V.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
- $V_C$  must be greater than  $5.0$  V.
- Standby is disabled for  $V_{R\ P\ Stby} < 25$  mV typical.
- If not used, Synchronization input must be connected to Ground.
- Synchronization Pulse Width must be shorter than  $t_{OSC} = 1/f_{OSC}$ .
- This function can be inhibited by connecting Pin 8 to GND. This allows a continuous current mode operation.
- This function can be inhibited by connecting Pin 5 to  $V_{CC}$ .
- The MC44603A can be shut down by connecting the Soft-Start pin (Pin 11) to Ground.

# MC44603A

**ELECTRICAL CHARACTERISTICS** (continued) ( $V_{CC}$  and  $V_C = 12$  V, (Note 3),  $R_{ref} = 10$  k $\Omega$ ,  $C_T = 820$  pF, for typical values  $T_A = 25^\circ\text{C}$ , for min/max values  $T_A = -25^\circ$  to  $+85^\circ\text{C}$  (Note 4), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

## OSCILLATOR AND SYNCHRONIZATION SECTION

Frequency Change with Temperature ( $T_A = -25^\circ$ to $+85^\circ\text{C}$ )	$\Delta f_{OSC}/\Delta T$	–	0.05	–	%/ $^\circ\text{C}$
Oscillator Voltage Swing (Peak-to-Peak)	$V_{OSC(pp)}$	1.65	1.8	1.95	V
Ratio Charge Current/Reference Current $T_A = 0^\circ$ to $+70^\circ\text{C}$ ( $V_{CT} = 2.0$ V) $T_A = -25^\circ$ to $+85^\circ\text{C}$	$I_{charge}/I_{ref}$	0.375 0.37	0.4 –	0.425 0.43	–
Fixed Maximum Duty Cycle = $I_{discharge}/(I_{discharge} + I_{charge})$	D	78	80	82	%
Ratio Standby Discharge Current versus $I_{RF Stby}$ (Note 6) $T_A = 0^\circ$ to $+70^\circ\text{C}$ $T_A = -25^\circ$ to $+85^\circ\text{C}$ (Note 8)	$I_{disch-Stby}/I_{RF Stby}$	0.46 0.43	0.53 –	0.6 0.63	–
$V_{RF Stby}$ ( $I_{RF Stby} = 100$ $\mu\text{A}$ )	$V_{RF Stby}$	2.4	2.5	2.6	V
Frequency in Standby Mode ( $R_{F Stby}$ (Pin 15) = 25 k $\Omega$ )	$F_{Stby}$	18	21	24	kHz
Current Range	$I_{RF Stby}$	–200	–	–50	$\mu\text{A}$
Synchronization Input Threshold Voltage (Note 7)	$V_{inthH}$ $V_{inthL}$	3.2 0.45	3.7 0.7	4.3 0.9	V
Synchronization Input Current	$I_{Sync-in}$	–5.0	–	0	$\mu\text{A}$
Minimum Synchronization Pulse Width (Note 8)	$t_{Sync}$	–	–	0.5	$\mu\text{s}$

## UNDERVOLTAGE LOCKOUT SECTION

Startup Threshold	$V_{stup-th}$	13.6	14.5	15.4	V
Output Disable Voltage After Threshold Turn-On (UVLO 1) $T_A = 0^\circ$ to $+70^\circ\text{C}$ $T_A = -25^\circ$ to $+85^\circ\text{C}$	$V_{disable1}$	8.6 8.3	9.0 –	9.4 9.6	V
Reference Disable Voltage After Threshold Turn-On (UVLO 2)	$V_{disable2}$	7.0	7.5	8.0	V

## DEMAGNETIZATION DETECTION SECTION (Note 9)

Demagnetization Detect Input Demagnetization Comparator Threshold ( $V_{Pin 9}$ Decreasing) Propagation Delay (Input to Output, Low to High) Input Bias Current ( $V_{demag} = 65$ mV)	$V_{demag-th}$ – $I_{demag-lb}$	50 – –0.5	65 0.25 –	80 – –	mV $\mu\text{s}$ $\mu\text{A}$
Negative Clamp Level ( $I_{demag} = -2.0$ mA)	$C_{L(neg)}$	–	–0.38	–	V
Positive Clamp Level ( $I_{demag} = 2.0$ mA)	$C_{L(pos)}$	–	0.72	–	V

## SOFT-START SECTION (Note 11)

Ratio Charge Current/ $I_{ref}$ $T_A = 0^\circ$ to $+70^\circ\text{C}$ $T_A = -25^\circ$ to $+85^\circ\text{C}$	$I_{ss(ch)}/I_{ref}$	0.37 0.36	0.4 –	0.43 0.44	–
Discharge Current ( $V_{soft-start} = 1.0$ V)	$I_{discharge}$	1.5	5.0	–	mA
Clamp Level	$V_{ss(CL)}$	2.2	2.4	2.6	V

- Adjust  $V_{CC}$  above the startup threshold before setting to 12 V.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
- $V_C$  must be greater than 5.0 V.
- Standby is disabled for  $V_{RP Stby} < 25$  mV typical.
- If not used, Synchronization input must be connected to Ground.
- Synchronization Pulse Width must be shorter than  $t_{OSC} = 1/f_{OSC}$ .
- This function can be inhibited by connecting Pin 8 to GND. This allows a continuous current mode operation.
- This function can be inhibited by connecting Pin 5 to  $V_{CC}$ .
- The MC44603A can be shut down by connecting the Soft-Start pin (Pin 11) to Ground.

# MC44603A

**ELECTRICAL CHARACTERISTICS** (continued) ( $V_{CC}$  and  $V_C = 12$  V, (Note 3),  $R_{ref} = 10$  k $\Omega$ ,  $C_T = 820$  pF, for typical values  $T_A = 25^\circ\text{C}$ , for min/max values  $T_A = -25^\circ$  to  $+85^\circ\text{C}$  (Note 4), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

## SOFT-START SECTION (Note 11)

Duty Cycle ( $R_{\text{soft-start}} = 12$ k $\Omega$ ) ( $V_{\text{soft-start}}(\text{Pin } 11) = 0.1$ V)	$D_{\text{soft-start } 12k}$ $D_{\text{soft-start}}$	36 –	42 –	49 0	%
--	---	---------	---------	---------	---

## OVERVOLTAGE SECTION

Protection Threshold Level on $V_{OVP}$	$V_{OVP-th}$	2.42	2.5	2.58	V
Propagation Delay ( $V_{OVP} > 2.58$ V to $V_{out}$ Low)		1.0	–	3.0	$\mu\text{s}$
Protection Level on $V_{CC}$ $T_A = 0^\circ$ to $+70^\circ\text{C}$ $T_A = -25^\circ$ to $+85^\circ\text{C}$	$V_{CC\text{ prot}}$	16.1 15.9	17 –	17.9 18.1	V
Input Resistance $T_A = 0^\circ$ to $+70^\circ\text{C}$ $T_A = -25^\circ$ to $+85^\circ\text{C}$	–	1.5 1.4	2.0 –	3.0 3.4	k $\Omega$

## FOLDBACK SECTION (Note 10)

Current Sense Voltage Threshold ( $V_{\text{foldback}}(\text{Pin } 5) = 0.9$ V)	$V_{CS-th}$	0.86	0.89	0.9	V
Foldback Input Bias Current ( $V_{\text{foldback}}(\text{Pin } 5) = 0$ V)	$I_{\text{foldback-ib}}$	–6.0	–2.0	–	$\mu\text{A}$

## STANDBY SECTION

Ratio $I_{R\text{ P Stby}}/I_{ref}$ $T_A = 0^\circ$ to $+70^\circ\text{C}$ $T_A = -25^\circ$ to $+85^\circ\text{C}$	$I_{R\text{ P Stby}}/I_{ref}$	0.37 0.36	0.4 –	0.43 0.44	–
Ratio Hysteresis ( $V_h$ Required to Return to Normal Operation from Standby Operation) $T_A = 0^\circ$ to $+70^\circ\text{C}$ $T_A = -25^\circ$ to $+85^\circ\text{C}$	$V_h/V_{R\text{ P Stby}}$	1.42 1.4	1.5 –	1.58 1.6	–
Current Sense Voltage Threshold ( $V_{R\text{ P Stby}}(\text{Pin } 12) = 1.0$ V)	$V_{CS-Stby}$	0.28	0.31	0.34	V

## CURRENT SENSE SECTION

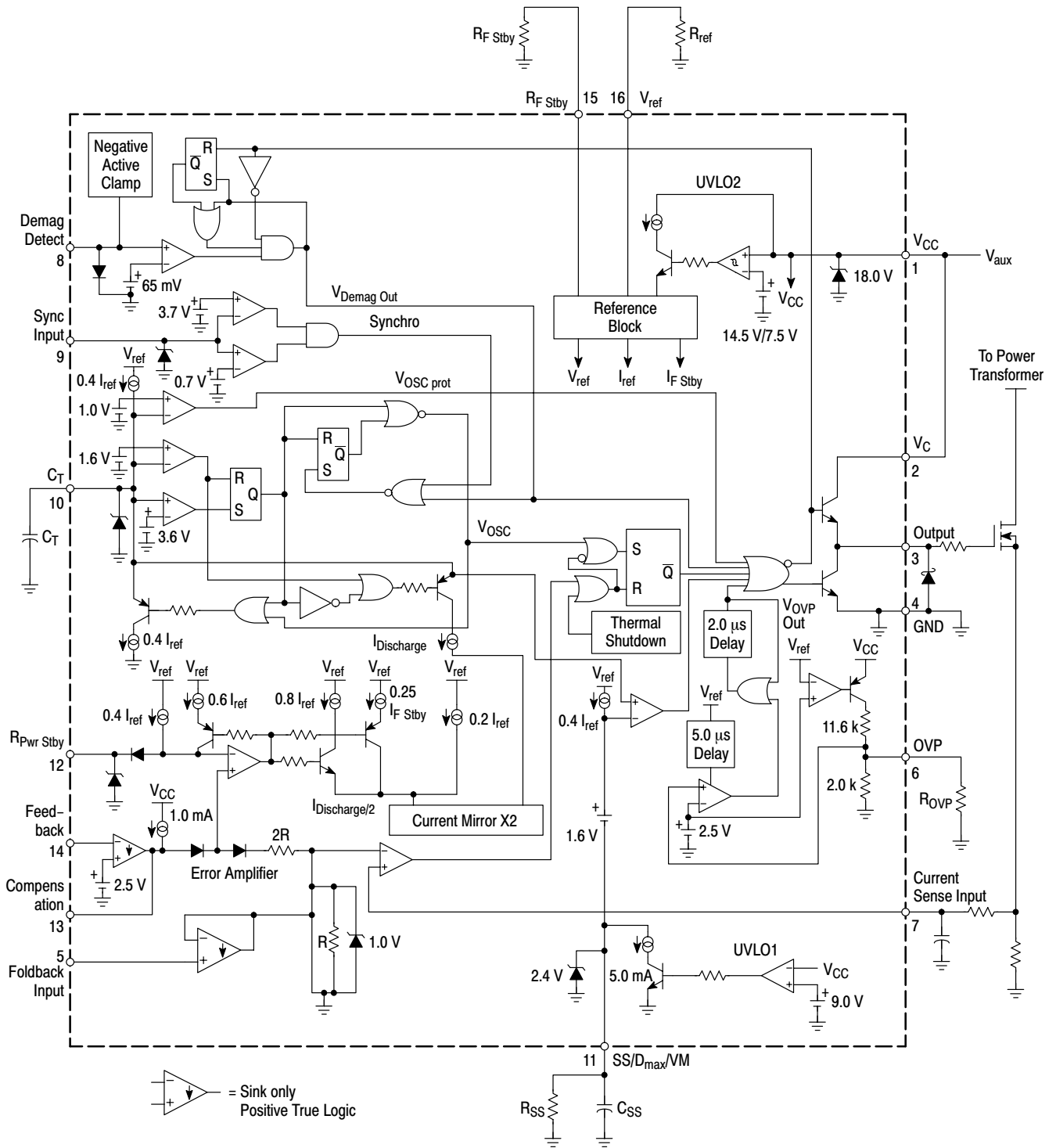
Maximum Current Sense Input Threshold ( $V_{\text{feedback}}(\text{Pin } 14) = 2.3$ V and $V_{\text{foldback}}(\text{Pin } 6) = 1.2$ V)	$V_{CS-th}$	0.96	1.0	1.04	V
Input Bias Current	$I_{CS-ib}$	–10	–2.0	–	$\mu\text{A}$
Propagation Delay (Current Sense Input to Output at $V_{TH}$ of MOS transistor = 3.0 V)	–	–	120	200	ns

## TOTAL DEVICE

Power Supply Current Startup ( $V_{CC} = 13$ V with $V_{CC}$ Increasing) Operating $T_A = -25^\circ$ to $+85^\circ\text{C}$ (Note 3)	$I_{CC}$	– 13	0.3 17	0.45 20	mA
Power Supply Zener Voltage ( $I_{CC} = 25$ mA)	$V_Z$	18.5	–	–	V
Thermal Shutdown	–	–	155	–	$^\circ\text{C}$

- Adjust  $V_{CC}$  above the startup threshold before setting to 12 V.
- Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
- $V_C$  must be greater than 5.0 V.
- Standby is disabled for  $V_{R\text{ P Stby}} < 25$  mV typical.
- If not used, Synchronization input must be connected to Ground.
- Synchronization Pulse Width must be shorter than  $t_{OSC} = 1/f_{OSC}$ .
- This function can be inhibited by connecting Pin 8 to GND. This allows a continuous current mode operation.
- This function can be inhibited by connecting Pin 5 to  $V_{CC}$ .
- The MC44603A can be shut down by connecting the Soft-Start pin (Pin 11) to Ground.

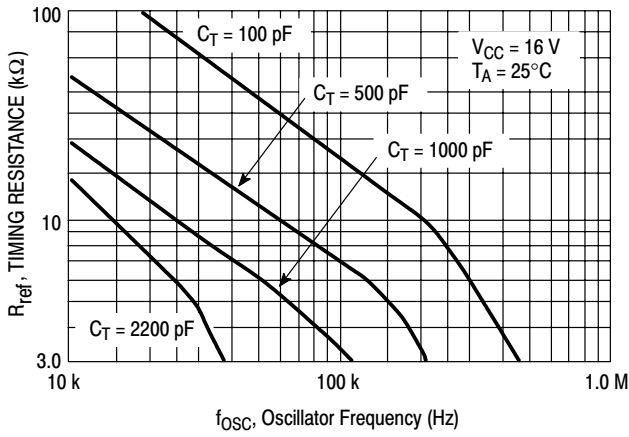
# MC44603A



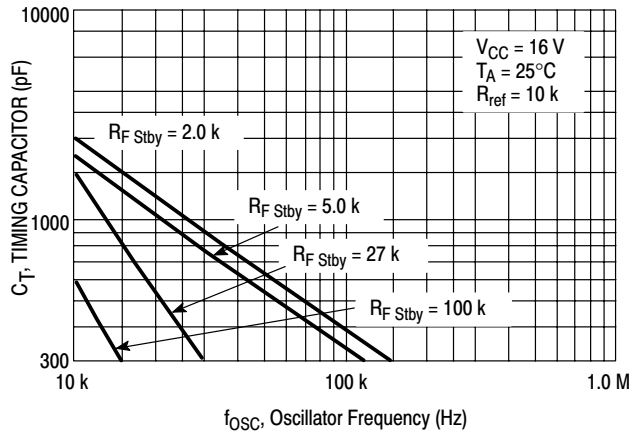
This device contains 243 active transistors.

**Figure 1. Representative Block Diagram**

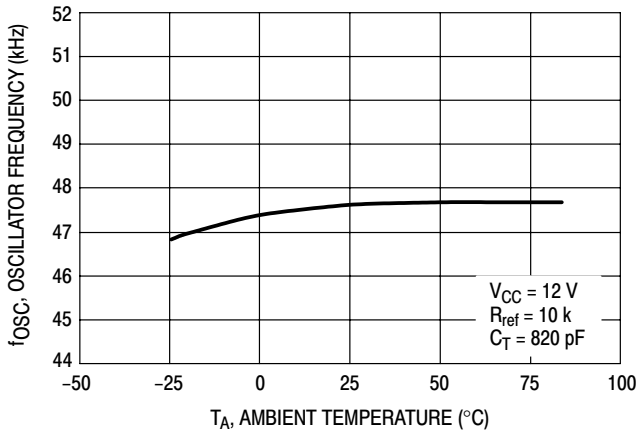
# MC44603A



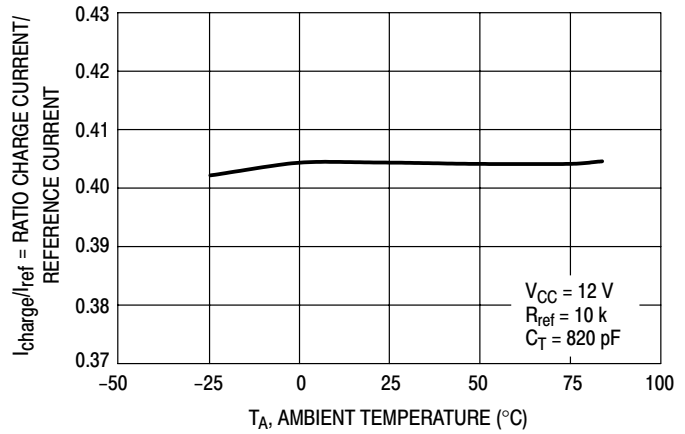
**Figure 2. Timing Resistor versus Oscillator Frequency**



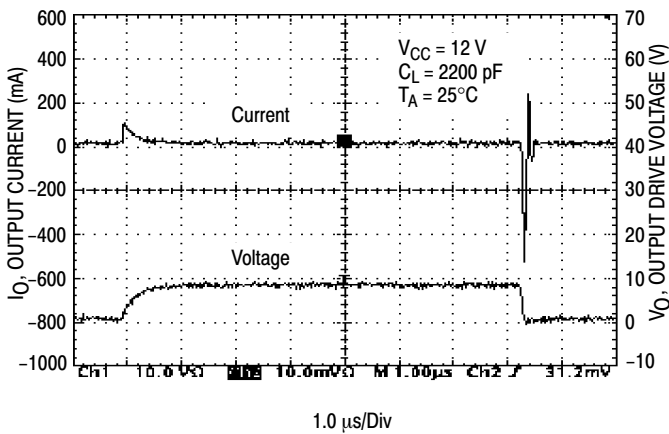
**Figure 3. Standby Mode Timing Capacitor versus Oscillator Frequency**



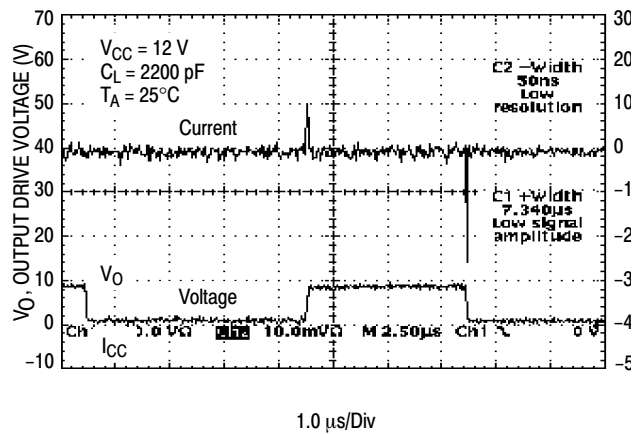
**Figure 4. Oscillator Frequency versus Temperature**



**Figure 5. Ratio Charge Current/Reference Current versus Temperature**



**Figure 6. Output Waveform**



**Figure 7. Output Cross Conduction**

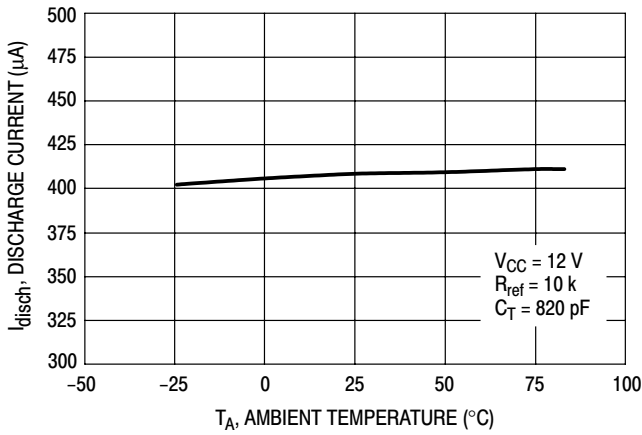


Figure 8. Oscillator Discharge Current versus Temperature

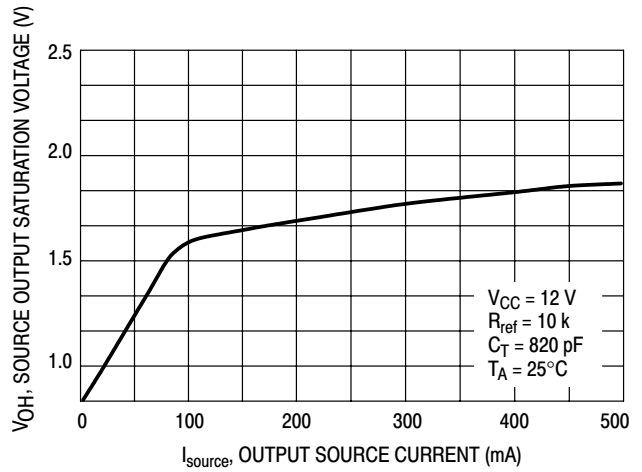


Figure 9. Source Output Saturation Voltage versus Load Current

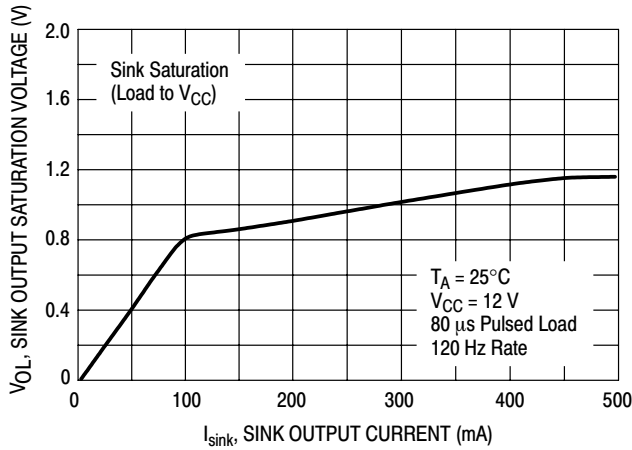


Figure 10. Sink Output Saturation Voltage versus Sink Current

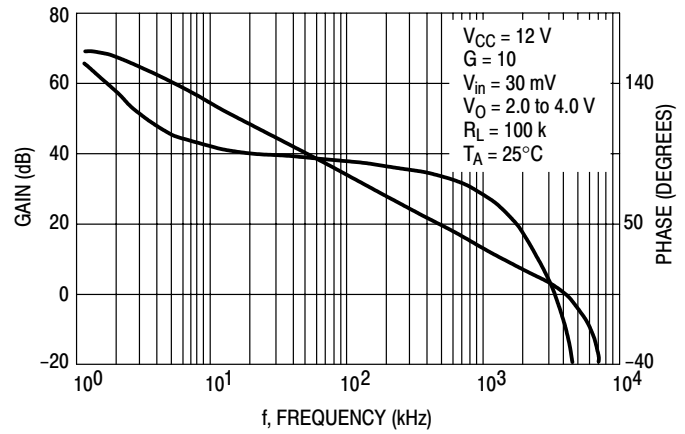


Figure 11. Error Amplifier Gain and Phase versus Frequency

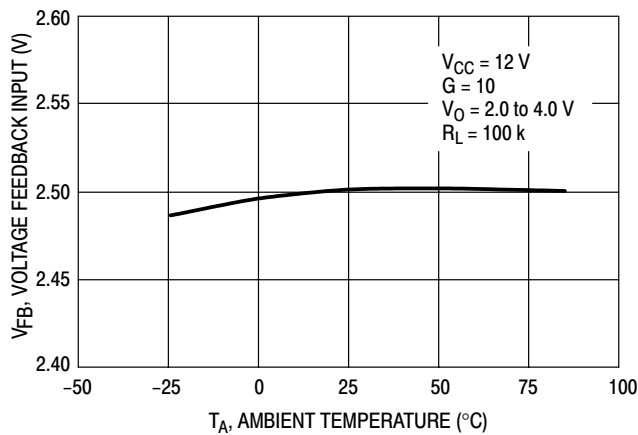


Figure 12. Voltage Feedback Input versus Temperature

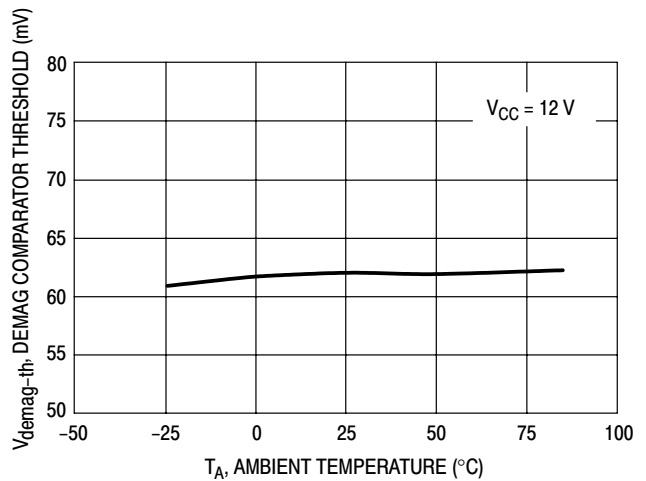


Figure 13. Demag Comparator Threshold versus Temperature



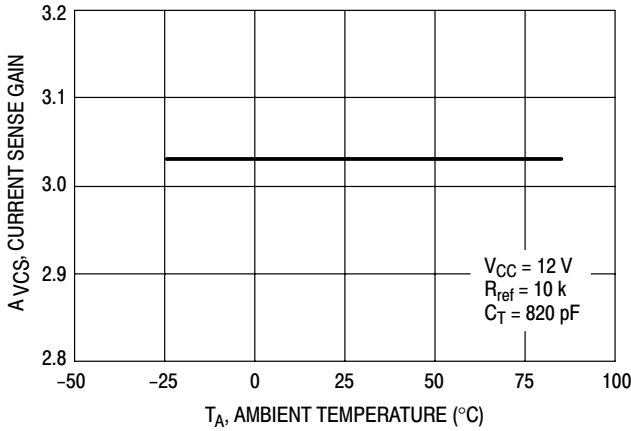


Figure 14. Current Sense Gain versus Temperature

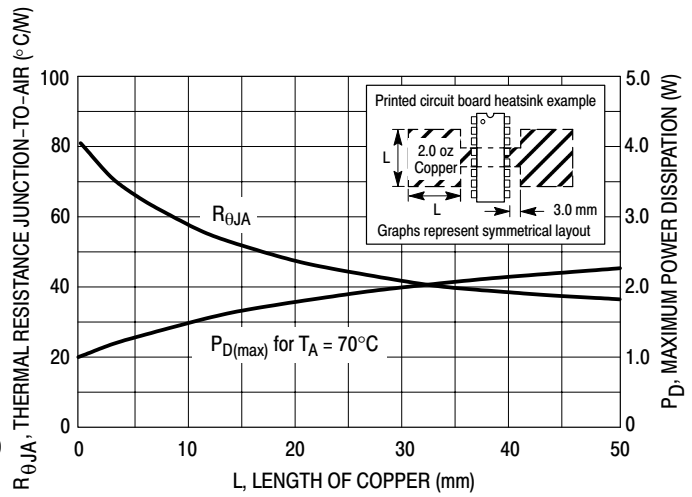


Figure 15. Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

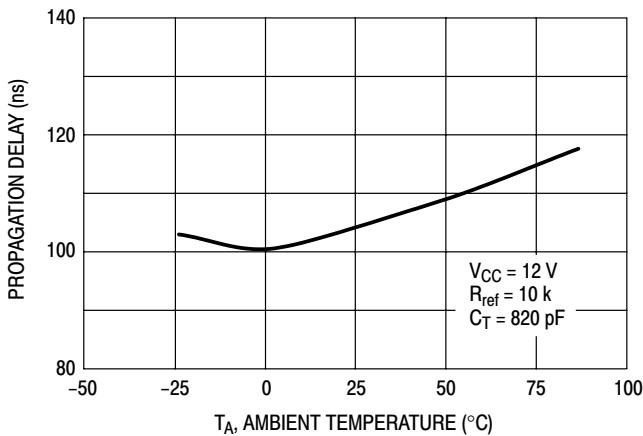


Figure 16. Propagation Delay Current Sense Input to Output versus Temperature

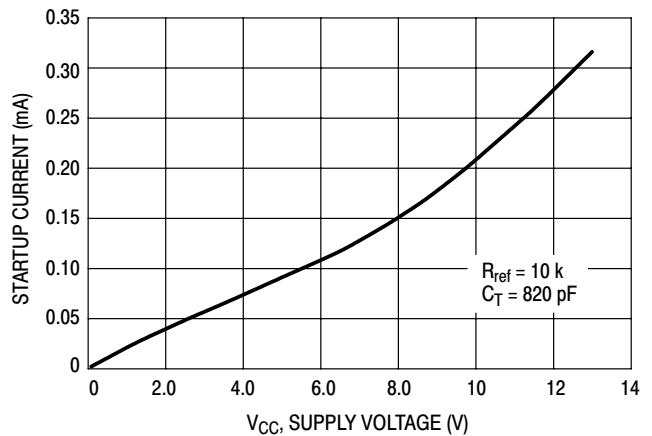


Figure 17. Startup Current versus VCC

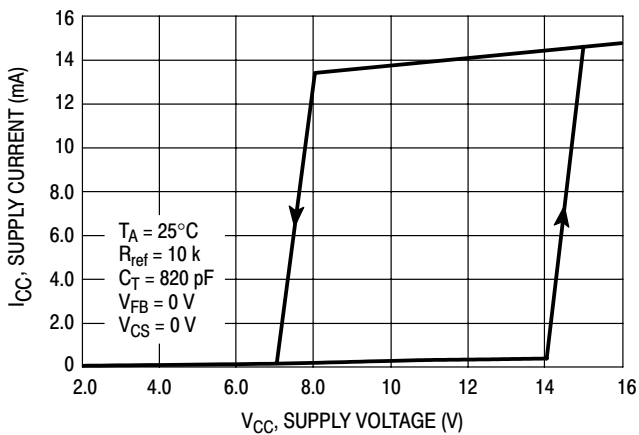


Figure 18. Supply Current versus Supply Voltage

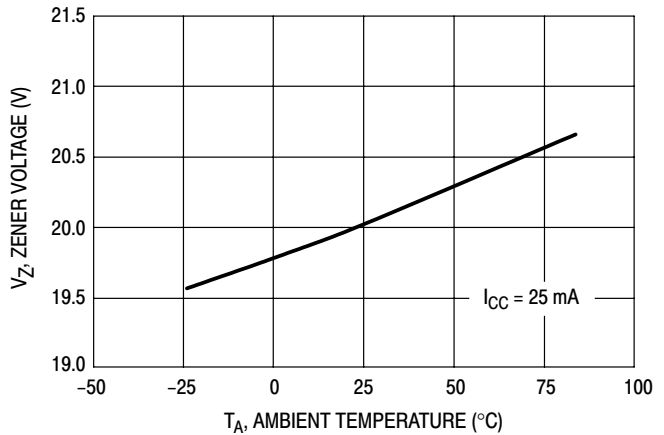


Figure 19. Power Supply Zener Voltage versus Temperature

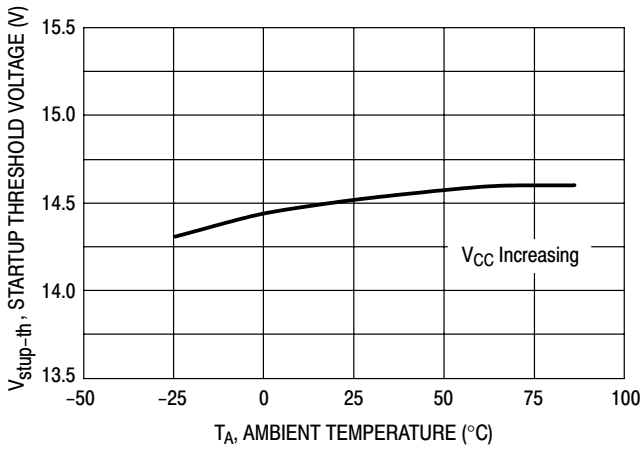


Figure 20. Startup Threshold Voltage versus Temperature

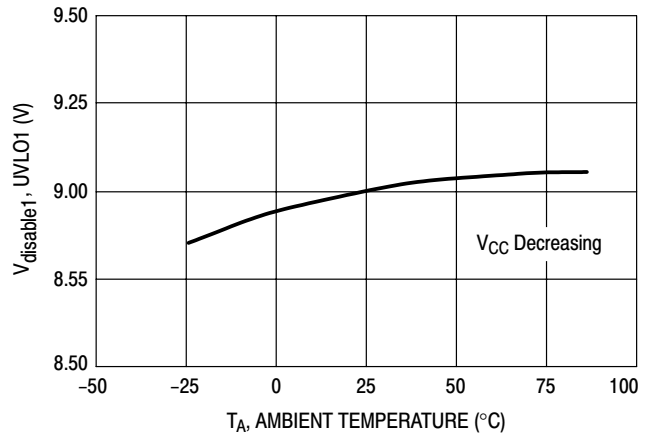


Figure 21. Disable Voltage After Threshold Turn-On (UVLO1) versus Temperature

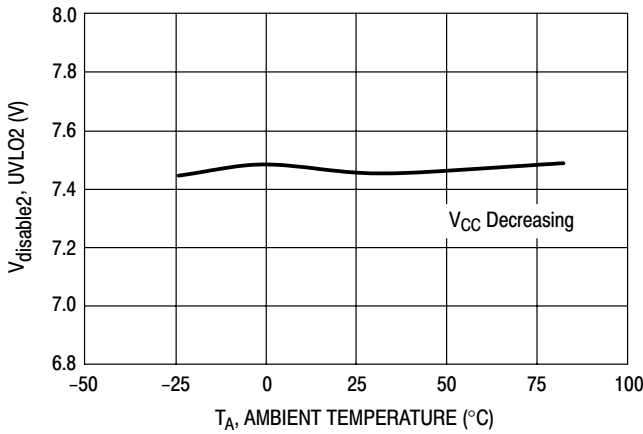


Figure 22. Disable Voltage After Threshold Turn-On (UVLO2) versus Temperature

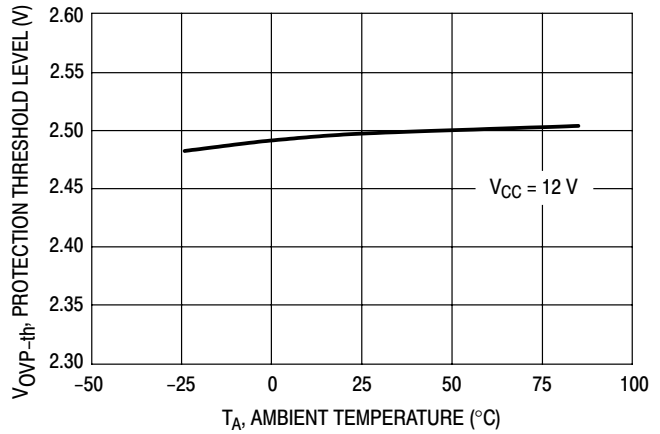


Figure 23. Protection Threshold Level on  $V_{OVP}$  versus Temperature

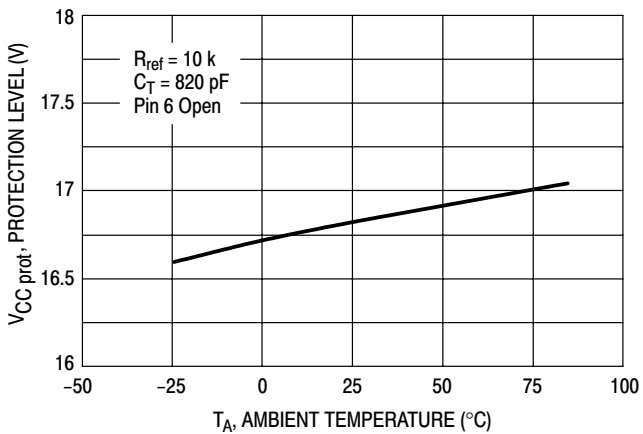


Figure 24. Protection Level on  $V_{CC}$  versus Temperature

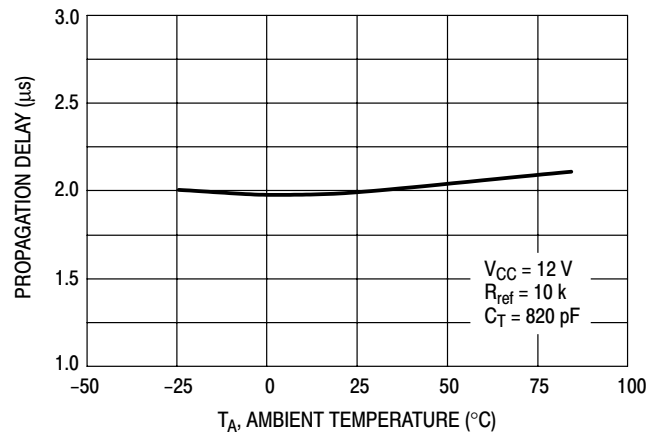


Figure 25. Propagation Delay ( $V_{OVP} > 2.58 V$  to  $V_{out}$  Low) versus Temperature

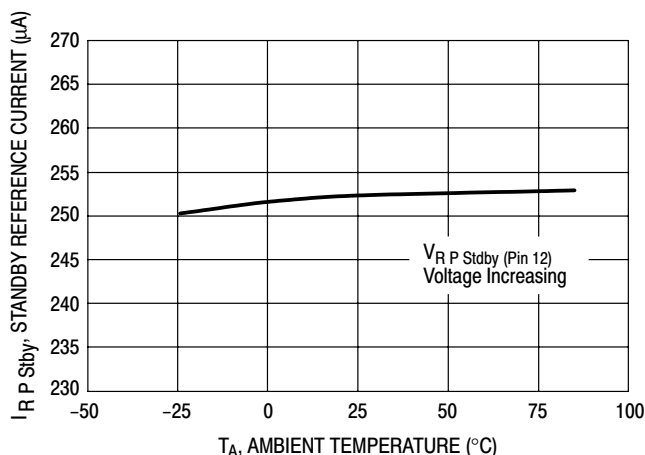


Figure 26. Standby Reference Current versus Temperature

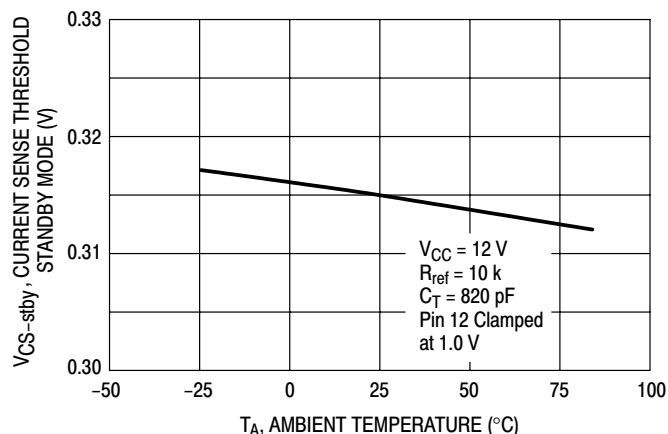


Figure 27. Current Sense Voltage Threshold Standby Mode versus Temperature

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	V <sub>CC</sub>	This pin is the positive supply of the IC. The operating voltage range after startup is 9.0 to 14.5 V.
2	V <sub>C</sub>	The output high state (V <sub>OH</sub> ) is set by the voltage applied to this pin. With a separate connection to the power source, it can reduce the effects of switching noise on the control circuitry.
3	Output	Peak currents up to 750 mA can be sourced or sunk, suitable for driving either MOSFET or Bipolar transistors. This output pin must be shunted by a Schottky diode, 1N5819 or equivalent.
4	GND	The ground pin is a single return, typically connected back to the power source; it is used as control and power ground.
5	Foldback Input	The foldback function provides overload protection. Feeding the foldback input with a portion of the V <sub>CC</sub> voltage (1.0 V max) establishes on the system control loop a foldback characteristic allowing a smoother startup and sharper overload protection. Above 1.0 V the foldback input is inactive.
6	Overshoot Protection	When the overshoot protection pin receives a voltage greater than 17 V, the device is disabled and requires a complete restart sequence. The overshoot level is programmable.
7	Current Sense Input	A voltage proportional to the current flowing into the power switch is connected to this input. The PWM latch uses this information to terminate the conduction of the output buffer when working in a current mode of operation. A maximum level of 1.0 V allows either current or voltage mode operation.
8	Demagnetization Detection	A voltage delivered by an auxiliary transformer winding provides to the demagnetization pin an indication of the magnetization state of the flyback transformer. A zero voltage detection corresponds to complete core saturation. The demagnetization detection ensures a discontinuous mode of operation. This function can be inhibited by connecting Pin 8 to GND.
9	Synchronization Input	The synchronization input pin can be activated with either a negative pulse going from a level between 0.7 V and 3.7 V to GND or a positive pulse going from a level between 0.7 V and 3.7 V up to a level higher than 3.7 V. The oscillator runs free when Pin 9 is connected to GND.
10	C <sub>T</sub>	The normal mode oscillator frequency is programmed by the capacitor C <sub>T</sub> choice together with the R <sub>ref</sub> resistance value. C <sub>T</sub> , connected between Pin 10 and GND, generates the oscillator sawtooth.
11	Soft-Start/D <sub>max</sub> /Voltage-Mode	A capacitor, resistor or a voltage source connected to this pin limits the switching duty-cycle. This pin can be used as a voltage mode control input. By connecting Pin 11 to Ground, the MC44603A can be shut down.
12	R <sub>P Standby</sub>	A voltage level applied to the R <sub>P Standby</sub> pin determines the output power level at which the oscillator will turn into the reduced frequency mode of operation (i.e. standby mode). An internal hysteresis comparator allows to return in the normal mode at a higher output power level.
13	E/A Out	The error amplifier output is made available for loop compensation.
14	Voltage Feedback	This is the inverting input of the Error Amplifier. It can be connected to the switching power supply output through an optical (or other) feedback loop.
15	R <sub>F Standby</sub>	The reduced frequency or standby frequency programming is made by the R <sub>F Standby</sub> resistance choice.
16	R <sub>ref</sub>	R <sub>ref</sub> sets the internal reference current. The internal reference current ranges from 100 µA to 500 µA. This requires that 5.0 kΩ ≤ R <sub>ref</sub> ≤ 25 kΩ.

# MC44603A

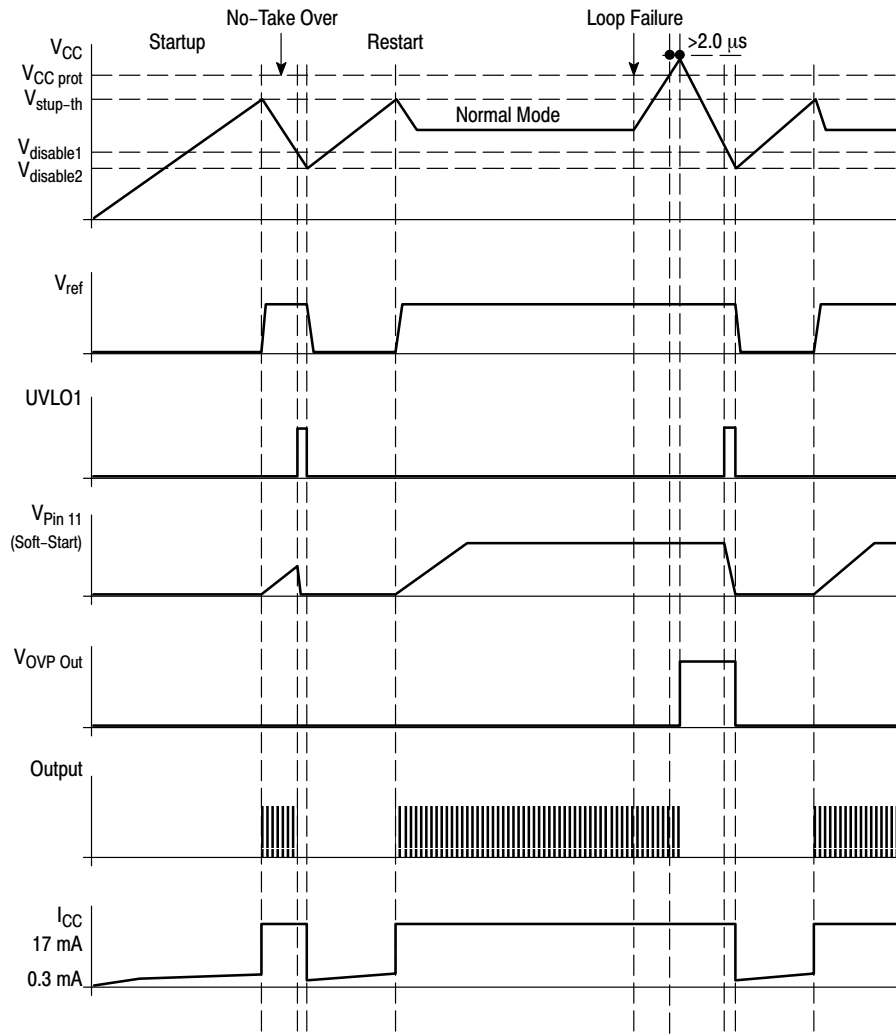


Figure 28. Starting Behavior and Overvoltage Management

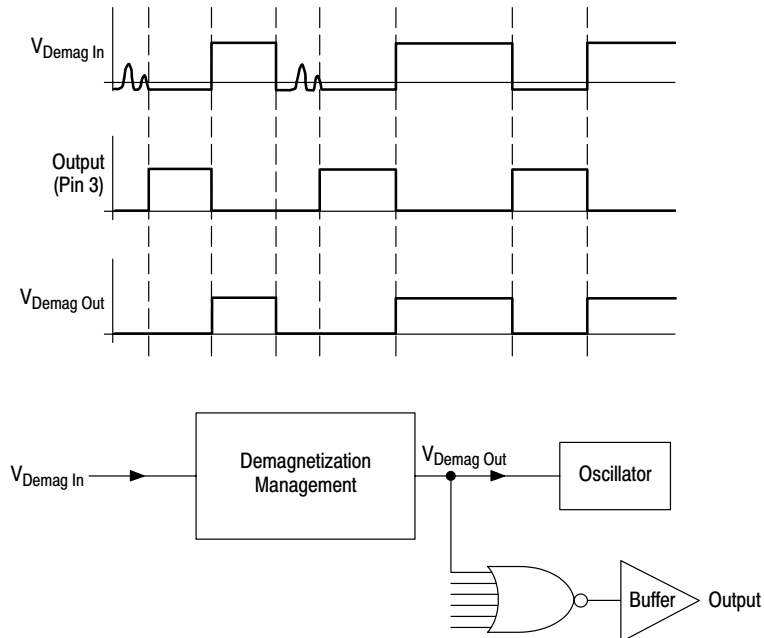
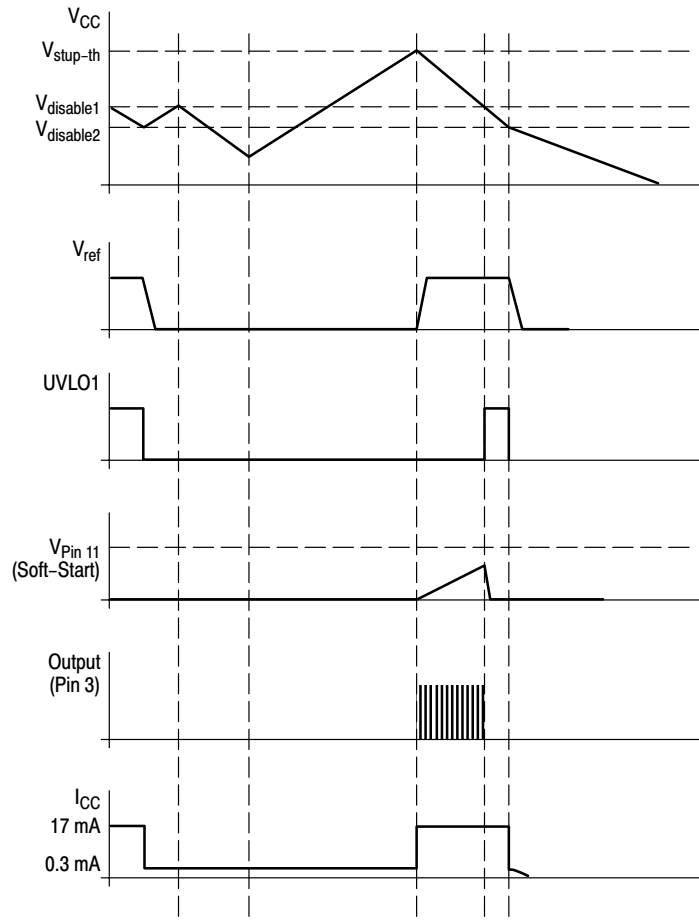
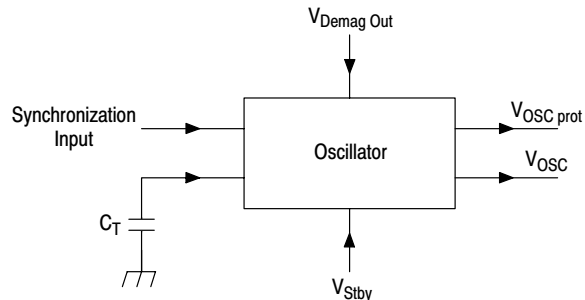
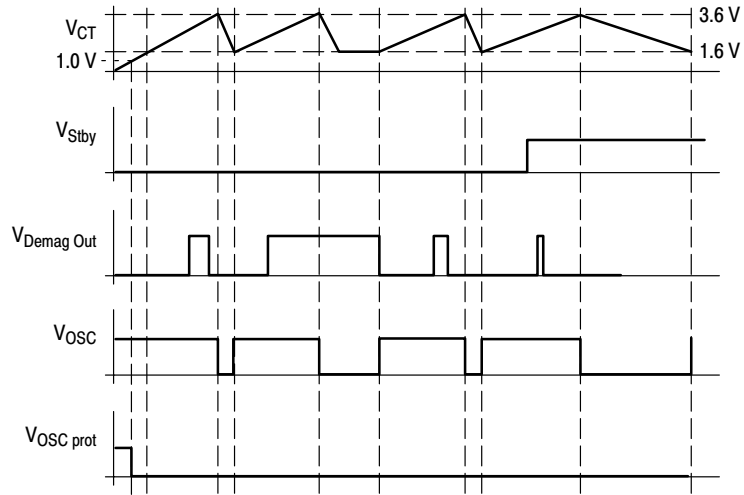


Figure 29. Demagnetization

# MC44603A



**Figure 30. Switching Off Behavior**



**Figure 31. Oscillator**

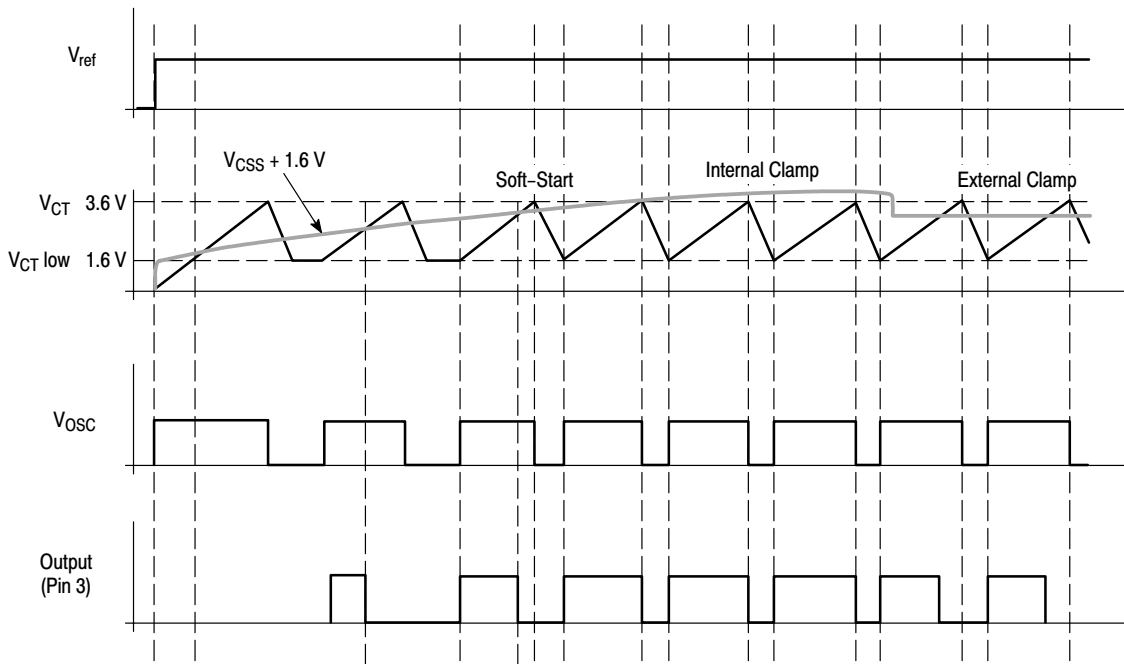


Figure 32. Soft-Start & D<sub>max</sub>

OPERATING DESCRIPTION

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 70 dB. The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current with the inverting input at 2.5 V is -2.0 μA. This can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp output (Pin 13) is provided for external loop compensation. The output voltage is offset by two diode drops (≈ 1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 3) when Pin 13 is at its lowest state (V<sub>OL</sub>). The Error Amp minimum feedback resistance is limited by the amplifier’s minimum source current (0.2 mA) and the required output voltage (V<sub>OH</sub>) to reach the current sense comparator’s 1.0 V clamp level:

$$R_{f(\min)} \approx \frac{3.0 (1.0 \text{ V}) + 1.4 \text{ V}}{0.2 \text{ mA}} = 22 \text{ k}\Omega$$

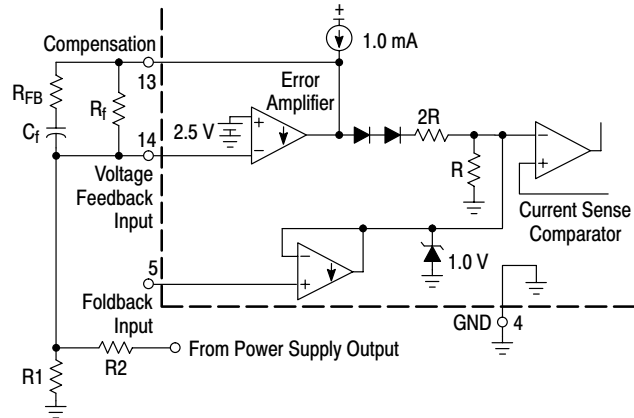


Figure 33. Error Amplifier Compensation

Current Sense Comparator and PWM Latch

The MC44603A can operate as a current mode controller or as a voltage mode controller. In current mode operation, the MC44603A uses the current sense comparator. The output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the

threshold level established by the Error Amplifier output (Pin 13). Thus, the error signal controls the peak inductor current on a cycle-by-cycle basis. The Current Sense Comparator PWM Latch ensures that only a single pulse appears at the Source Output during the appropriate oscillator cycle.

The inductor current is converted to a voltage by inserting the ground referenced sense resistor  $R_S$  in series with the power switch Q1.

This voltage is monitored by the Current Sense Input (Pin 7) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 13 where:

$$I_{pk} \approx \frac{V(\text{Pin 13}) - 1.4 \text{ V}}{3 R_S}$$

The Current Sense Comparator threshold is internally clamped to 1.0 V. Therefore, the maximum peak switch current is:

$$I_{pk(\text{max})} \approx \frac{1.0 \text{ V}}{R_S}$$

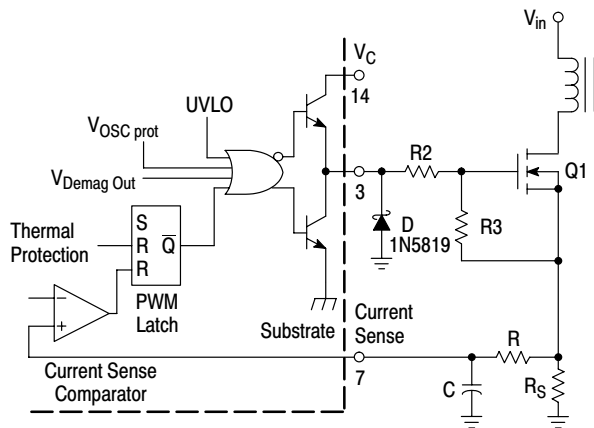


Figure 34. Output Totem Pole

Series gate resistor, R2, will dampen any high frequency oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit. Diode D is required if the negative current into the output drive pin exceeds 15 mA.

**Oscillator**

The oscillator is a very accurate sawtooth generator that can work either in free mode or in synchronization mode. In this second mode, the oscillator stops in the low state and waits for a demagnetization or a synchronization pulse to start a new charging cycle.

• **The Sawtooth Generation:**

In the steady state, the oscillator voltage varies between about 1.6 V and 3.6 V.

The sawtooth is obtained by charging and discharging an external capacitor  $C_T$  (Pin 10), using two distinct current sources =  $I_{\text{charge}}$  and  $I_{\text{discharge}}$ . In fact,  $C_T$  is permanently

connected to the charging current source ( $0.4 I_{\text{ref}}$ ) and so, the discharge current source has to be higher than the charge current to be able to decrease the  $C_T$  voltage (refer to Figure 36).

This condition is performed, its value being ( $2.0 I_{\text{ref}}$ ) in normal working and ( $0.4 I_{\text{ref}} + 0.5 I_{\text{F Stby}}$  in standby mode).

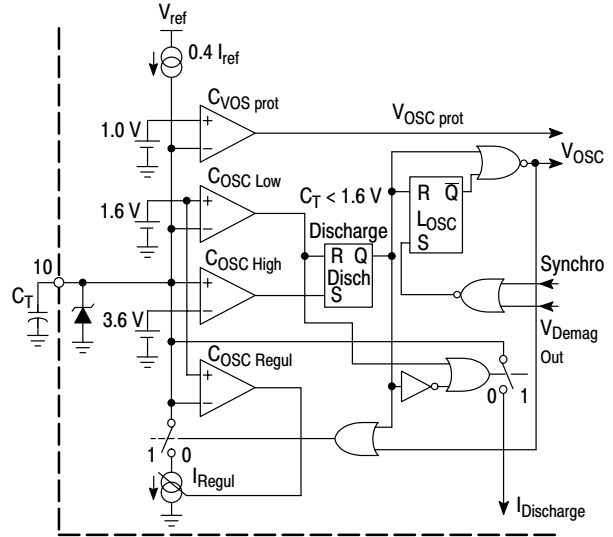


Figure 35. Oscillator

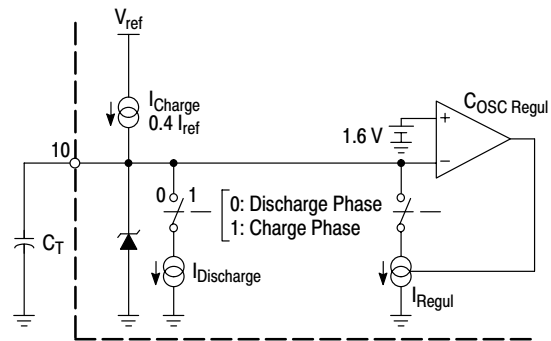


Figure 36. Simplified Block Oscillator

Two comparators are used to generate the sawtooth. They compare the  $C_T$  voltage to the oscillator valley (1.6 V) and peak reference (3.6 V) values. A latch ( $L_{\text{disch}}$ ) memorizes the oscillator state.

In addition to the charge and discharge cycles, a third state can exist. This phase can be produced when, at the end of the discharge phase, the oscillator has to wait for a synchronization or demagnetization pulse before restarting. During this delay, the  $C_T$  voltage must remain equal to the oscillator valley value ( $\approx 1.6 \text{ V}$ ). So, a third regulated current source  $I_{\text{Regul}}$  controlled by  $C_{\text{OSC Regul}}$ , is connected to  $C_T$  in order to perfectly compensate the ( $0.4 I_{\text{ref}}$ ) current source that permanently supplies  $C_T$ .

The maximum duty cycle is 80%. Indeed, the on-time is allowed only during the oscillator capacitor charge.

Consequently:

$$T_{\text{charge}} = C_T \times \Delta V / I_{\text{charge}}$$

$$T_{\text{discharge}} = C_T \times \Delta V / I_{\text{discharge}}$$

where:

$T_{\text{charge}}$  is the oscillator charge time

$\Delta V$  is the oscillator peak-to-peak value

$I_{\text{charge}}$  is the oscillator charge current

and

$T_{\text{discharge}}$  is the oscillator discharge time

$I_{\text{discharge}}$  is the oscillator discharge current

So, as  $f_S = 1 / (T_{\text{charge}} + T_{\text{discharge}})$  when the Regul arrangement is not activated, the operating frequency can be obtained from the graph in Figure 2.

**NOTE:** The output is disabled by the signal  $V_{\text{OSC prot}}$  when  $V_{\text{CT}}$  is lower than 1.0 V (refer to Figure 31).

**Synchronization and Demagnetization Blocks**

To enable the output, the  $L_{\text{OSC}}$  latch complementary output must be low. Reset is activated by the  $L_{\text{disch}}$  output during the discharge phase. To restart, the  $L_{\text{OSC}}$  has to be set (refer to Figure 35). To perform this, the demagnetization signal and the synchronization must be low.

• **Synchronization:**

The synchronization block consists of two comparators that compare the synchronization signal (external) to 0.7 and 3.7 V (typical values). The comparators' outputs are connected to the input of an AND gate so that the final output of the block should be:

- high when  $0.7 < \text{SYNC} < 3.7 \text{ V}$
- low in the other cases.

As a low level is necessary to enable the output, synchronized low level pulses have to be generated on the output of the synchronization block. If synchronization is not required, the Pin 9 must be connected to the ground.

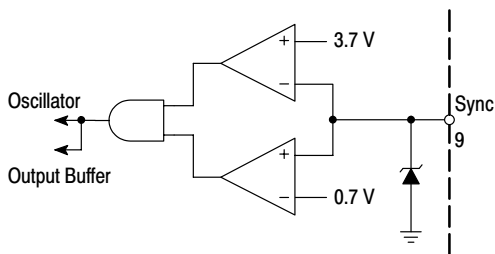


Figure 37. Synchronization

• **Demagnetization:**

In flyback applications, a good means to detect magnetic saturation of the transformer core, or demagnetization, consists in using the auxiliary winding voltage. This voltage is:

- negative during the on-time,
- positive during the off-time,
- equal to zero for the dead-time with generally some ringing (refer to Figure 38).

That is why, the MC44603A demagnetization detection consists of a comparator that can compare the auxiliary winding voltage to a reference that is typically equal to 65 mV.

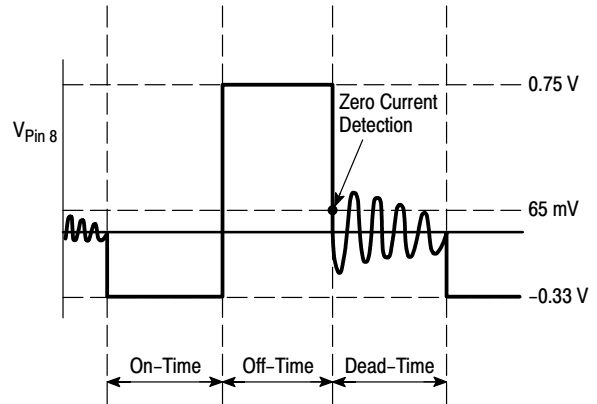


Figure 38. Demagnetization Detection

A diode D has been incorporated to clamp the positive applied voltages while an active clamping system limits the negative voltages to typically -0.33 V. This negative clamp level is sufficient to avoid the substrate diode switching on.

In addition to the comparator, a latch system has been incorporated in order to keep the demagnetization block output level low as soon as a voltage lower than 65 mV is detected and as long as a new restart is produced (high level on the output) (refer to Figure 39). This process prevents ringing on the signal at Pin 8 from disrupting the demagnetization detection. This results in a very accurate demagnetization detection.

The demagnetization block output is also directly connected to the output, disabling it during the demagnetization phase (refer to Figure 34).

**NOTE:** The demagnetization detection can be inhibited by connecting Pin 8 to the ground.

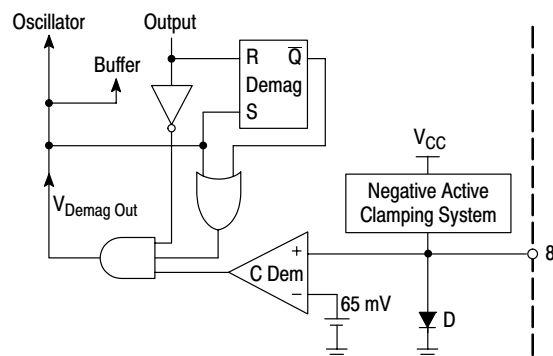
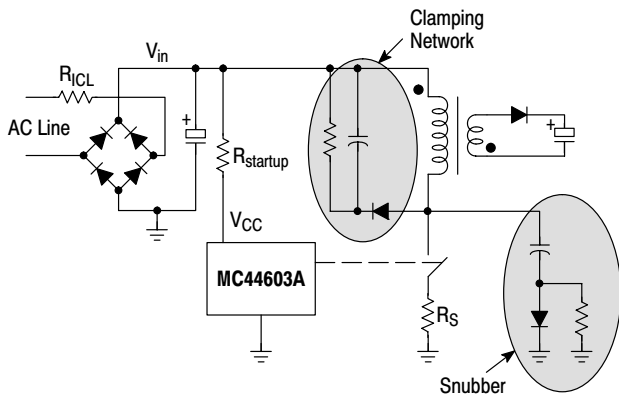


Figure 39. Demagnetization Block

**Standby**

• **Power Losses in a Classical Flyback Structure**





**Figure 40. Power Losses in a Classical Flyback Structure**

In a classical flyback (as depicted in Figure 40), the standby losses mainly consist of the energy waste due to:

- the startup resistor  $R_{start-up}$  →  $P_{start-up}$
- the consumption of the IC and the power switch control →  $P_{control}$
- the inrush current limitation resistor  $R_{ICL}$  →  $P_{ICL}$
- the switching losses in the power switch →  $P_{SW}$
- the snubber and clamping network →  $P_{SN-CLN}$

$P_{start-up}$  is nearly constant and is equal to:

$$((V_{in}-V_{CC})^2/R_{start-up})$$

$P_{ICL}$  only depends on the current drawn from the mains. Losses can be considered constant. This waste of energy decreases when the standby losses are reduced.

$P_{control}$  increases when the oscillator frequency is increased (each switching requires some energy to turn on the power switch).

$P_{SW}$  and  $P_{SN-CLN}$  are proportional to the switching frequency.

Consequently, standby losses can be minimized by decreasing the switching frequency as much as possible.

The MC44603A was designed to operate at a standby frequency lower than the normal working one.

• **Standby Power Calculations with MC44603A**

During a switching period, the energy drawn by the transformer during the on-time to be transferred to the output during the off-time, is equal to:

$$E = \frac{1}{2} \times L \times I_{pk}^2$$

where:

- L is the transformer primary inductor,
- $I_{pk}$  is the inductor peak current.

Input power is labelled  $P_{in}$ :

$$P_{in} = 0.5 \times L \times I_{pk}^2 \times f_S$$

where  $f_S$  is the normal working switching frequency.

Also,

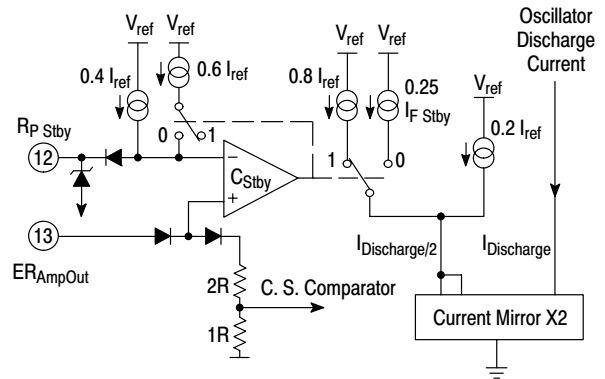
$$I_{pk} = \frac{V_{CS}}{R_S}$$

where  $R_S$  is the resistor used to measure the power switch current.

Thus, the input power is proportional to  $V_{CS}^2$  ( $V_{CS}$  being the internal current sense comparator input).

That is why the standby detection is performed by creating a  $V_{CS}$  threshold. An internal current source ( $0.4 \times I_{ref}$ ) sets the threshold level by connecting a resistor to Pin 12.

As depicted in Figure 41, the standby comparator noninverting input voltage is typically equal to  $(3.0 \times V_{CS} + V_F)$  while the inverter input value is  $(V_{R P Stby} + V_F)$ .



**Figure 41. Standby**

The  $V_{CS}$  threshold level is typically equal to  $[(V_{R P Stby})/3]$  and if the corresponding power threshold is labelled  $P_{thL}$ :

$$P_{thL} = 0.5 \times L \times \left( \frac{V_{R P Stby}}{3.0 R_S} \right)^2 \times f_S$$

And as:

$$\begin{aligned} V_{R P Stby} &= R_{P Stby} \times 0.4 \times I_{ref} \\ &= R_{R P Stby} \times 0.4 \times \frac{V_{ref}}{R_{ref}} \end{aligned}$$

$$R_{P Stby} = \frac{10.6 \times R_S \times R_{ref}}{V_{ref}} \times \sqrt{\frac{P_{thL}}{L \times f_S}}$$

Thus, when the power drawn by the converter decreases,  $V_{CS}$  decreases and when  $V_{CS}$  becomes lower than  $[V_{CS-th} \times (V_{R P Stby})/3]$ , the standby mode is activated. This results in an oscillator discharge current reduction in order to increase the oscillator period and to diminish the switching frequency. As it is represented in Figure 41, the  $(0.8 \times I_{ref})$  current source is disconnected and is replaced by a lower value one  $(0.25 \times I_{F Stby})$ .

Where:  $I_{F Stby} = V_{ref}/R_{F Stby}$

In order to prevent undesired mode switching when power is close to the threshold value, a hysteresis that is proportional to  $V_{RP\ Stby}$  is incorporated creating a second  $V_{CS}$  threshold level that is equal to  $[2.5 \times (V_{RP\ Stby})/3]$ . When the standby comparator output is high, a second current source ( $0.6 \times I_{ref}$ ) is connected to Pin 12.

Finally, the standby mode function can be shown graphically in Figure 42.

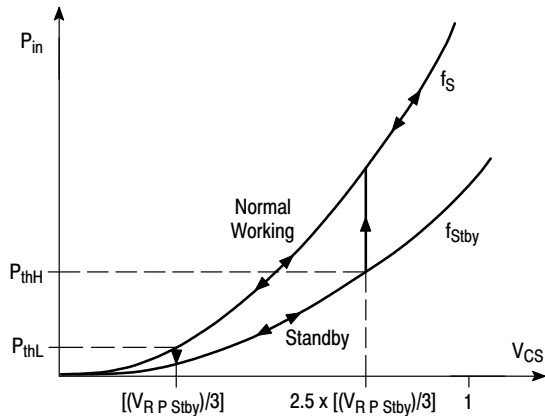


Figure 42. Dynamic Mode Change

This curve shows that there are two power threshold levels:

- the low one:

$P_{thL}$  fixed by  $V_{RP\ Stby}$

- the high one:

$$P_{thH} = (2.5)^2 \times P_{thL} \times \frac{f_{Stby}}{f_S}$$

$$P_{thH} = 6.25 \times P_{thL} \times \frac{f_{Stby}}{f_S}$$

**Maximum Duty Cycle and Soft-Start Control**

Maximum duty cycle can be limited to values less than 80% by utilizing the  $D_{max}$  and soft-start control. As depicted in Figure 43, the Pin 11 voltage is compared to the oscillator sawtooth.

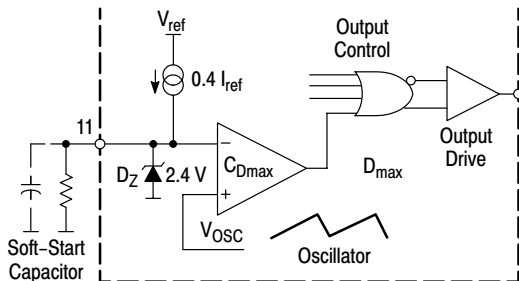


Figure 43.  $D_{max}$  and Soft-Start

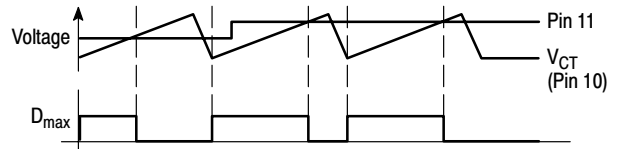


Figure 44. Maximum Duty Cycle Control

Using the internal current source ( $0.4 I_{ref}$ ), the Pin 11 voltage can easily be set by connecting a resistor to this pin.

If a capacitor is connected to Pin 11, the voltage increases from 0 to its maximum value progressively (refer to Figure 45), thereby, implementing a soft-start. The soft-start capacitor is discharged internally when the  $V_{CC}$  (Pin 1) voltage drops below 9.0 V.

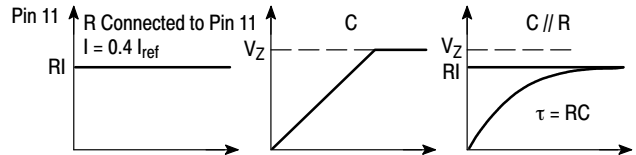


Figure 45. Different Possible Uses of Pin 11

If no external component is connected to Pin 11, an internal zener diode clamps the Pin 11 voltage to a value  $V_Z$  that is higher than the oscillator peak value, disabling soft-start and maximum duty cycle limitation.

**Foldback**

As depicted in Figures 33 and 49, the foldback input (Pin 5) can be used to reduce the maximum  $V_{CS}$  value, providing foldback protection. The foldback arrangement is a programmable peak current limitation.

If the output load is increased, the required converter peak current becomes higher and  $V_{CS}$  increases until it reaches its maximum value (normally,  $V_{CS\ max} = 1.0\ V$ ).

Then, if the output load keeps on increasing, the system is unable to supply enough energy to maintain the output voltages in regulation. Consequently, the decreasing output can be applied to Pin 5, in order to limit the maximum peak current. In this way, the well known foldback characteristic can be obtained (refer to Figure 46).

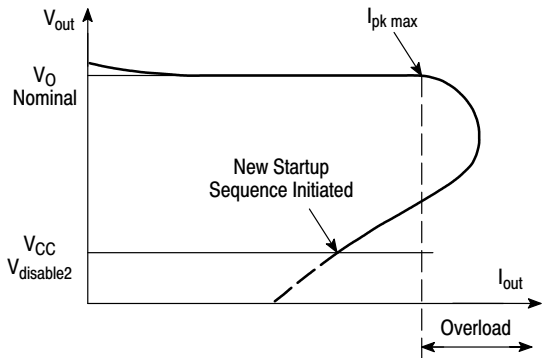


Figure 46. Foldback Characteristic

NOTE: Foldback is disabled by connecting Pin 5 to VCC.

**Overvoltage Protection**

The overvoltage arrangement consists of a comparator that compares the Pin 6 voltage to Vref (2.5 V) (refer to Figure 47).

If no external component is connected to Pin 6, the comparator noninverting input voltage is nearly equal to:

$$\left( \frac{2.0 \text{ k}\Omega}{11.6 \text{ k}\Omega + 2.0 \text{ k}\Omega} \right) \times V_{CC}$$

The comparator output is high when:

$$\left( \frac{2.0 \text{ k}\Omega}{11.6 \text{ k}\Omega + 2.0 \text{ k}\Omega} \right) \times V_{CC} \geq 2.5 \text{ V}$$

$$\Leftrightarrow V_{CC} \geq 17 \text{ V}$$

A delay latch (2.0 μs) is incorporated in order to sense overvoltages that last at least 2.0 μs.

If this condition is achieved, VOVP out, the delay latch output, becomes high. As this level is brought back to the input through an OR gate, VOVP out remains high (disabling the IC output) until Vref is disabled.

Consequently, when an overvoltage longer than 2.0 μs is detected, the output is disabled until VCC is removed and then re-applied.

The VCC is connected after Vref has reached steady state in order to limit the circuit startup consumption.

The overvoltage section is enabled 5.0 μs after the regulator has started to allow the reference Vref to stabilize.

By connecting an external resistor to Pin 6, the threshold VCC level can be changed.

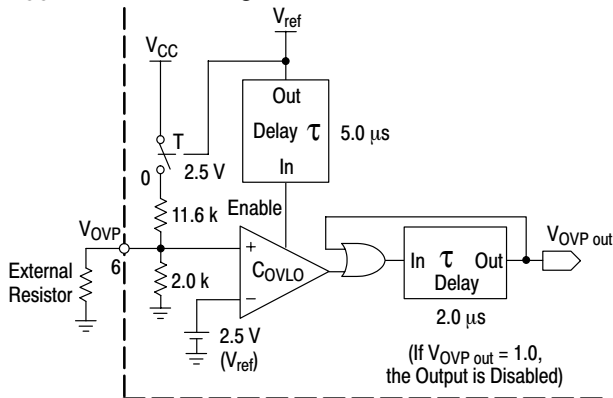


Figure 47. Overvoltage Protection

**Undervoltage Lockout Section**

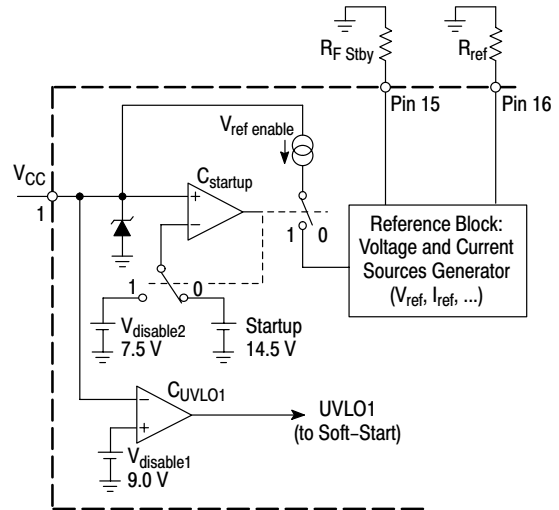


Figure 48. VCC Management

As depicted in Figure 48, an undervoltage lockout has been incorporated to guarantee that the IC is fully functional before allowing system operation.

This block particularly, produces Vref (Pin 16 voltage) and Iref that is determined by the resistor Rref connected between Pin 16 and the ground:

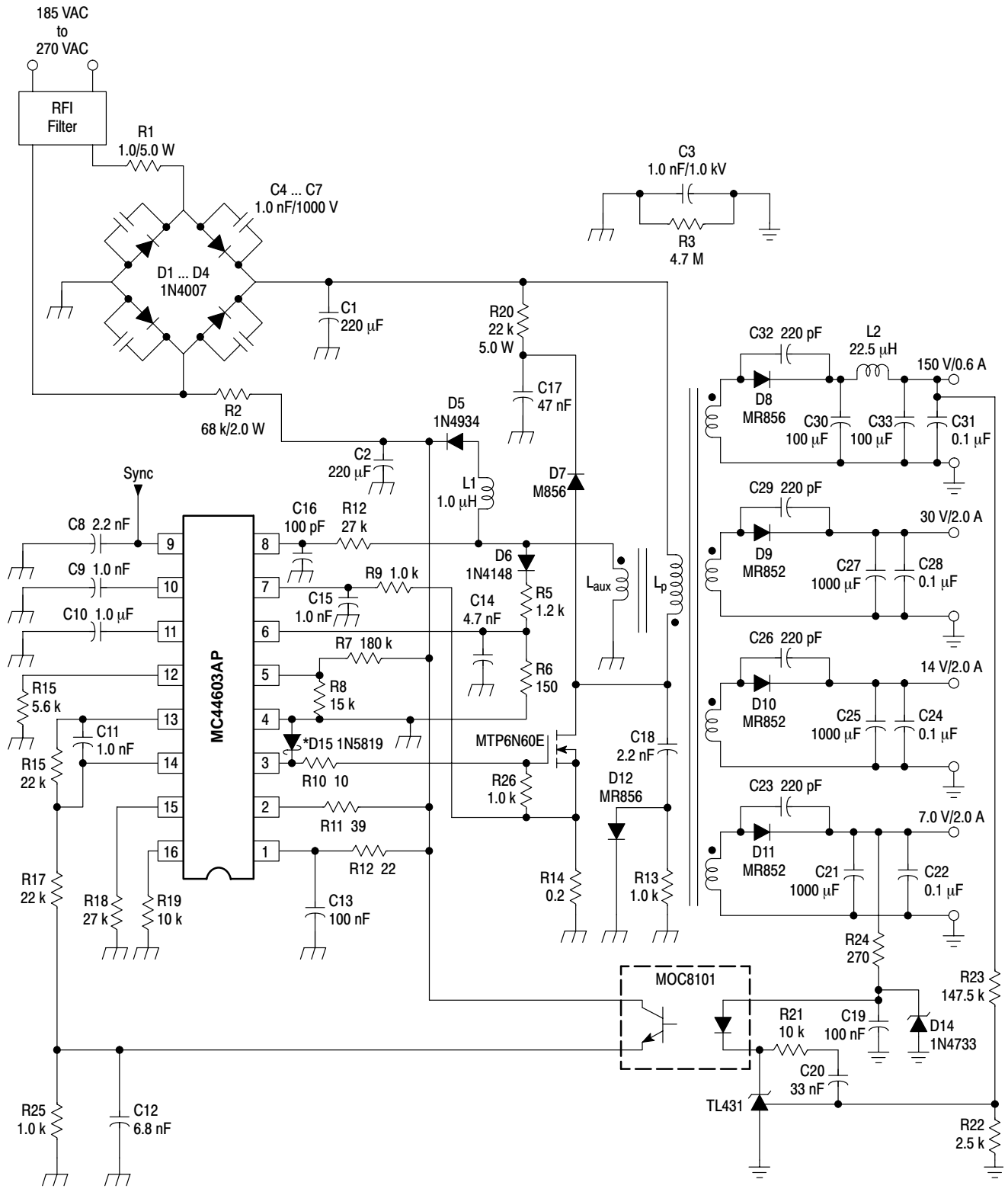
$$I_{ref} = \frac{V_{ref}}{R_{ref}} \text{ where } V_{ref} = 2.5 \text{ V (typically)}$$

Another resistor is connected to the Reference Block: RF Stby that is used to fix the standby frequency.

In addition to this, VCC is compared to a second threshold level that is nearly equal to 9.0 V (Vdisable1). UVLO1 is generated to reset the maximum duty cycle and soft-start block disabling the output stage as soon as VCC becomes lower than Vdisable1. In this way, the circuit is reset and made ready for the next startup, before the reference block is disabled (refer to Figure 30). Finally, the upper limit for the minimum normal operating voltage is 9.4 V (maximum value of Vdisable1) and so the minimum hysteresis is 4.2 V. ((Vstup-th) min = 13.6 V).

The large hysteresis and the low startup current of the MC44603A make it ideally suited for off-line converter applications where efficient bootstrap startup techniques are required.

# MC44603A



\* Diode D15 is required if the negative current into the output pin exceeds 15 mA.

**Figure 49. 250 W Input Power Off-Line Flyback Converter with MOSFET Switch**

# MC44603A

## 250 W Input Power Fly-Back Converter 185 V – 270 V Mains Range MC44603AP & MTP6N60E

Tests	Conditions	Results
Line Regulation 150 V 30 V 14 V 7.0 V	$V_{in} = 185 \text{ VAC to } 270 \text{ VAC}$ $F_{mains} = 50 \text{ Hz}$ $I_{out} = 0.6 \text{ A}$ $I_{out} = 2.0 \text{ A}$ $I_{out} = 2.0 \text{ A}$ $I_{out} = 2.0 \text{ A}$	10 mV 10 mV 10 mV 20 mV
Load Regulation 150 V	$V_{in} = 220 \text{ VAC}$ $I_{out} = 0.3 \text{ A to } 0.6 \text{ A}$	50 mV
Cross Regulation 150 V	$V_{in} = 220 \text{ VAC}$ $I_{out} (150 \text{ V}) = 0.6 \text{ A}$ $I_{out} (30 \text{ V}) = 0 \text{ A to } 2.0 \text{ A}$ $I_{out} (14 \text{ V}) = 2.0 \text{ A}$ $I_{out} (7.0 \text{ V}) = 2.0 \text{ A}$	< 1.0 mV
Efficiency	$V_{in} = 220 \text{ VAC}$ , $P_{in} = 250 \text{ W}$	81%
Standby Mode P input	$V_{in} = 220 \text{ VAC}$ , $P_{out} = 0 \text{ W}$	3.3 W
Switching Frequency		20 kHz fully stable
Output Short Circuit	$P_{out (max)} = 270 \text{ W}$	Safe on all outputs
Startup	$P_{in} = 250 \text{ W}$	VAC = 160 V

### DEVICE ORDERING INFORMATION

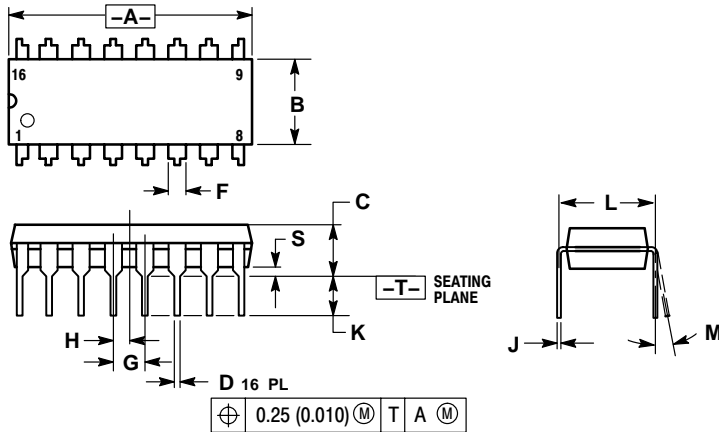
Device	Operating Temperature Range	Package	Shipping <sup>†</sup>
MC44603P	TA = -25°C to +85°C	PDIP-16	25 Units / Rail
MC44603ADW		SOIC-16	47 Units / Rail
MCRR602ADWR2		SOIC-16	1000 / Tape & Reel
MC44603APG		SOIC-16 (Pb-Free)	25 Units / Rail

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MC44603A

## PACKAGE DIMENSIONS

### PDIP-16 CASE 648-08 ISSUE R

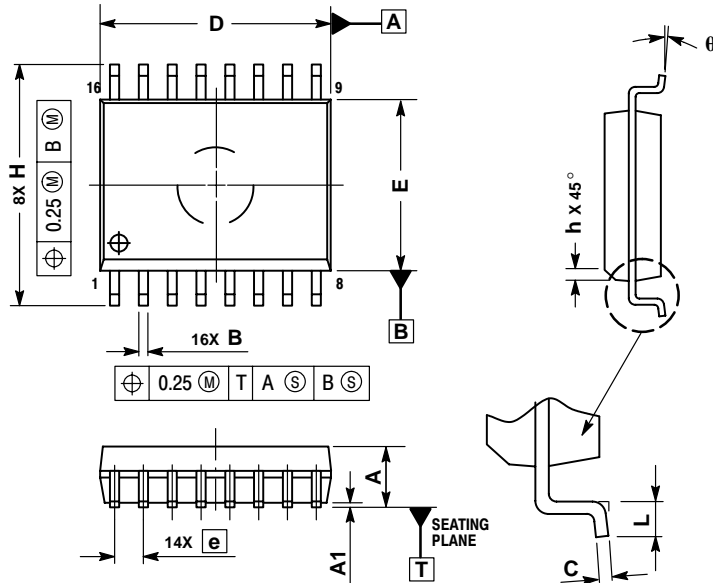


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

### SOIC-16 CASE 751G-03 ISSUE B



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
$\theta$	0°	7°

GreenLine is a trademark of Motorola, Inc.

**ON Semiconductor** and  $\text{\textcircled{M}}$  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.