FAIRCHILD SEMICONDUCTOR®

QFET™

FQD18N20V2 / FQU18N20V2

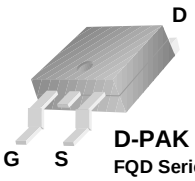
200V N-Channel MOSFET

General Description

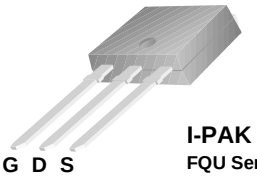
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as automotive, high efficiency switching for DC/DC converters, and DC motor control.

Features

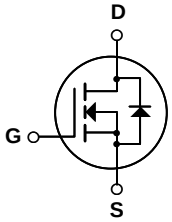
- 15A, 200V, $R_{DS(on)}$ = 0.14Ω @V_{GS} = 10 V
- Low gate charge (typical 20 nC)
- Low Crss (typical 25 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



D-PAK
FQD Series



I-PAK
FQU Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQD18N20V2 / FQU18N20V2	Units
V_{DSS}	Drain-Source Voltage		200	V
I_D	Drain Current - Continuous (T_C = 25°C)		15	A
	- Continuous (T_C = 100°C)		9.75	A
I_{DM}	Drain Current - Pulsed	(Note 1)	60	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	340	mJ
I_{AR}	Avalanche Current	(Note 1)	15	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	8.3	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *		2.5	W
	Power Dissipation (T_C = 25°C)		83	W
	- Derate above 25°C		0.67	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	1.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	200	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.25	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 200 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 160 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 7.5 A	--	0.12	0.14	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 7.5 A (Note 4)	--	11	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	830	1080	pF
C_{oss}	Output Capacitance		--	200	260	pF
C_{rss}	Reverse Transfer Capacitance		--	25	33	pF
C_{oss}	Output Capacitance	V_{DS} = 160 V, V_{GS} = 0 V, f = 1.0 MHz	--	70	--	pF
C_{oss} eff.	Effective Output Capacitance	V_{DS} = 0V to 160 V, V_{GS} = 0 V	--	135	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 100 V, I_D = 18 A, R_G = 25 Ω (Note 4, 5)	--	16	40	ns
t_r	Turn-On Rise Time		--	133	275	ns
$t_{d(off)}$	Turn-Off Delay Time		--	38	85	ns
t_f	Turn-Off Fall Time		--	62	135	ns
Q_g	Total Gate Charge	V_{DS} = 160 V, I_D = 18 A, V_{GS} = 10 V (Note 4, 5)	--	20	26	nC
Q_{gs}	Gate-Source Charge		--	5.6	--	nC
Q_{gd}	Gate-Drain Charge		--	10	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	15	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	60	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 15 A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 18 A, dI_F / dt = 100 A/μs (Note 4)	--	158	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.0	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 1.58mH, I_{AS} = 18A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 18A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

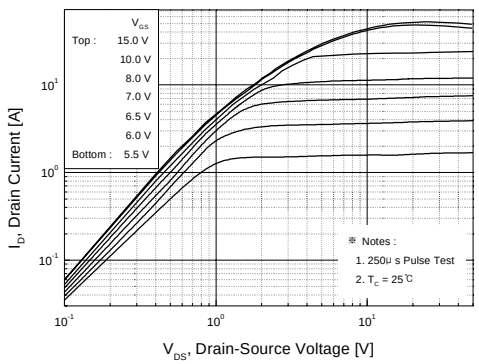


Figure 1. On-Region Characteristics

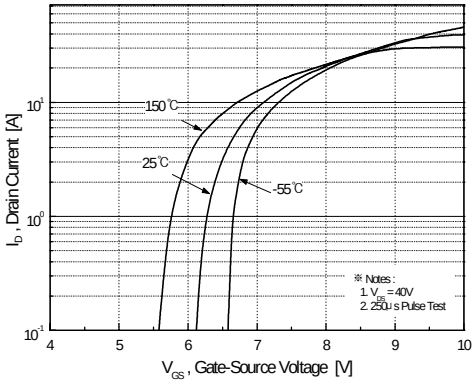


Figure 2. Transfer Characteristics

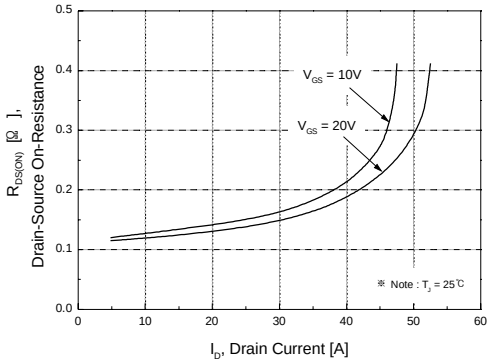


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

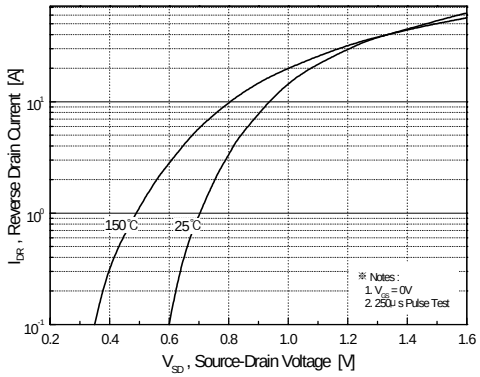


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

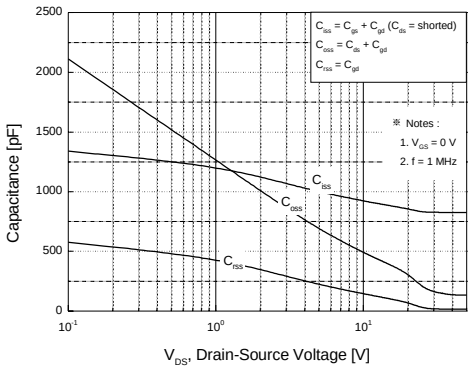


Figure 5. Capacitance Characteristics

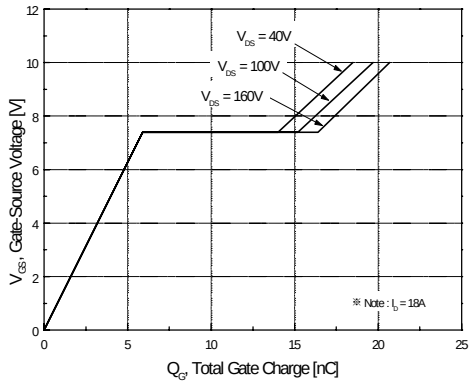


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

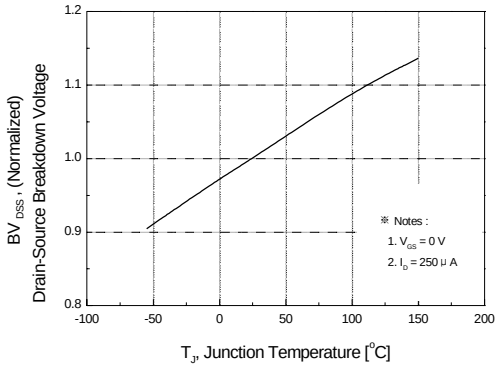


Figure 7. Breakdown Voltage Variation vs. Temperature

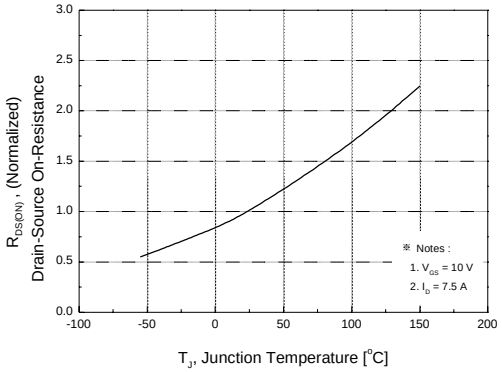


Figure 8. On-Resistance Variation vs. Temperature

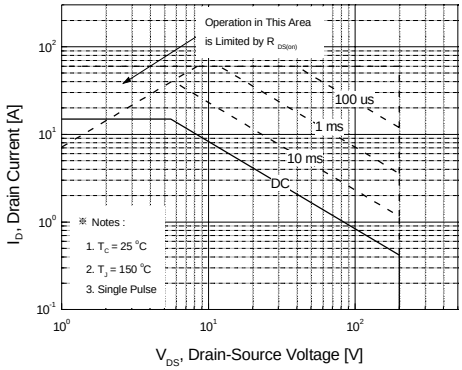


Figure 9. Maximum Safe Operating Area

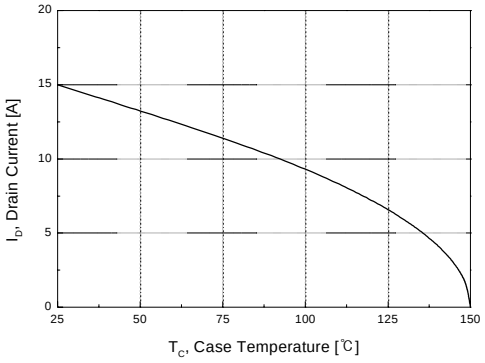


Figure 10. Maximum Drain Current vs. Case Temperature

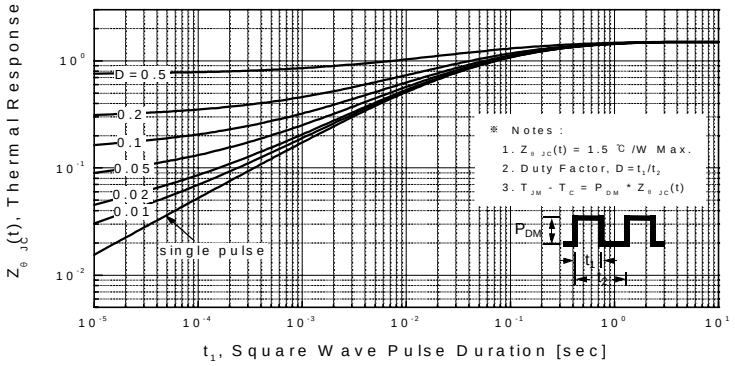
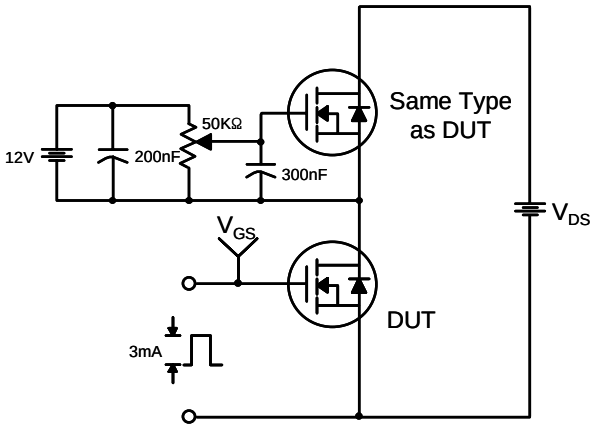
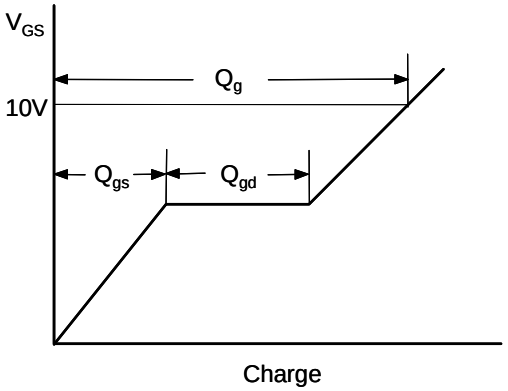


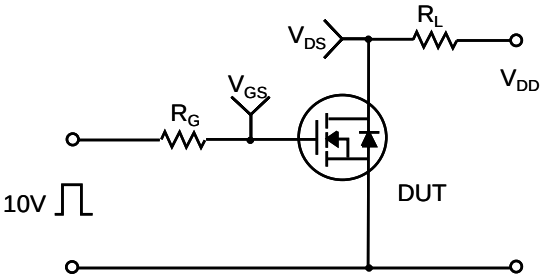
Figure 11. Transient Thermal Response Curve

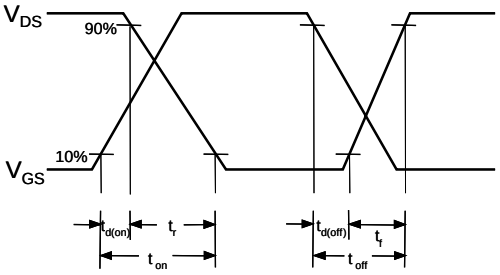
Gate Charge Test Circuit & Waveform



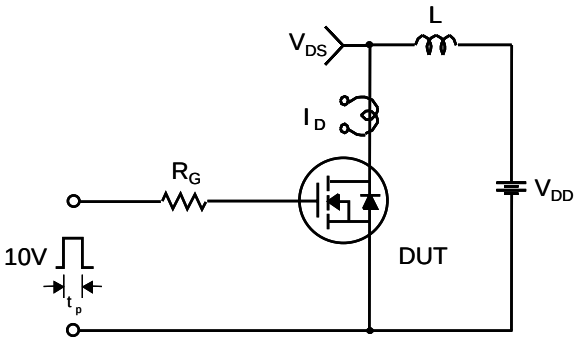


Resistive Switching Test Circuit & Waveforms

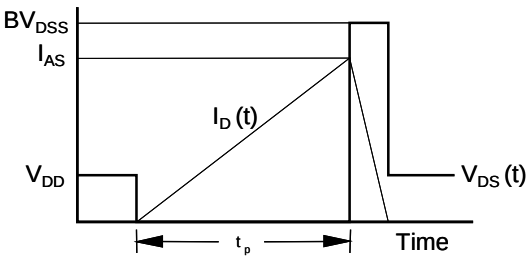




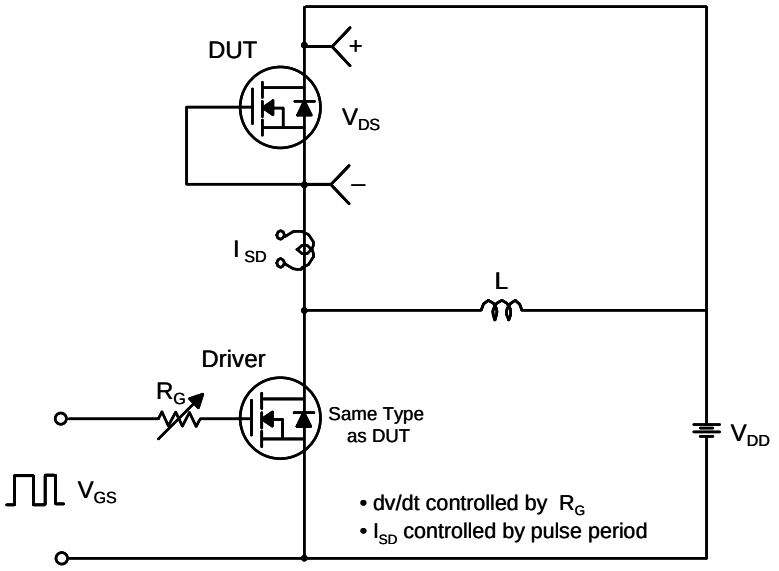
Unclamped Inductive Switching Test Circuit & Waveforms

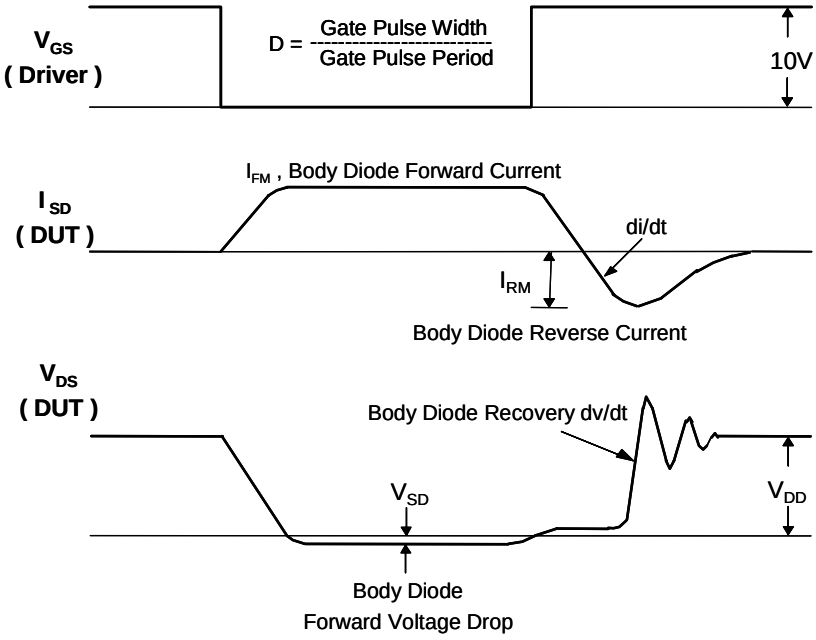


$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



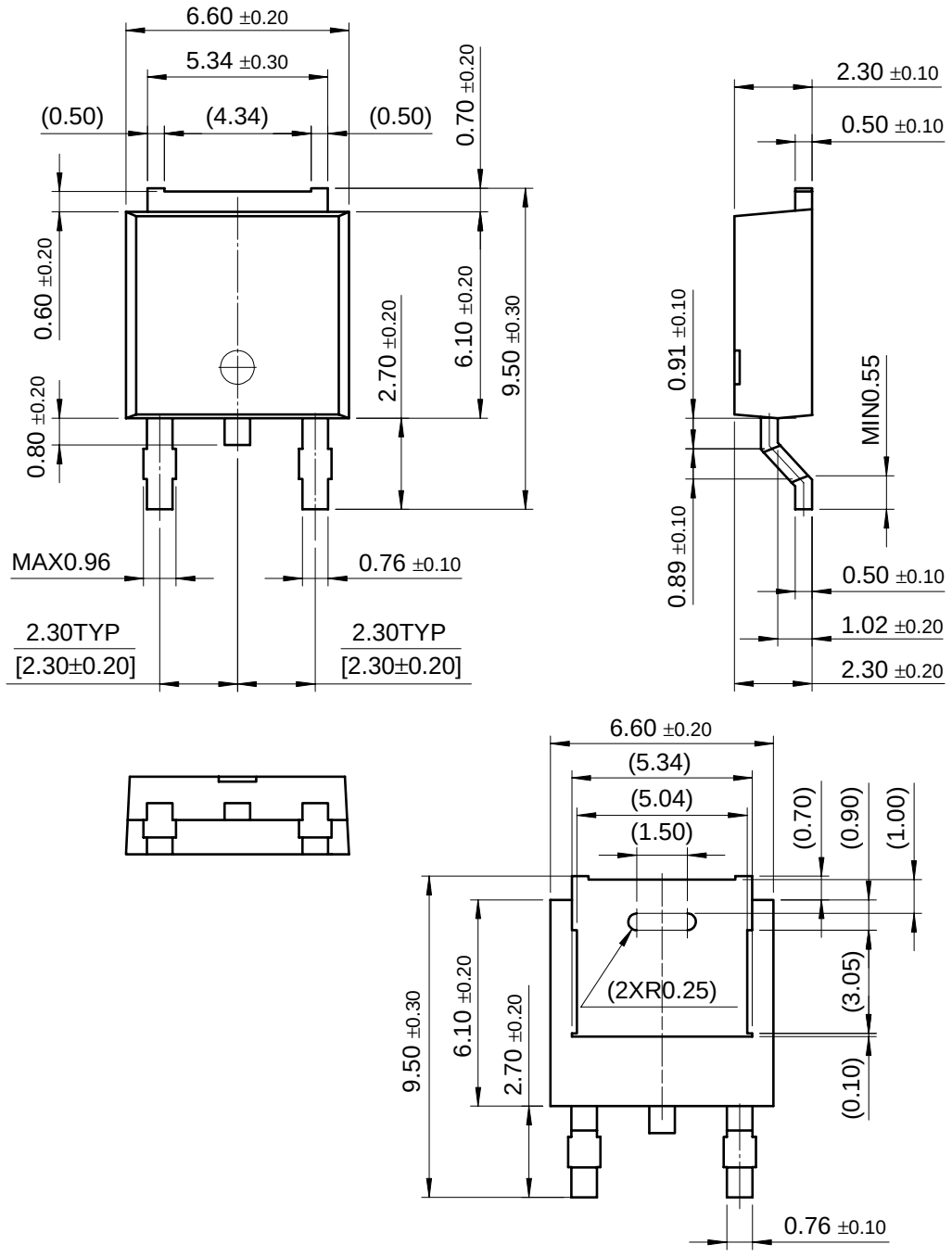
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Package Dimensions

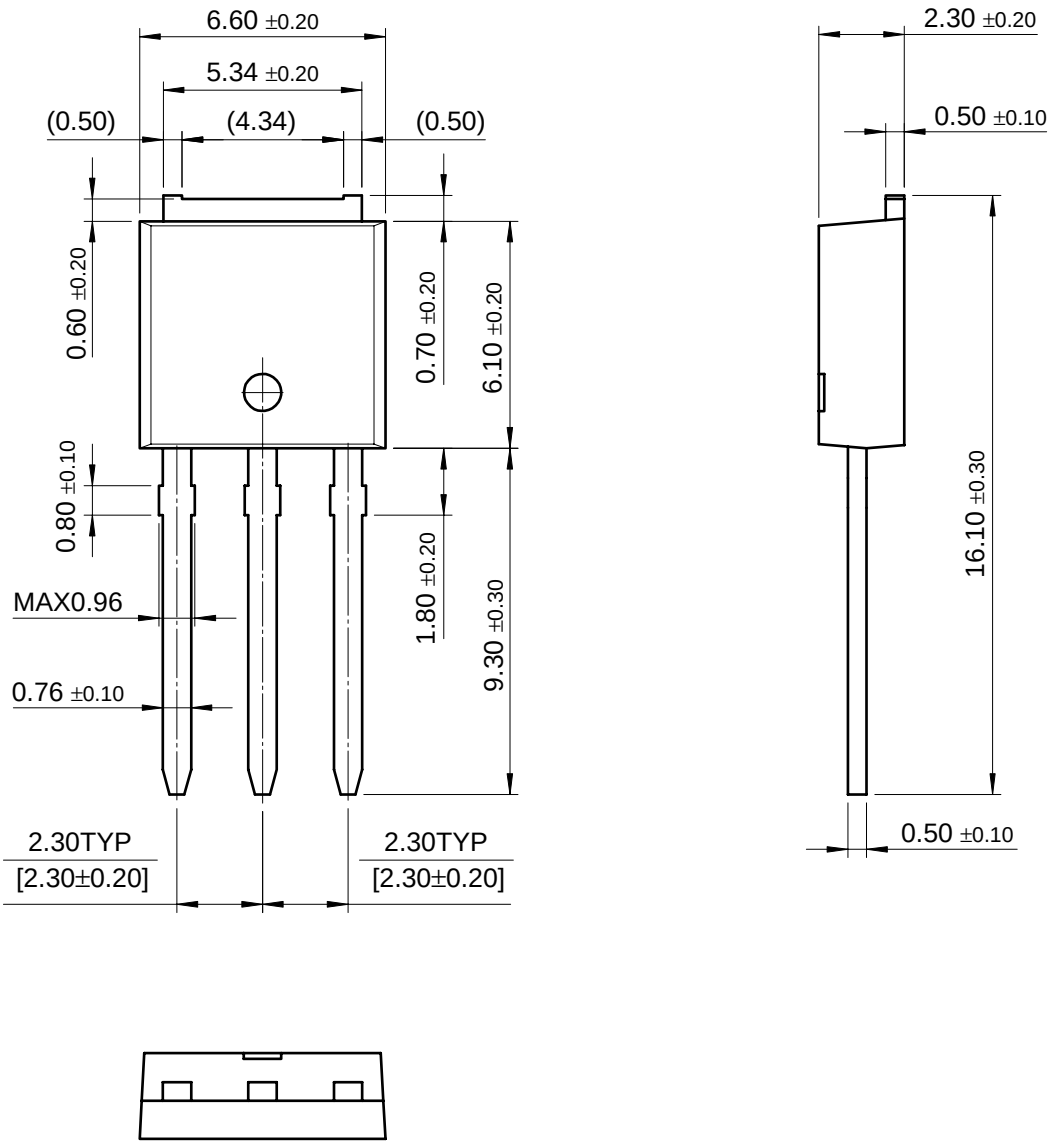
DPAK



Dimensions in Millimeters

Package Dimensions (Continued)

IPAK



Dimensions in Millimeters

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CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
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EnSigna™	I^2C™	OCX™	RapidConfigure™	UHC™
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Programmable Active Droop™		OPTOPLANAR™	SMART START™	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

FQD18N20V2

200V N-Channel Advanced QFET V2 series

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General description

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- Low gate charge (typical 20 nC)
- Low Crss (typical 25 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

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Product status/pricing/packaging

BUY

Product	Product status	Pb-free Status	Pricing*	Package type	Leads	Packing method	Package Marking Convention**
							Line 1: **$Y** (Fairchild logo)

FQD18N20V2TF	Full Production	Full Production	$1.08	TO-252(DPAK)	2	TAPE REEL	&**Z** (Asm. Plant Code) &E&**3** (3-Digit Date Code) Line 2: DV2 Line 3: 18N20
FQD18N20V2TM	Full Production	Full Production	$1.08	TO-252(DPAK)	2	TAPE REEL	Line 1: **$Y** (Fairchild logo) &**Z** (Asm. Plant Code) &E&**3** (3-Digit Date Code) Line 2: DV2 Line 3: 18N20

* Fairchild 1,000 piece Budgetary Pricing
** A sample button will appear if the part is available through Fairchild's on-line samples program. If there is no sample button, please contact a Fairchild distributor to obtain samples

Indicates product with Pb-free second-level interconnect. For more information click here.

Package marking information for product FQD18N20V2 is available. Click here for more information .

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Models

Package & leads	Condition	Temperature range	Vcc range	Software version	Revision date
PSPICE					
TO-252(DPAK)-2	Electrical/Thermal	-55°C to 150°C	0V to 50V	OrCAD 10.3	Jun 27, 2007

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Qualification Support

Click on a product for detailed qualification data

Product
FQD18N20V2TF
FQD18N20V2TM

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