SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TDA9102C

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TECHNICAL INFORMATION

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1. ABSTRACT

The system evolution in the monitor field leads to develop suitable I.C.'s whose performances and characteristics are mainly monitors oriented rather than TV oriented. The automatic frequencies raster preset of the monitor by computer and optical equipments leads to the adoption of Digital to Analog converters in order to set the different parameters, and consequently all regulation must be DC compatible.
High scanning frequency and low jitter are additional factors that characterize the quality and the resolution of the monitor. In this note new circuit solutions on silicon, concerning the monitor field, are described. In a single I.C., making use of TTL compatible synchro pulses, horizontal and vertical processing functions and vertical ramp generation are implemented.

2. INTRODUCTION

In Figure 1 is shown the block diagram of TDA9102C.
Horizontal frequency and phase as well as vertical frequency, amplitude and linearity are all DC adjustable on different terminals.The horizontal phase adjustment within ± 45° is implemented on first PLL (sync-oscillator) rather than on the second PLL (flyback-oscillator) allowing the raster to be centered in case of no standard phase sync position.
An additional feature makes the raster phase independent by the duty-cycle of the input synchronizing pulse thanks to an internal shaper circuit generating a standard sync pulse starting from the leading edge of input signal.
The vertical amplitude changes depending on a voltage amplifier whose gain is set on Pin 16 ; the peak to peak voltage of the sawtooth does not influence its average value which is maintained constant.
The current capability of the horizontal output stage (Pin 7) is such to directly drive an external darlington used as line power switch.
Since part of the jitter effect is due to the internal voltage reference circuits, an external pin connected to the V_{CO} supply voltage is got available for noise filtering (Pin 19).

3. FUNCTIONAL DESCRIPTION

Here following are briefly described all the functional blocks of TDA9102C.

3.1 Horizontal oscillator

The circuit in Figure 2 is a Current Controlled Oscillator, it works charging and discharging the capacitor at pin 2 between two thresholds V_{S1} = 2.5V and V_{S2} = 6.5V coming from an internal resistor divider. This one is also used to provide a voltage reference at pin 1 (V_1 = 3.5V) by means of a unity gain amplifier.
An external resistor connected between Pin 1 and ground sets the current reference.
This current is mirrored with 0.5 : 1 ratio to charge the capacitor C_O at Pin 2, and with 2 : 1 ratio to discharge C_O.
The charging and discharging time ratio will result in 3 : 1.
The differential switch Q_{22}-Q_{23} is driven by a S-R flip-flop, which changes its state every time that the peak of the triangular waveform reaches one of the two thresholds V_{S1} or V_{S2}.

3.2 Horizontal synchronism shaper circuit

The electric diagram shown in Figure 3 can be divided in three stages. The first of which is a negative edge detector able to set the S-R flip-flop each time that a negative edge of the sync pulse is applied to the input (Pin 4).
The second one is a differential stage that feeds the first phase comparator (φ 1).
The third stage uses an external capacitor to produce a ramp on the Pin 5. As soon as the peak of the ramp reaches the internal threshold (6V) the external capacitor is suddenly discharged and the flip-flop is reset.
The horizonal sync pulse width on the collector of Q_{59} will depend on the value of the capacitor at Pin 5.

3.3 First phase comparator (φ 1) and phase adjustment interface circuit

In the circuit of Figure 4, a comparator squares the horizontal waveform using as voltage reference Vref1 which represents the output of the phase adjustment interface circuit.
If the voltage at Pin 10 changes in the range from 0.5V to 4.5V, the phase will shift of ± 45° between the sync and the middle of H-sawtooth (consequently middle of H-flyback).
The rectangular waveforms that are the outputs of first differential amplifier are applied to another differential stage which is activated only during the internal horizontal sync pulse coming from the horizontal sync shaper circuit (see Figure 3).
The product in terms of current of the sync signal and the oscillator signal is available at Pin 3.
Two clamps limit the maximum voltage range of Pin 3 (from 1V to 6V) and consequently the hold in range of the CCO.

Figure 1

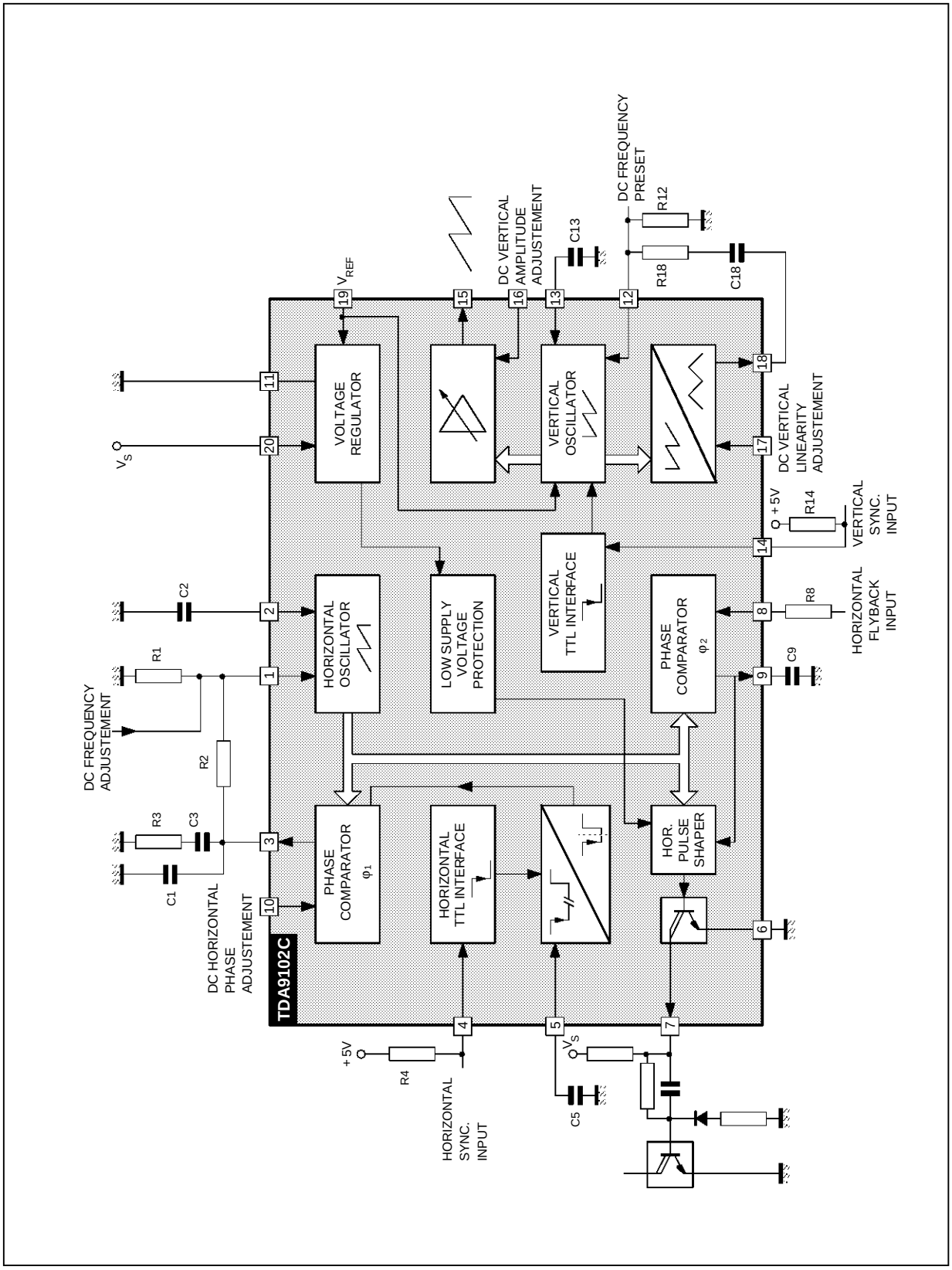

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Figure 2

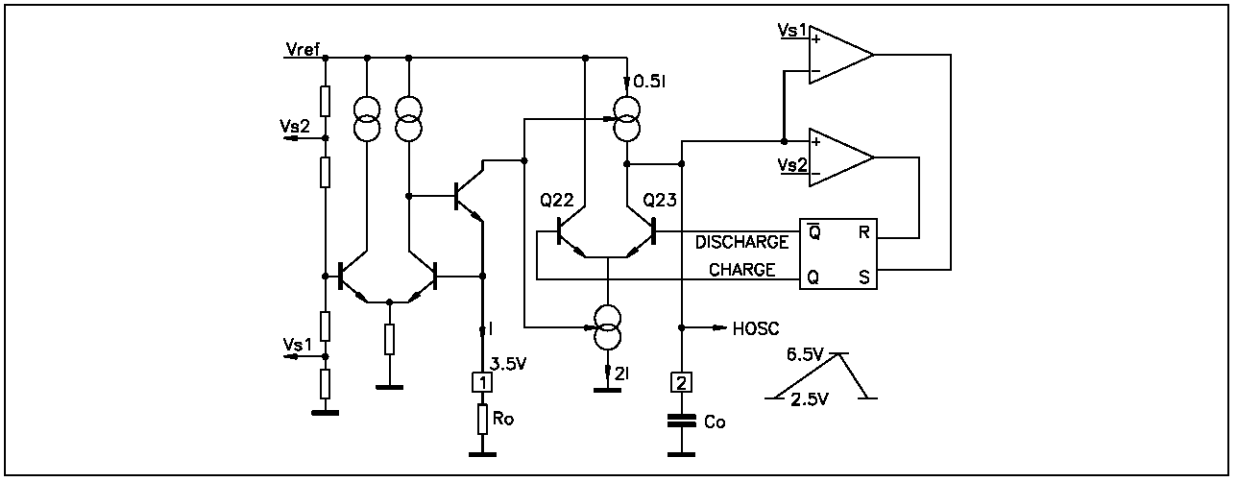


Figure 3

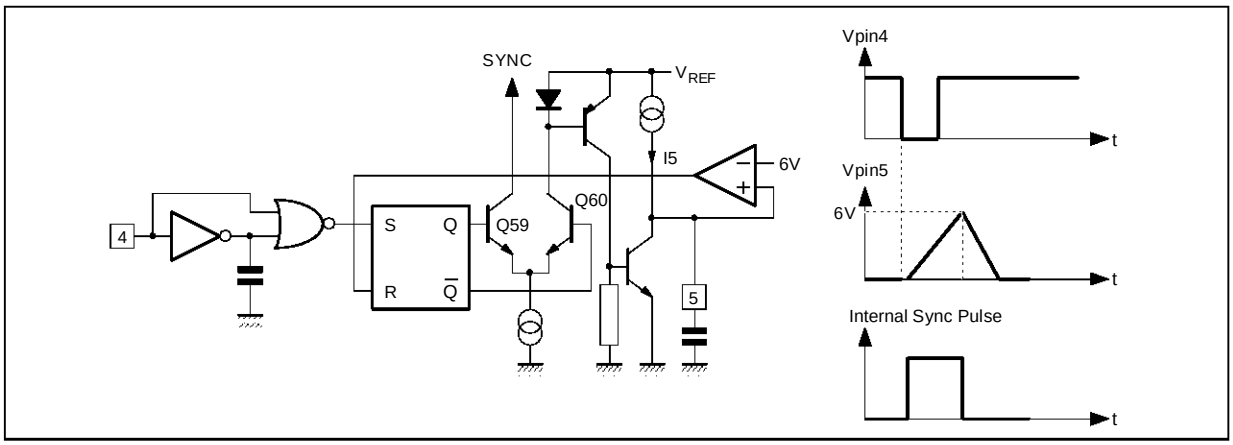
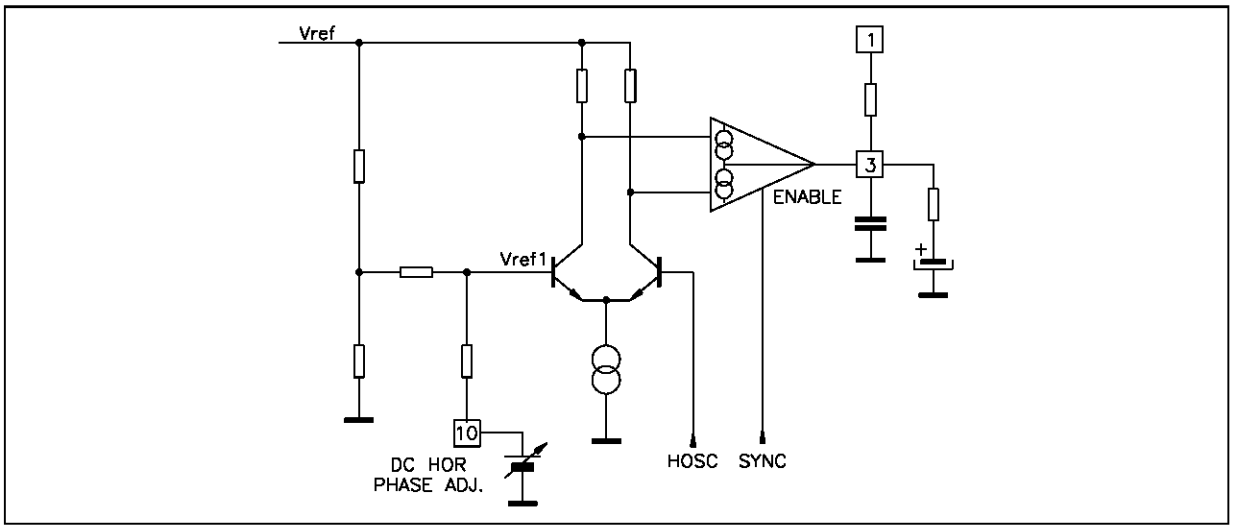


Figure 4



3.4 Second phase comparator (φ 2) between flyback and oscillator

This circuit recovers dynamically the deflection delay of line output transistor.

The flyback pulse applied to Pin 8 (see Figure 5) is detected and clamped at a voltage level of 0.7V.

This circuit is similar to φ 1, the substantial differences are two, the input pulse is the flyback pulse instead of sync pulse and the first differential stage is activated by S-R flip-flop of horizontal oscillator.

The φ 2 output acts on the horizontal output stage in order to shift the output pulse to recover the deflection delay.

3.5 Phase shifter, output stage and start up circuit

The storage time t_S of the line output transistor is recovered by advancing the leading edge of the output pulse of ts with respect to the phase of the sync reference.

The triangular oscillator waveform (Figure 6a) is compared with internal threshold S_1 and S_2 whose voltages depend upon the voltage level present at the output of phase comparator φ 2 (Pin 9).

The voltage difference S_1-S_2 is constant and this value fixes the duty-cycle of the horizontal output pulse present at Pin 7.

During the positive slope of the oscillator the output pulse (Pin 7) is low when the triangular waveform voltage is in the voltage range established by S_1 and S_2; whereas during the negative slope of the oscillator the output pulse is always at high level thanks to a comparator driven by S-R flip-flop of horizontal oscillator.

As shown in Figure 6a, a transistor insures that the output pulse is low when the flyback pulse is present (this feature can be used to simplify X-ray protection).

At the switch on, the horizontal output stage (Pin 7) is inhibited until the power supply does not overcome 8 V.

About the maximun allowable delay, it depends on the flyback time and the working frequency (see Figure 6b).

The PLL2 works in such a way as to maintain the middle of the flyback exactly in correspondence with the crossing between of the V_{REF} = 4.5V and the oscillator ramp.

Then if you suppose to have zero delay time, the switch-off edge of the output pulse will rise at point "A" now if the delay time increases the switch-off edge will move to point "B" to recover the delay.

The equation to calculate the t_D with a good approximation is the following :

$$\text{Maximum Allowable Delay : } t_D = \frac{t_r}{2} - \frac{t_{FLY}}{2}$$

where t_R is the rise time of the horizontal ramp = 3/4 T and t_{FLY} is the flyback time.

The typical value of the horizontal duty cycle of the TDA9102C is 41%.

Figure 5

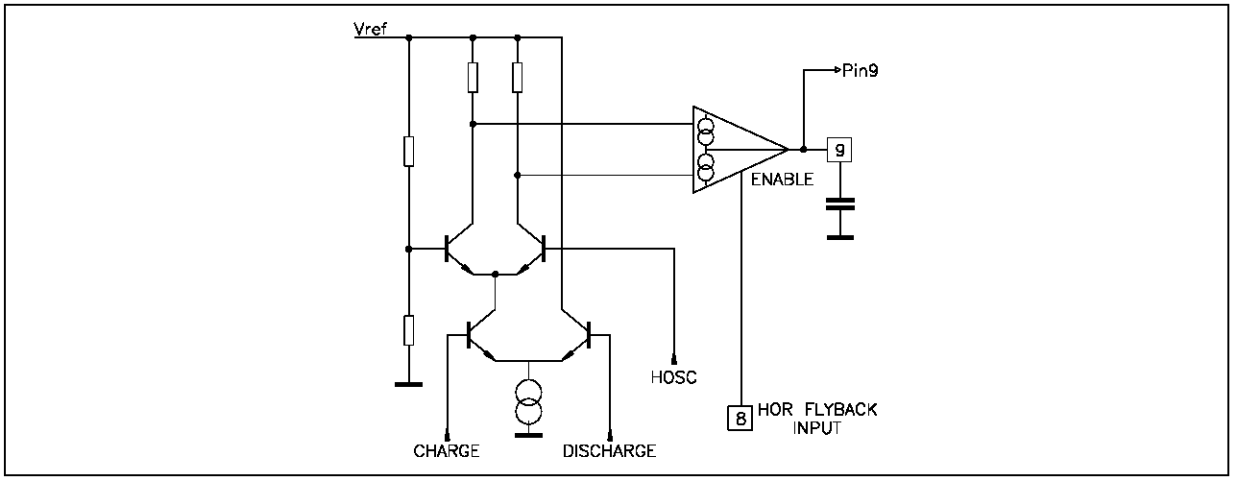


Figure 6a

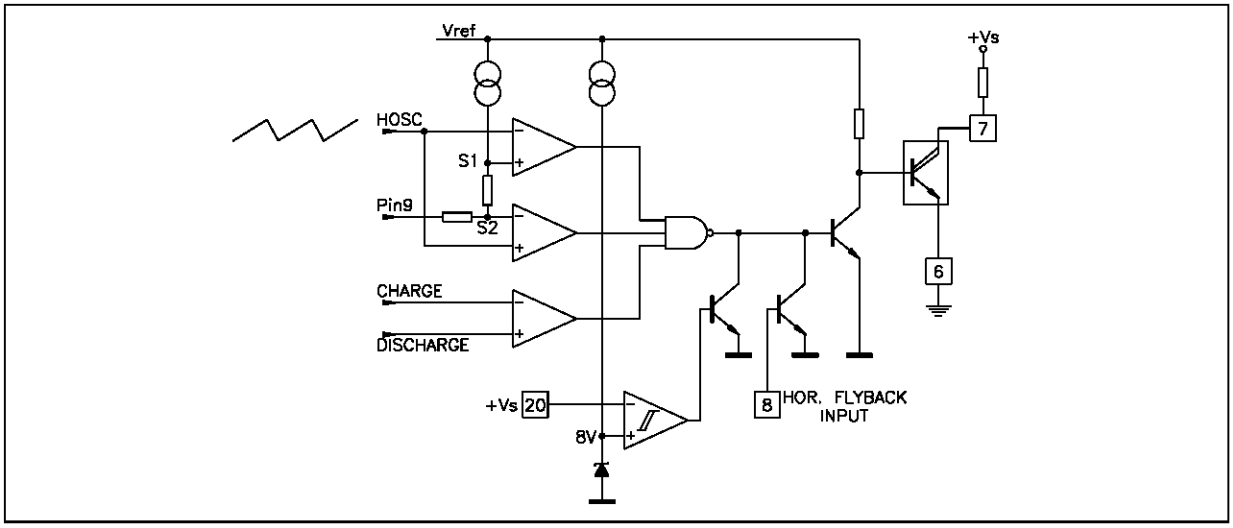
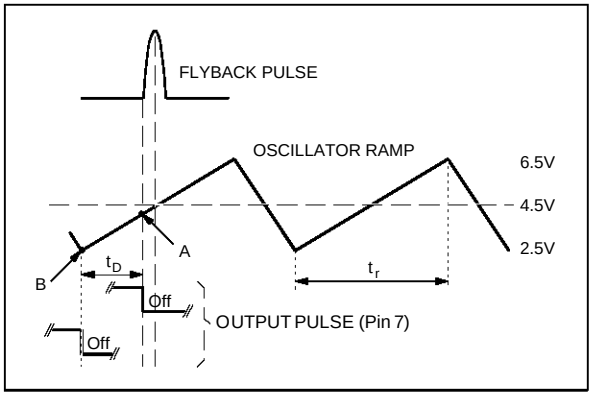


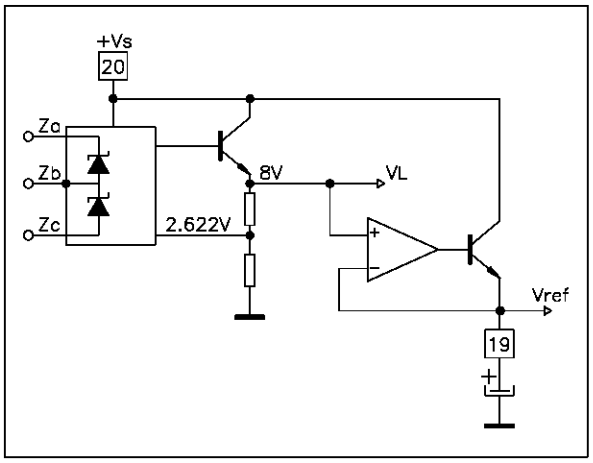
Figure 6b



3.6 Voltage regulator 8 V

The voltage reference, Figure 7, is a band-gap circuit that allows on the output a voltage reference equal to 2.622V that means a voltage V_L = 8V.

Figure 7



By means of zener zap is possible to adjust, during the testing, the voltage reference from ± 6% into a ± 2% range.

V_L feeds all the circuits of the vertical side and, by means of a unity gain amplifier, provides a voltage reference (V_{REF}) at Pin 19 to supply all the circuits of the horizontal side.

The unity gain amplifier is necessary to avoid all the possible interactions between the horizontal and vertical sections.

Moreover, to minimize jitter on the horizontal oscillator, is possible to connect an external capacitor between Pin 19 and ground.

3.7 Vertical oscillator

A new concept of vertical oscillator is implemented in this I.C. whose resistor divider, used to set the lower and higher thresholds (V_{low} = 2V ; V_{high} = 6.8V), is not commutated .

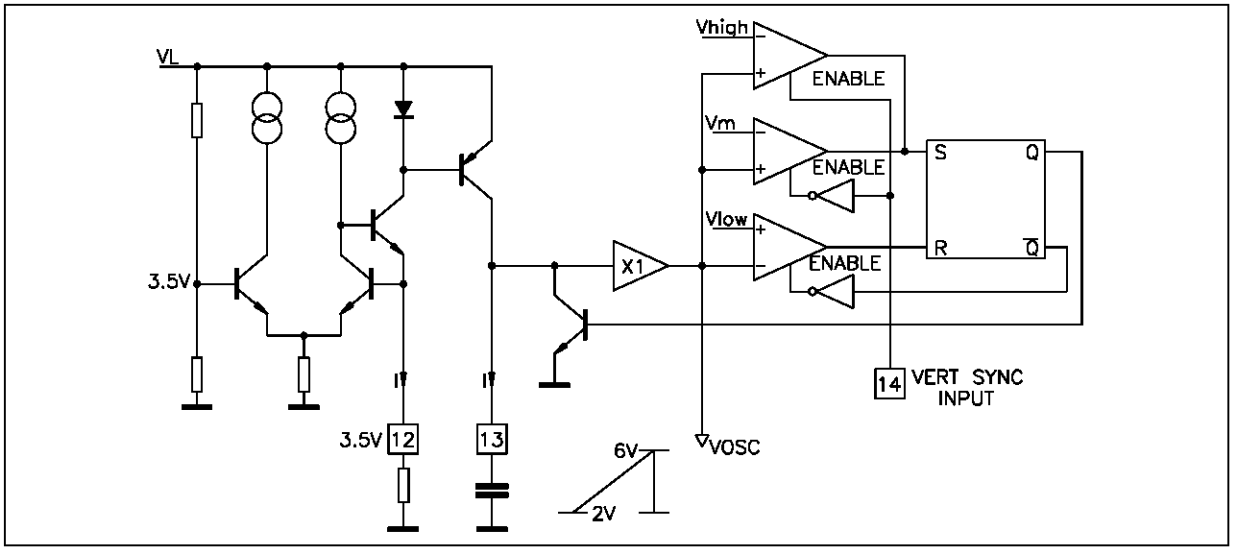
The circuit shown in Figure 8 works charging an external capacitor connected at Pin 13 with a current set at Pin 12 and reflectd to Pin 13 through a current mirror.

As soon as the ramp gets V_m or V_{high} the capacitor is quickly discharged by a darlington, the voltage on the capacitor will fall down till to get the lower threshold; at this point the darlington will be driven off and the current will charge again the capacitor.

A buffer is used to decouple the ramp generator from other circuits (like linearity correction and amplitude regulation circuits).

The lower threshold is detected by a differential stage whose current generator is only activated during the discharge phase.

Figure 8



A comparator detects the higher threshold corresponding to the free running frequency; if no sync pulse (negative edge) is applied on Pin 14, this stage is continually fed and the capacitor at Pin 13 is discharged when the vertical ramp reaches V_{high}.

If the sync pulse is present the previous comparator will be inhibited and another comparator, which has the threshold at 5.2V (V_m), will be activated.

This last comparator, when it is set going, is able to cause the discharge of the capacitor at Pin 13 if the vertical ramp is between the thresholds Vm and V_{high}.

In this way the vertical synchronization is established.

To guarantee that the vertical oscillator is locked in the middle of the pull-in range is necessary to adjust the current at Pin 12 until the peak of the vertical sawtooth, in locking condition, reaches the voltage equal to:

$$V_P = \frac{V_m + V_{high}}{2} = 6\ V$$

that means V_{pp} = 4V.

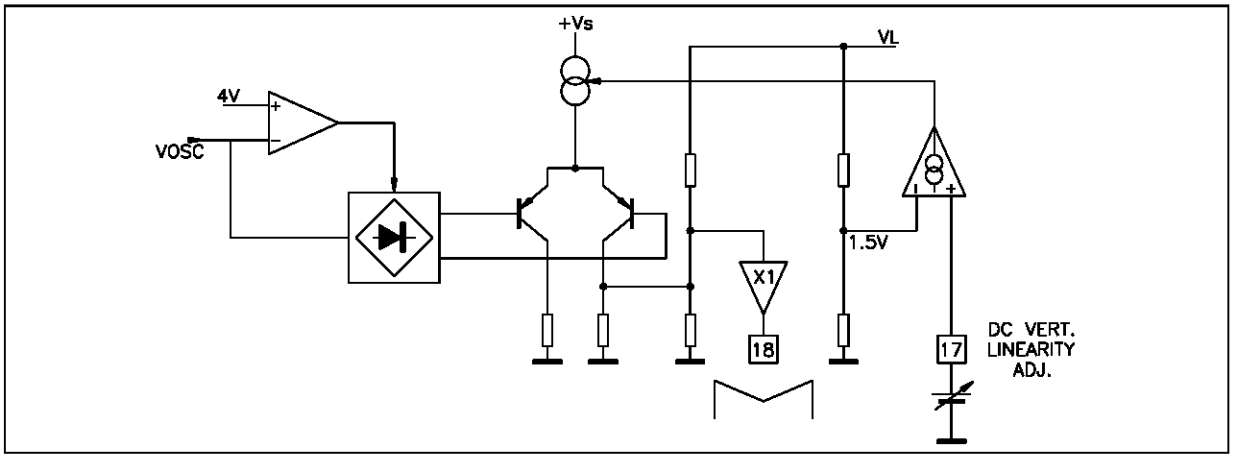
3.8 S Correction circuit and DC linearity adjustment

The circuit which is used to realize a new concept of vertical linearity regulation is shown in Figure 9.

A comparator rectifies the vertical sawtooth using as voltage reference a fixed value (4V) that is the average value of sawtooth.

This squared signal is used to drive a particular configuration of differential stage in order to obtain, in terms of current, a triangular waveform which inverts its slope just when the original sawtooth crosses the voltage reference.

Figure 9



This current signal is converted in voltage by a resistor divider and transferred on Pin 18 through a buffer.
The peak to peak voltage on this pin depends on the maximum current that the output differential stage is able to handle, the value of this current can be externally regulated by means of Pin 17 through a transconductance amplifier.
An external feedback resistor in series to a capacitor (to avoid any DC offset) must be connected between Pins 18 and 12 in order to obtain the proper S correction as shown in Figure 10.

3.9 Vertical amplitude regulation circuit

This function has been implemented using the circuit configuration that can be seen in Figure 11.
It consists of an Op-Amp in non inverting input configuration and of a variable gain OTA whose gain can be set by means of the Pin 16 through a transconductance amplifier.
Both the inputs of the two circuit handle the vertical ramp and the output of the multiplier is fed back to the inverting input.
The control circuit is a transconductance amplifier that modulates the current of the variable gain OTA depending on the DC voltage applied on Pin 16.
This circuit guarantees a gain adjustment of ± 20% around the nominal value.

4. CONCLUSION

This new I.C. can be considered as a first step towards a new generation of serial bus compatible LSI circuits in which additional logic function can be implemented and all the D/A converters can be included.
It is assembled in 20 pins DIL plastic package able to dissipate the 0.7W required by a typical application.

Figure 10

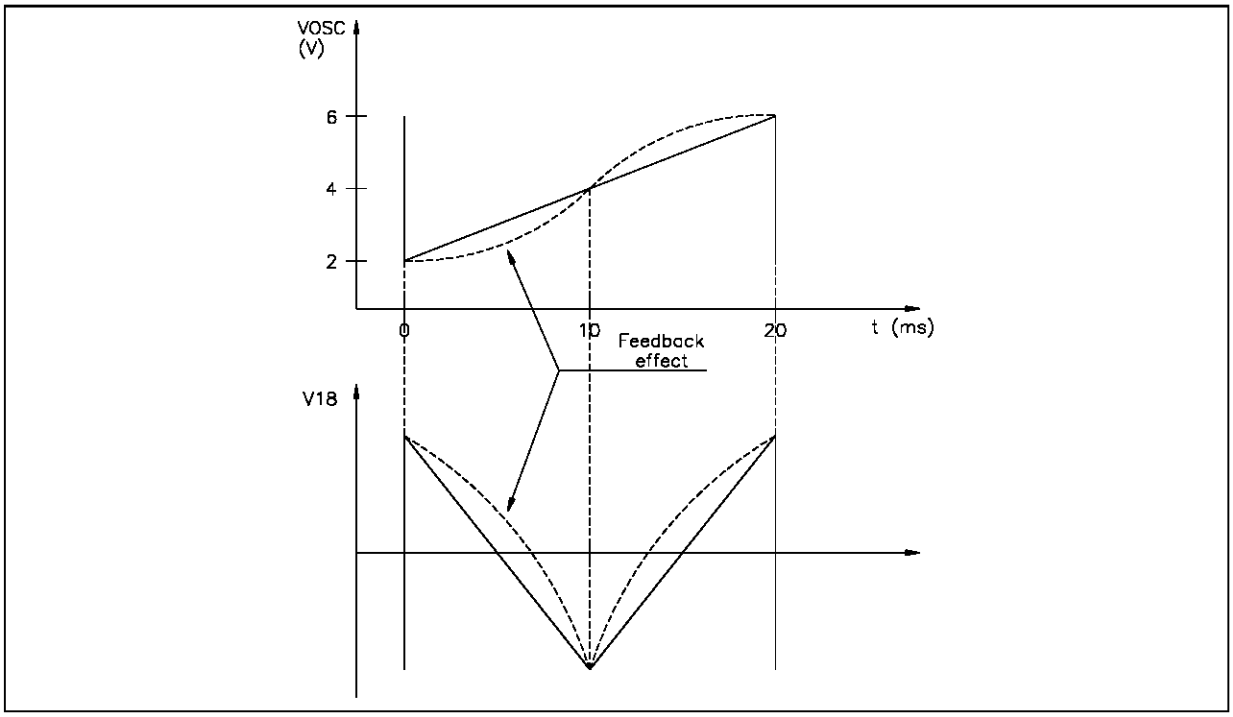
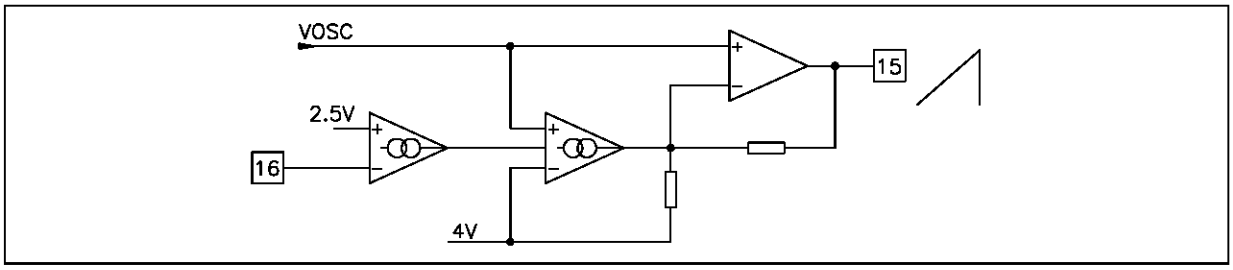


Figure 11



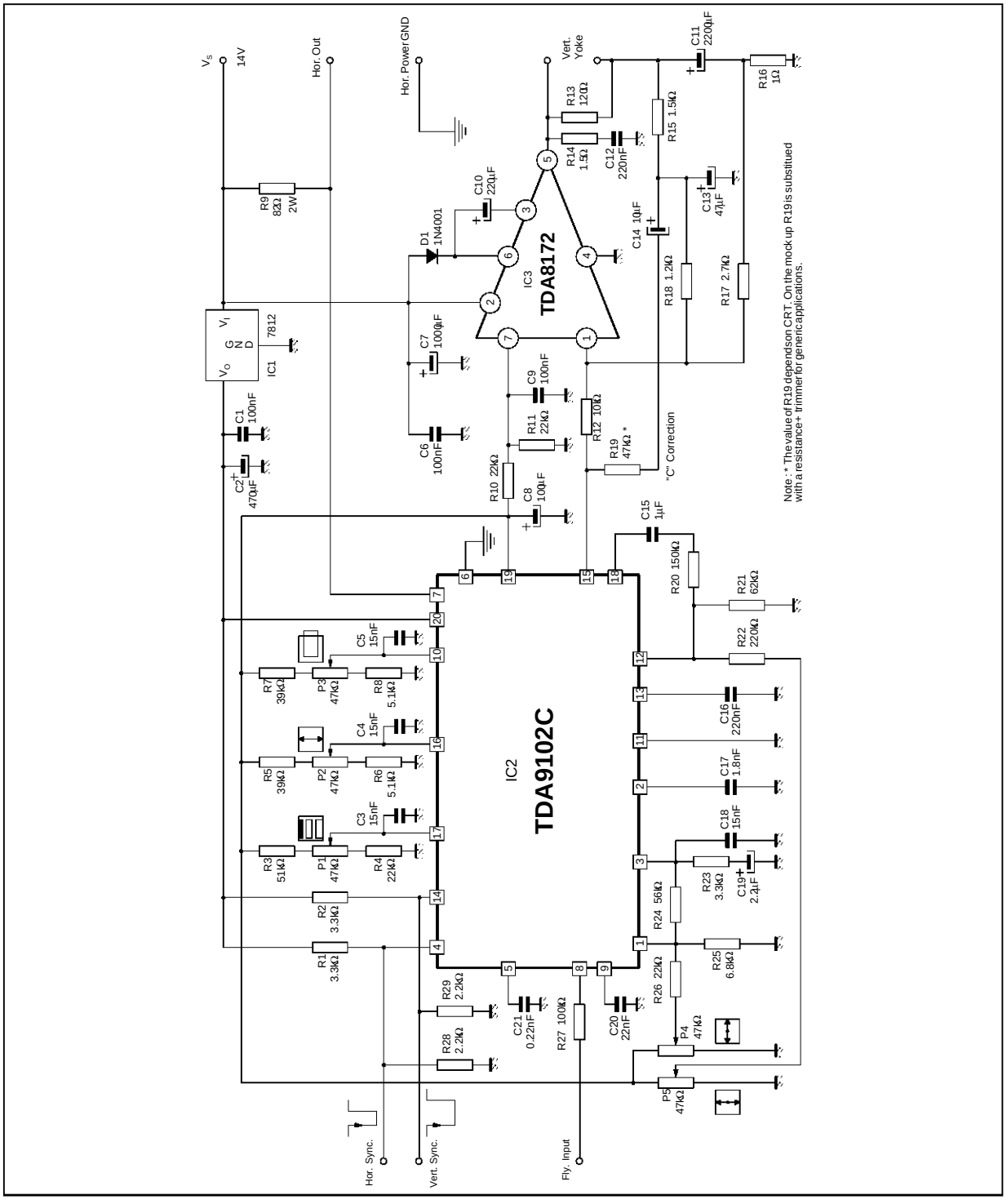
APPLICATION INFORMATION

In Figure12 is shown a typical application of the TDA9102C with the TDA8172, which is a vertical booster; for further information regarding TDA8172 consult the note :

SGS-THOMSON "Vertical Deflection Stages for TV and Monitor" by A. MESSI

All the information is referred to the above mentioned figure.

Figure 12



5. HORIZONTAL SECTION

5.1 Frequency

The device is able to work from 15kHz to 100kHz.

The free running frequency is fixed by the resistor at Pin 1 (R_{25}) and by the capacitor at Pin 2 (C_{17}) with the following formula:

$$f_O = \frac{1}{K_O \times R_{25} \times C_{17}}$$

where K_O is typically $3.0476 \pm 5\%$ (see data-sheet).

In the aplication of Figure 12, using $R_{25} = 6.8k\Omega$ and $C_{17} = 1.8nF$, we obtain:

$$f_O = \frac{10^6}{3.0476 \times 6.8 \times 1.8} = 26.808kHz$$

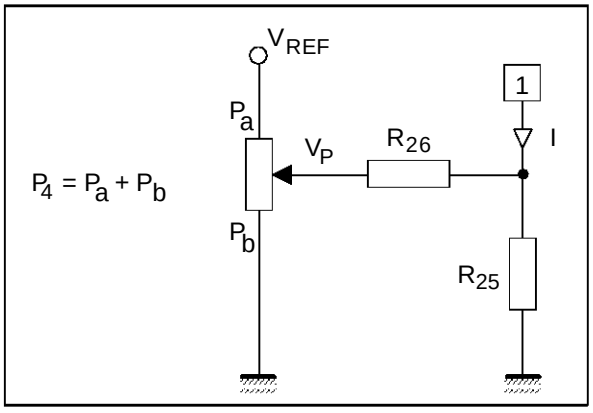
The maximum available current at Pin 1 is 1mA, so it must be $\frac{V_1}{R_{25}} \leq 1mA$.

By means of trimmer P_4 , it is possible to adjust the horizontal free running frequency, that changes accordingly with the following formula:

$$f_H = f_O \left\{ 1 - \frac{(V_p - V_1) / R_{26}}{V_1 / R_{25}} \right\}$$

where $0 \leq V_p \leq 8V$ is the voltage at the central point of the trimmer (see Figure 13).

Figure 13



5.2 Pull-in range

This range is determined by the ability of the first comparator (φ 1) to correct the difference between the sync frequency and the free running frequency and it is set by R_{24} and R_{25}.

$$f_{pull-in} = f_O \frac{|V_3 - V_1| / R_{24}}{V_1 / R_{25}}$$

$|V_3 - V_1|$ is typically 2.5V, while $V_1 = 3.5V$.

This is the theoretical value calculated if the frequency adjustment is disconnected.

In the application inf Figure 12 we have:

$$f_{pull-in} = 26808 \frac{2.5}{3.5} \cdot \frac{6800}{56000} = \pm 2.3kHz$$

When the frequency adjustment is connected the pull-in range changes due to the fact that in parallel with R_{25} are connected $R_{26} + P_b$ (see Figure 13).

When the device is synchronized and perfectly tuned, $V_3 = V_1$ and the φ 1 will work in the best way.

C_{17}, on the contrary of R_{25}, is influential only for the free running frequency of the horizontal oscillator; it has no effect on the pull-in range, which doesn't change in percentage with respect to the free running frequency.

If you change the horizontal frequency changing R_{25} the pull-in range changes accordingly with the previous formula.

5.3 Internal sync. width

The internal sync. pulse is made by current generator (I_5) that charges an external capacitor at Pin 5 (C_{21}) up to the trigger threshold $V_5 = 6V$.

$$t_5 = \frac{C_{21} \times V_5}{I_5}$$

$t_5 = 1 / (12 \times f_O)$ is recommended.

5.4 Phase adjustment range

The voltage range accepted at Pin 10 is from 0.5V to 4.5V, so the resistor divider must be dimensioned to supply these values.

In our application we have :

$$V_{10\ min} \left| \begin{array}{l} = \frac{V_{19}}{R_7 + P_3 + R_8} R_8 \\ = \frac{8}{39 + 47 + 5.1} 5.1 \\ = 0.447V \end{array} \right.$$

$$V_{10\ max} \left| \begin{array}{l} = \frac{V_{19}}{R_7 + P_3 + R_8} (P_3 + R_8) \\ = \frac{8}{39 + 47 + 5.1} 52.1 \\ = 4.575V \end{array} \right.$$

5.5 Flyback input

The resistor in series at Pin 8 (R_{27}) must be dimensioned in order to have an input current included between 0.7mA and 2mA (typ 1mA), according with the following formula:

$$R_{27} = \frac{V_{fly} - 0.6V}{1mA}$$

6. VERTICAL SECTION

6.1 Frequency

The device is able to work form 30Hz to 120Hz.

The free running frequency is fixed by R_{21} and C_{16}.

The formula to calculate the free running frequency is the following:

$$f_v = \frac{I_C}{(V_{high} - V_{low}) \times C_{16}}$$

but

$$I_C = I = \frac{V_{12}}{R_{21}} \leq 0.5mA$$

then

$$f_v = \frac{V_{12}}{(V_{high} - V_{low}) \times C_{16} \times R_{21}}$$

where $V_{12} = 3.5V$, $V_{high} = 6.8V$ and $V_{low} = 2V$.

In the application proposed the free running frequency is:

$$f_v = \frac{3.5 \times 10^6}{(6.8 - 2) \times 220 \times 62} = 53.4Hz$$

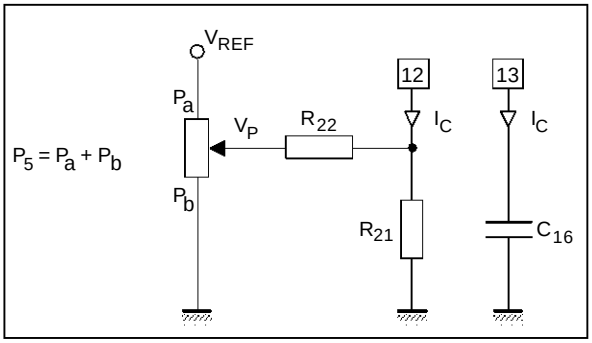
With the trimmer P_5 is possible to change the current that charges C_{16} and consequently to change the free running frequency.

The current in C_{16} due to this correction become:

$$I_C = \frac{V_{12}}{R_{21}} - \frac{V_P - V_{12}}{R_{22}}$$

where $0 \leq V_P \leq 8V$ is the voltage at the central point of the trimmer (see Figure 14).

Figure 14



It is easy to substitute the new I_C in the formula in order to obtain the new free running frequency.

6.2 Pull-in range

The vertical pull-in range is fixed by internal thresholds.

With reference to Figure 15 :

we can write :

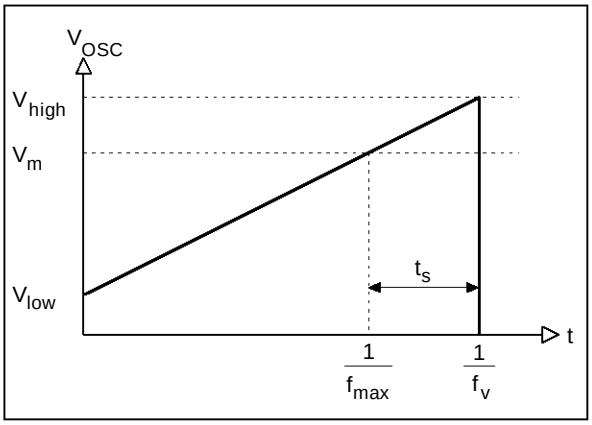
$f_{pull\ -\ in} = f_{max} - f_v$

$$f_{max} = \frac{1}{t_v - t_s}$$

$$t_s = \frac{(V_{high} - V_m)}{(V_{high} - V_{low})} \times t_v = K_{14} \times t_v$$

the value of K_{14} is 0.333 (see data-sheet).

Figure 15



6.3 Amplitude adjustment range

The voltage range accepted at pin 16 is from 0.5V to 4.5V.

So the resistor divider must be dimensioned to supply these values.

In our application we have:

$$V_{16min} = \frac{V_{19}}{R_5 + P_2 + R_6} R_6 = \frac{8}{39 + 47 + 5.1} 5.1 = 0.447V$$

$$V_{16max} = \frac{V_{19}}{R_5 + P_2 + R_6} (P_2 + R_6) = \frac{8}{39 + 47 + 5.1} 52.1 = 4.575V$$

This system allows a vertical ramp amplitude variation of ± 20% around the nominal value; the value of amplitude of vertical ramp at Pin 15 can be determined with the following formula:

$$V_{15\,pp} = [K_{16} (V_{16} - 2.5) + K_{15}]\, V_{13pp}$$

Where K_{15} is typically 1 and K_{16} is typically 0.1 (as you can see on the data-sheet).

6.4 Vertical DC reference

The average value of the vertical ramp at Pin 15 is the half of V_{19}, then with a resistive divider this DC voltage can be used as reference for the vertical booster as shown in Figure 12.

For a best noise immunity we suggest to filter V_{19} with an electrolytic capacitor.

6.5 Linearity correction

The "S" correction is performed with the new concept described in chapter 3.8.

The adjustment is obtained varying the DC voltage at Pin 17 from 1.5 to 4.5V, then the resistor divider (R3, P1 and R4) must be dimensioned for obtaining this range of values.

In our application we have:

$$V_{17min} = \frac{V_{19}}{R_3 + P_1 + R_4} R_4 = \frac{8}{51 + 47 + 22} 22 = 1.466V$$

$$V_{17max} = \frac{V_{19}}{R_3 + P_1 + R_4} (P_1 + R_4) = \frac{8}{51 + 47 + 22} 69 = 4.6V$$

The "S" correction is not performed when the voltage at Pin 17 is 1.5V, while it is maximum when the Pin 17 voltage is 4.5V.

You can verify this using the following formula:

$$V_{18pp} = K_{18} (V_{17} - 1.5)$$

where K_{18} is typically 1.

If the CRT requires a higher "S" correction, it is possible to obtain it reducing the value of R_{20}; however take care that C_{15} in series with R_{20} is a high-pass filter with the purpose to cut only the DC.

In our application we have:

$$f_t = \frac{1}{6.28 \times R_{20} \times C_{15}} = \frac{10^3}{6.28 \times 150 \times 1} = 1.06\ Hz$$

The "C" correction is obtained with a resistor in series to a capacitor connected between Pin 15 and the central point of the vertical DC feedback of vertical booster (R_{19} and C_{14}).

The value of R_{19} is strictly dependent on CRT used.

7. LAY-OUT SUGGESTIONS

It is necessary to take care not to connect the horizontal output ground (Pin 6) directly to Pin 11, to avoid horizontal interference on vertical stages.

The 15nF capacitors connected on Pins 10, 16 and 17 have the only aim to filter the DC control voltage against horizontal noise, so they must be connected as close as possible to the above mentioned pins.

8. ADJUSTING PROCEDURE

Here following it is shortly described the procedure to adjust horizontal and vertical frequencies, vertical amplitude, linearity and horizontal phase.

Before starting these operations take care that the horizontal and vertical synchronization pulses are properly applied to the device inputs.

8.1 Horizontal frequency

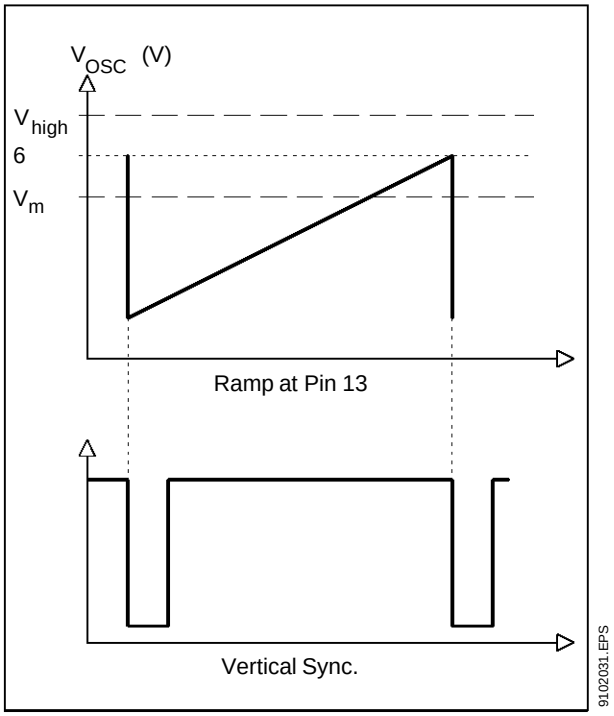
Adjust P_4 in order to obtain $V_3 = V_1$; in this way the horizontal synchronisation is perfect, and the pull-in range is maximum in both directions.

8.2 Vertical frequency

Adjust the vertical ramp amplitude using P_5 in order to have $4V_{pp}$; in this way the vertical frequency value is in the middle of the synchronization range; as shown in Figure 16.

This operation is important because some internal circuits are dimensioned for a 4_{Vpp} ramp.

Figure 16



8.3 Vertical amplitude and horizontal phase

Looking at the display correct P_2 for the right vertical amplitude and adjust P_3 in order to have the correct horizontal phase.

8.4 Vertical linearity

If the vertical ramp at Pin 13 is correctly set the central point of the "M" waveform at Pin 18 will be at the center of the scan; in other case, using P_5, lead the central point of "M" in correspondence of the scan center (see Figure 17).

where : t_S = scan time
$t_V = 1/f_V$ = vertical period
t_{SC} = scan centre
t_C = period centre

In this way the S linearity correction has a uniform behaviour on the top and bottom sides of the CRT.

Now looking at the display, adjust P_1 to obtain a right S correction and select R_{19} value to optimise the C correction.

Figure 17

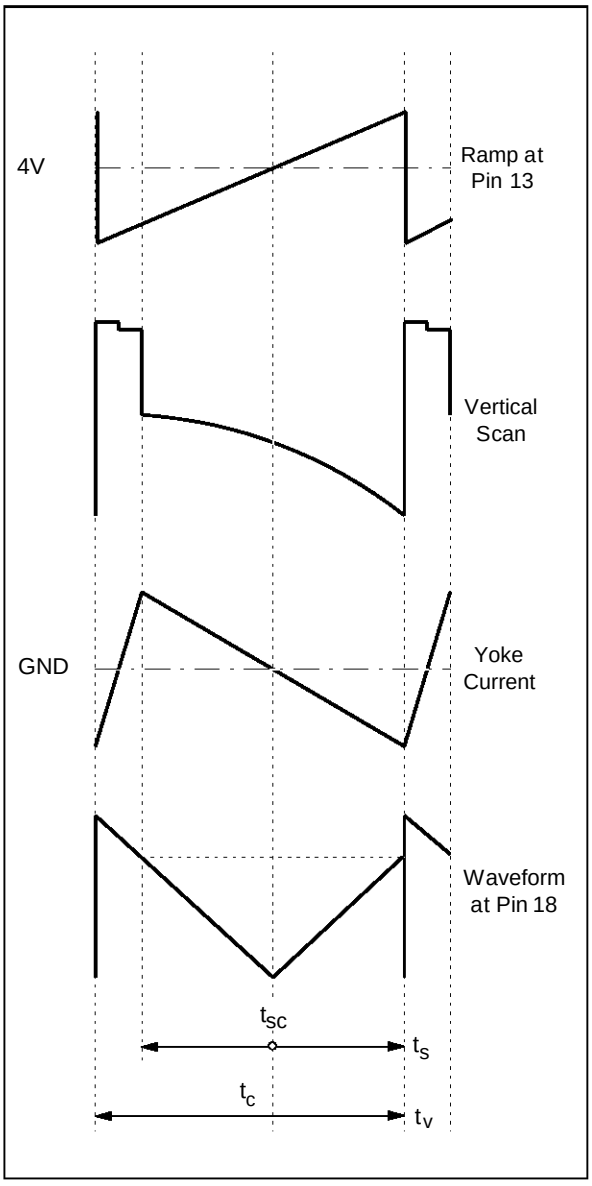
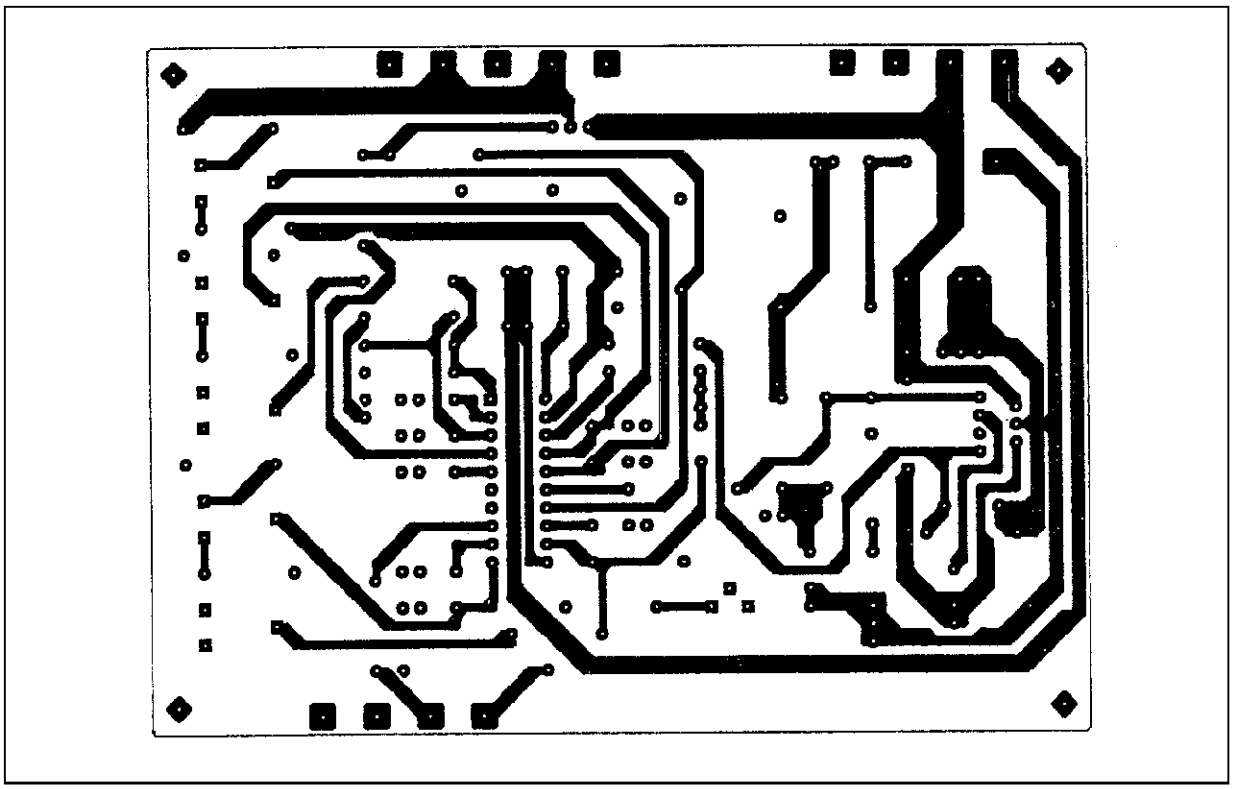
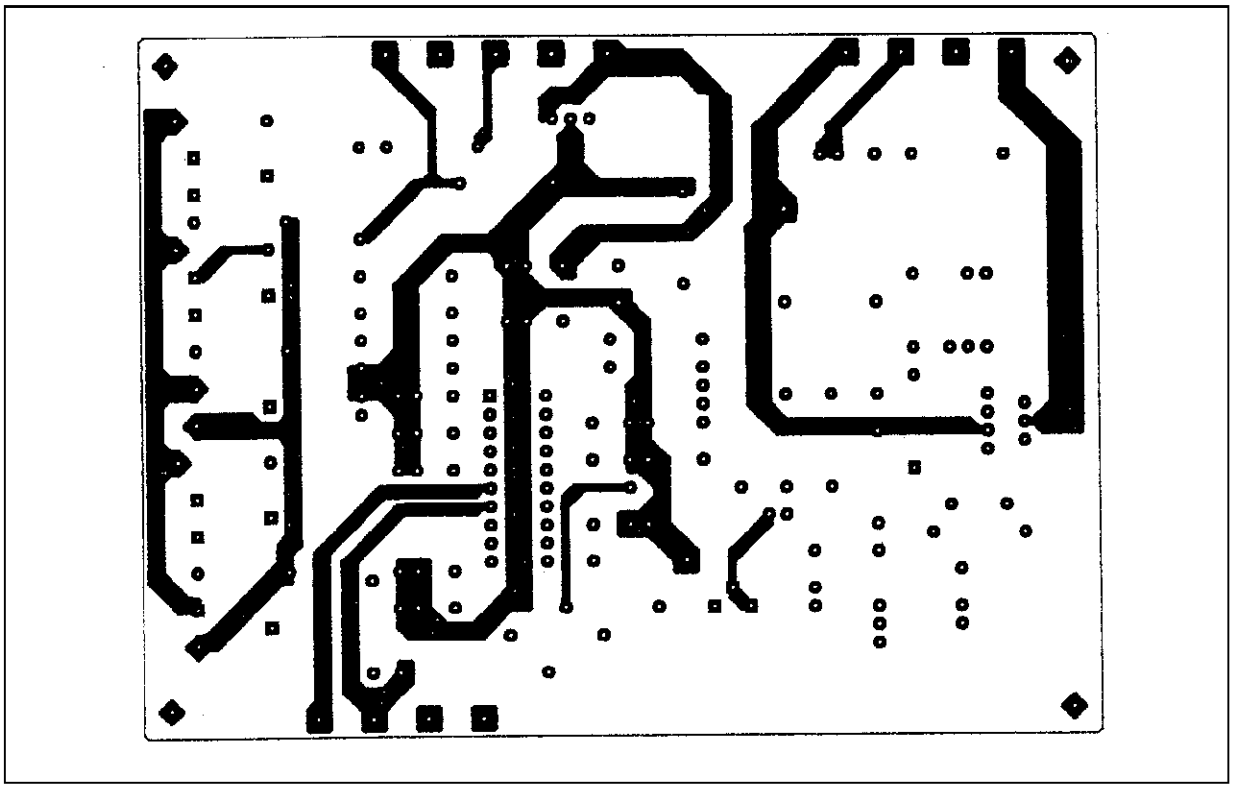


Figure 18 : Solder Side



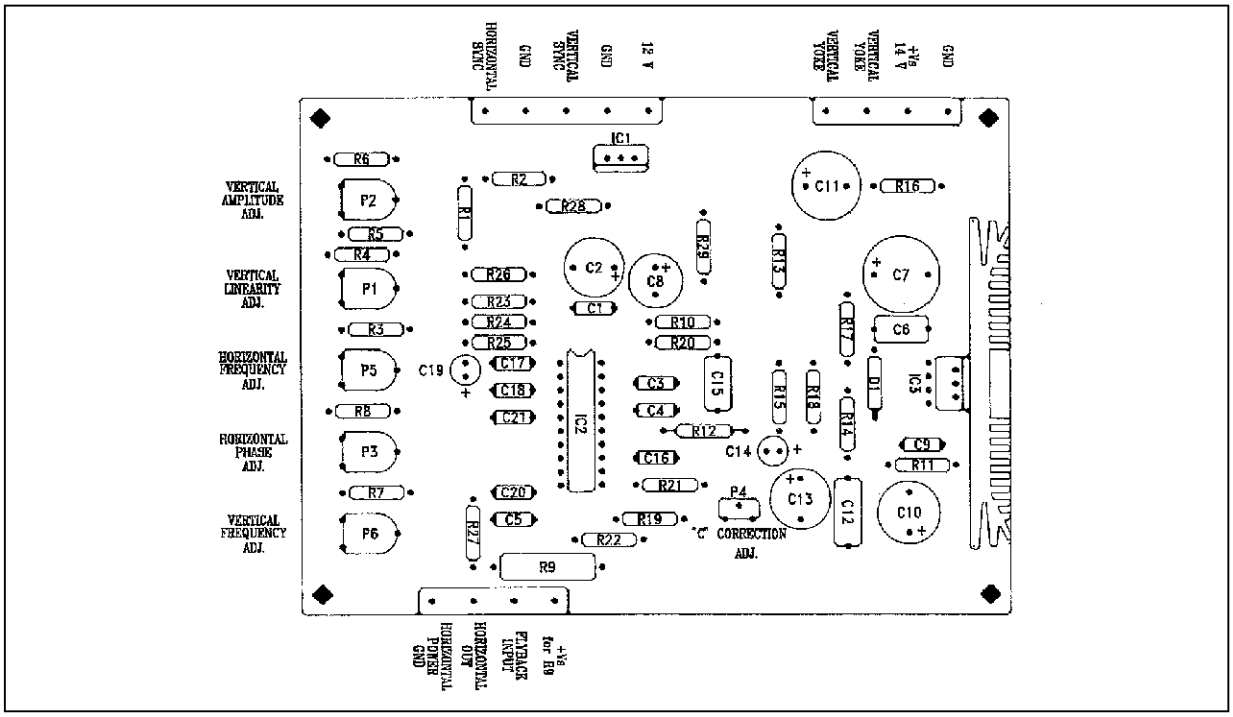
9102033.TIF

Figure 19 : Component Side



9102034.TIF

Figure 20 : PCB Layout



9102035.TIF

9. COMPONENT LIST

Component	Value	Component	Value	Component	Value
R_1, R_2, R_{23}	3.3kΩ	R_{20}	150kΩ	C_{10}	220µF / 25V
R_3	51kΩ	R_{21}	62kΩ	C_{11}	2200µF / 16V
R_4, R_{10}, R_{11}, R_{26}	22kΩ	R_{22}	220kΩ	C_{12}, C_{16}	220nF
R_5, R_7	39kΩ	R_{24}	56kΩ	C_{14}	10µF / 63V
R_6, R_8	5.1kΩ	R_{25}	6.8kΩ	C_{15}	1µF
R_9	82Ω / 2W	R_{27}	100kΩ	C_{17}	1.8nF
R_{12}	10kΩ	R_{28}, R_{29}	2.2kΩ	C_{19}	2.2µF / 63V
R_{13}	120Ω	P_1, P_2, P_3, P_5, P_6	47kΩ hor.	C_{20}	22nF
R_{14}	1.5Ω	P_4	47kΩ ver.	C_{21}	220pF
R_{15}	1.5kΩ	C_1, C_6, C_9	100nF	D_1	1N4001
R_{16}	1Ω	C_2, C_{13}	470µF / 16V	IC_1	L7812
R_{17}	2.7kΩ	C_3, C_4, C_5, C_{18}	15nF	IC_2	TDA9102
R_{18}	1.2kΩ	C_7	1000µF / 25V	IC_3	TDA8172
R_{19}	33kΩ	C_8	100µF / 16V		

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