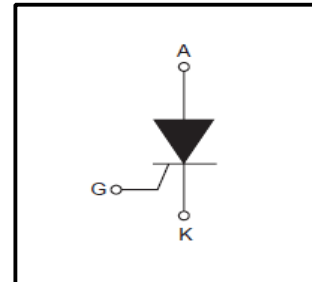


*Silicon Controlled Rectifiers*

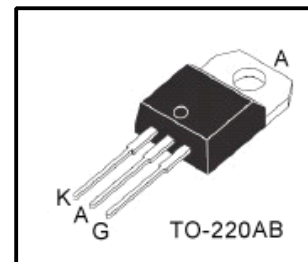
**Features**

- Repetitive Peak Off-State Voltage:600V
- R.M.S On-State Current ( $I_{T(RMS)}=25A$ )
- Low On-State Voltage(1.3V(Typ.)@ $I_{TM}$ )
- Non-isolated Type



**General Description**

Standard gate triggering SCR is fully isolated package suitable for the application where requiring high bidirectional blocking voltage capability and also suitable for over voltage protection ,motor control circuit in power tool, inrush current limit circuit and heating control system.



**Absolute Maximum Ratings** ( $T_J= 25^{\circ}C$  unless otherwise specified)

Symbol	Parameter	Condition	Value	Units
$V_{DRM}$	Repetitive Peak Off-State Voltage		600	V
$I_{T(AV)}$	Average On-State Current	Half Sine Wave: $T_C=102^{\circ}C$	16	A
$I_{T(RMS)}$	R.M.S On-State Current	180°conduction Angle	25	A
$I_{TSM}$	Non Repetitive Surge Peak on-state Current	$t_p=10ms$	300	A
		$t_p=8.3ms$	314	
$I^2t$	$I^2t$ for Fusing	$t=10ms$	450	$A^2s$
$di/dt$	Critical rate of rise of on-state current		50	$A/\mu s$
$P_{GM}$	Forward Peak Gate Power Dissipation		20	W
$P_{G(AV)}$	Forward Average Gate Power Dissipation	Over any 20ms period	1	W
$I_{FGM}$	Forward Peak Gate Current		5	A
$V_{RGM}$	Reverse Peak Gate Voltage		5	V
$T_J$	Operating Junction Temperature		-40~125	$^{\circ}C$
$T_{STG}$	Storage Temperature		-40~150	$^{\circ}C$

**Thermal Characteristics**

Symbol	Parameter	Value			Units
		Min	Typ	Max	
$R_{\theta Jc}$	Thermal Resistance Junction to Case	-	-	1.0	$^{\circ}C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	-	-	60	$^{\circ}C/W$

## Electrical Characteristics ( $T_C=25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test Conditions	Value			Units
			Min	Typ	Max	
$I_{DRM}$	Repetitive Peak Off-State Current	$V_{AK}=V_{DRM}$ $T_C=25^\circ\text{C}$	-	-	5	$\mu\text{A}$
		$T_C=125^\circ\text{C}$	-	-	2	$\text{mA}$
$V_{TM}$	Peak On-State Voltage (1)	$I_{TM}=38\text{A}$ , $t_p=380\mu\text{s}$	-	1.3	1.6	V
$I_{GT}$	Gate Trigger Current (2)	$V_D=12\text{V}$ , $R_L=30\Omega$ $T_C=25^\circ\text{C}$	3	-	25	$\text{mA}$
$V_{GT}$	Gate Trigger Voltage (2)	$V_D=12\text{V}$ , $R_L=30\Omega$ $T_C=25^\circ\text{C}$	-	-	1.3	V
$V_{GD}$	Non-Trigger Gate Voltage (1)	$V_D=V_{DRM}$ , $R_L=3.3\text{K}\Omega$ $T_J=125^\circ\text{C}$	0.2	-	-	V
dv/dt	Critical Rate of Rise Off-State Voltage	Linear slope up to $V_D=2/3V_{DRM}$ , gate open $T_J=125^\circ\text{C}$	800	-	-	$\text{V}/\mu\text{s}$
$I_H$	Holding Current	$I_T=500\text{mA}$ , Gate Open $T_C=25^\circ\text{C}$	-	-	50	$\text{mA}$
$I_L$	Dynamic resistance	$I_G=1.2I_{GT}$			60	$\text{mA}$

**\*Notes:**

1 Pulse Width  $\leq 1.0\text{ms}$ , Duty cycle  $\leq 1\%$

2  $R_{GK}$  Current is not Included in measurement.

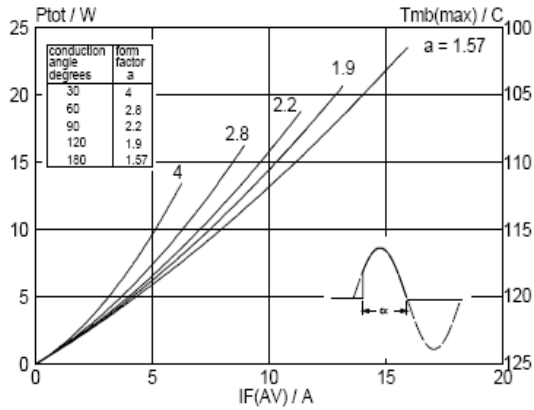


Fig. 1. Maximum on-state dissipation,  $P_{tot}$ , versus average on-state current,  $I_{T(AV)}$ , where  $a =$  form factor  $= I_{T(RMS)} / I_{T(AV)}$ .

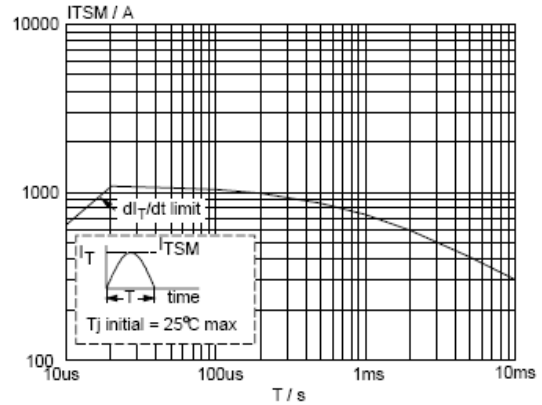


Fig. 2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 10$ ms.

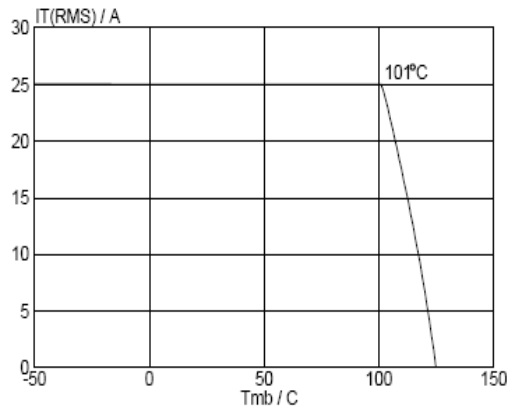


Fig. 3. Maximum permissible rms current  $I_{T(RMS)}$ , versus mounting base temperature  $T_{mb}$ .

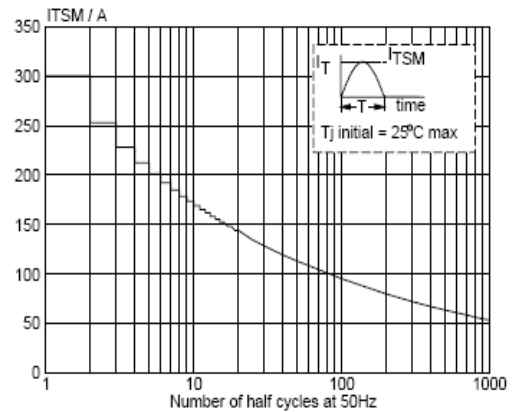


Fig. 4. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50$  Hz.

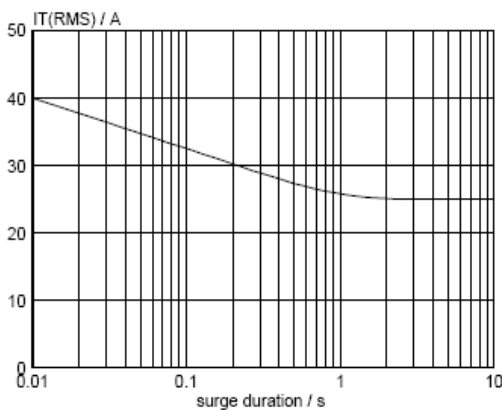


Fig. 5. Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents,  $f = 50$  Hz;  $T_{mb} \leq 101^\circ C$ .

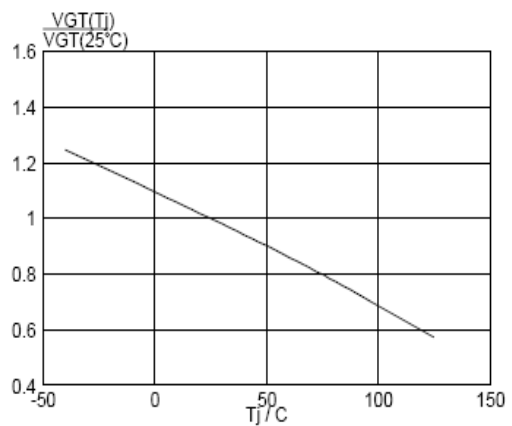


Fig. 6. Normalised gate trigger voltage  $V_{GT}(T_j) / V_{GT}(25^\circ C)$ , versus junction temperature  $T_j$ .

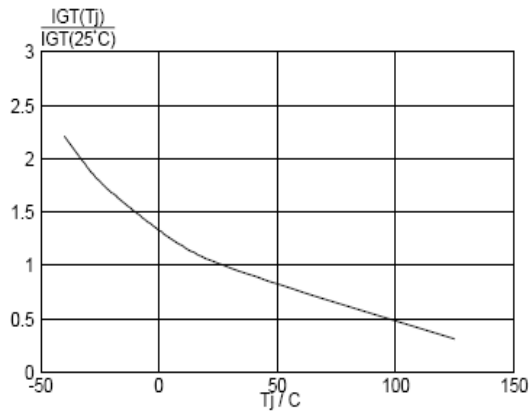


Fig. 7. Normalised gate trigger current  $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

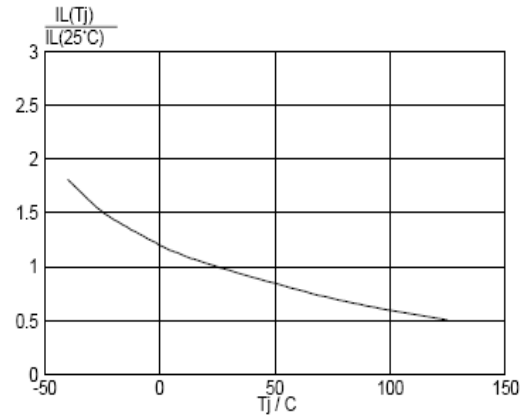


Fig. 8. Normalised latching current  $I_L(T_j)/I_L(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

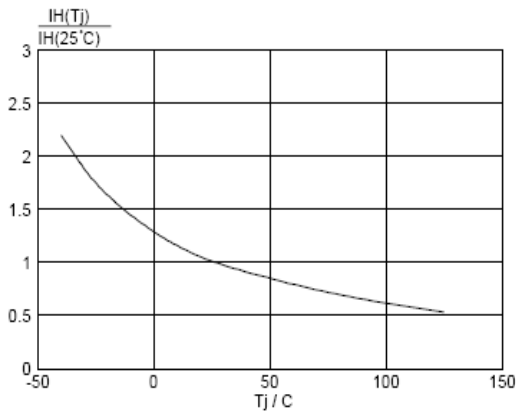


Fig. 9. Normalised holding current  $I_H(T_j)/I_H(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

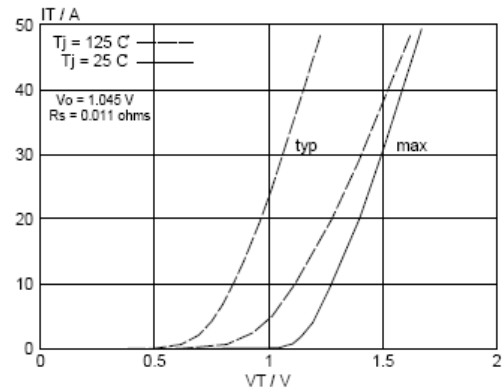


Fig. 10. Typical and maximum on-state characteristic.

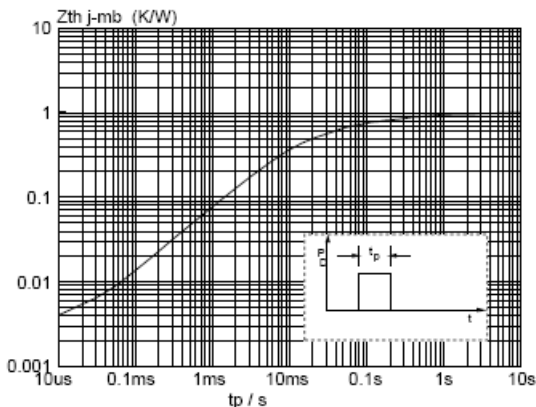


Fig. 11. Transient thermal impedance  $Z_{th(j-mb)}$ , versus pulse width  $t_p$ .

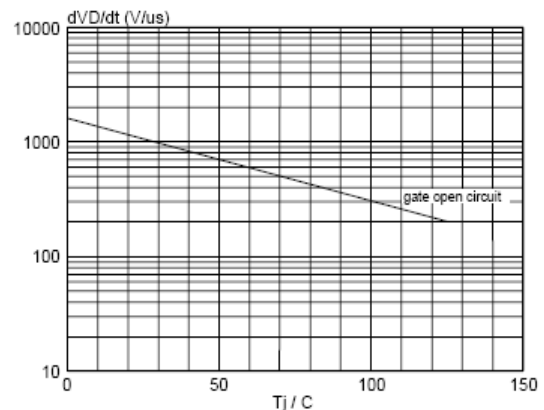


Fig. 12. Typical, critical rate of rise of off-state voltage,  $dV_D/dt$  versus junction temperature  $T_j$ .

**TO-220AB Package Dimension**

