

**TC74HCT138AP, TC74HCT138AF, TC74HCT138AFN**

**3 - TO - 8 LINE DECODER**

The TC74HCT138A is a high speed CMOS 3 - to - 8 LINE DECODER fabricated with silicon gate C<sup>2</sup>MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

When the device is enabled, 3 Binary Select inputs (A, B and C) determine which one of the outputs ( $\bar{Y}0 - \bar{Y}7$ ) will go low. When enable input G1 is held low or either  $\bar{G}2A$  or  $\bar{G}2B$  is held high, decoding function is inhibited and all outputs go high.

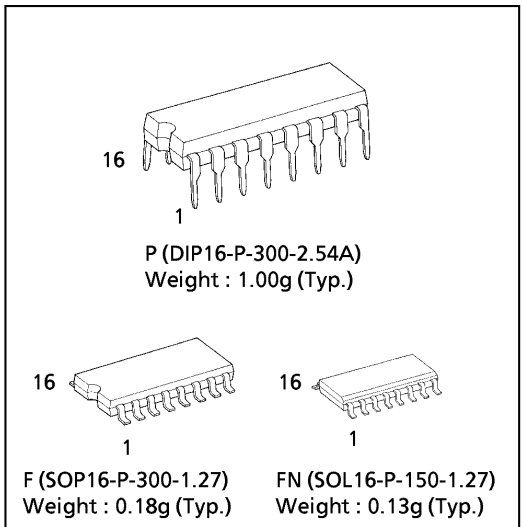
G1,  $\bar{G}2A$ , and  $\bar{G}2B$  inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

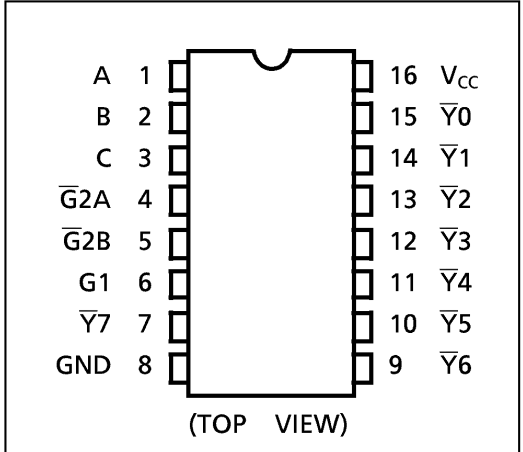
**FEATURES :**

- High Speed..... $t_{pd} = 17ns$ (typ.) at  $V_{CC} = 5V$
- Low Power Dissipation..... $I_{CC} = 4\mu A$ (Max.) at  $T_a = 25^\circ C$
- Compatible with TTL outputs..... $V_{IH} = 2V$ (Min.)  
 $V_{IL} = 0.8V$ (Max.)
- Wide interfacing ability.....LSTTL, NMOS, CMOS
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..... $|I_{OH}| = I_{OL} = 4mA$ (Min.)
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74LS138

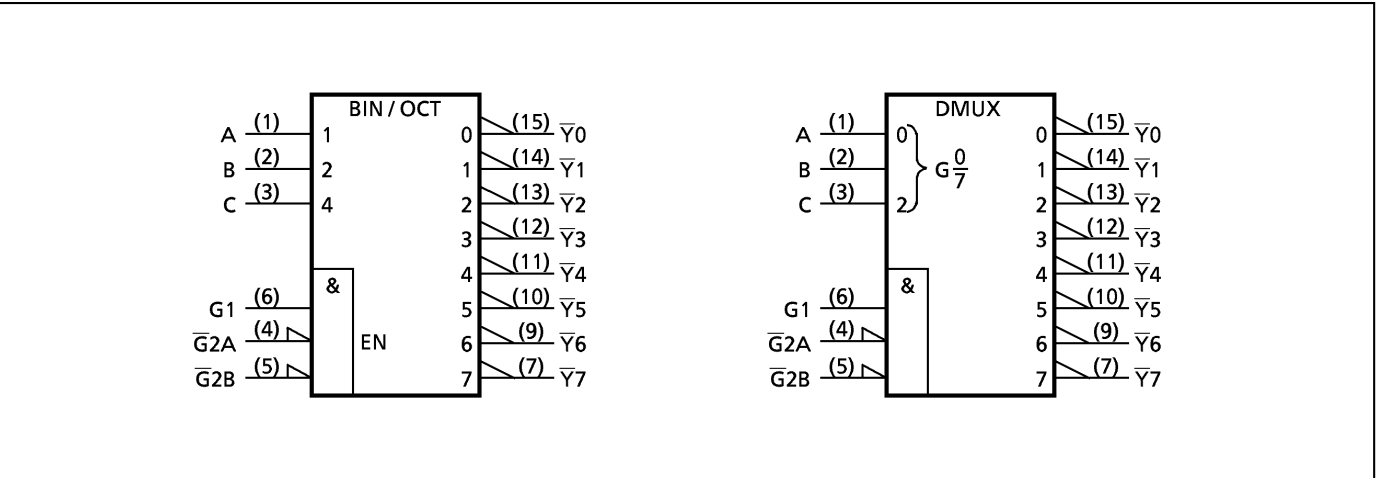
(Note) The JEDEC SOP (FN) is not available in Japan.



**PIN ASSIGNMENT**



**IEC LOGIC SYMBOL**

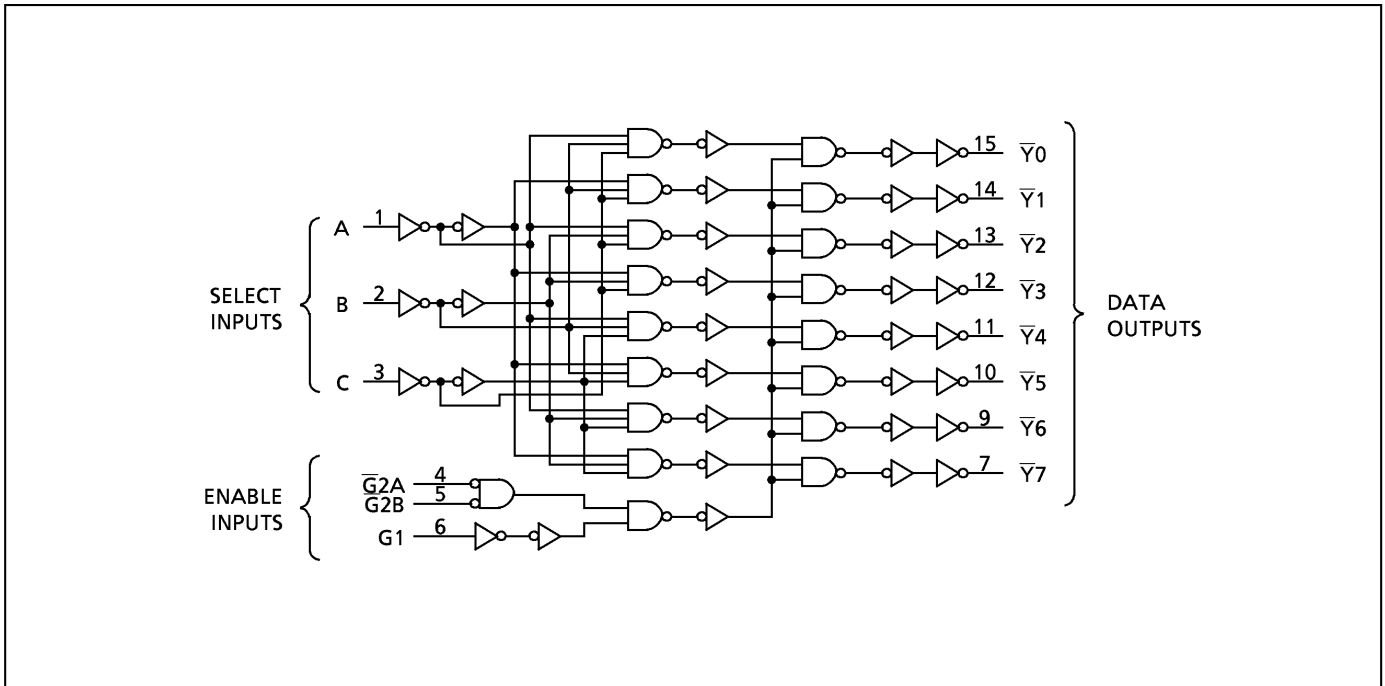


**TRUTH TABLE**

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT			$\bar{Y}0$	$\bar{Y}1$	$\bar{Y}2$	$\bar{Y}3$	$\bar{Y}4$	$\bar{Y}5$	$\bar{Y}6$	$\bar{Y}7$	
G1	$\bar{G}2A$	$\bar{G}2B$	C	B	A									
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\bar{Y}0$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\bar{Y}1$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\bar{Y}2$
H	L	L	L	H	H	H	H	L	H	H	H	H	H	$\bar{Y}3$
H	L	L	H	L	L	H	H	H	L	H	H	H	H	$\bar{Y}4$
H	L	L	H	L	H	H	H	H	H	L	H	H	H	$\bar{Y}5$
H	L	L	H	H	L	H	H	H	H	H	L	H	H	$\bar{Y}6$
H	L	L	H	H	H	H	H	H	H	H	H	L	H	$\bar{Y}7$

X : Don't Care

**LOGIC DIAGRAM**



## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7	V
DC Input Voltage	$V_{IN}$	-0.5~ $V_{CC}+0.5$	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}+0.5$	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ / Ground Current	$I_{CC}$	$\pm 50$	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	-65~150	°C

\*500mW in the range of  $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$ . From  $T_a = 65^\circ\text{C}$  to  $85^\circ\text{C}$  a derating factor of  $-10\text{mW}/^\circ\text{C}$  shall be applied until 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	4.5~5.5	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	-40~85	°C
Input Rise and Fall Time	$t_r, t_f$	0~500	ns

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	$V_{IH}$		4.5 } 5.5	2.0	—	—	2.0	—	V	
Low - Level Input Voltage	$V_{IL}$		4.5 } 5.5	—	—	0.8	—	0.8	V	
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	4.5	4.4	4.5	—	4.4	—	V
			$I_{OH} = -4 \text{ mA}$	4.5	4.18	4.31	—	4.13	—	
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$	4.5	—	0.0	0.1	—	0.1	V
			$I_{OL} = 4 \text{ mA}$	4.5	—	0.17	0.26	—	0.33	
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$	
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0		
		$I_C$	PER INPUT: $V_{IN} = 0.5\text{V}$ or $2.4\text{V}$ OTHER INPUT: $V_{CC}$ or GND	5.5	—	—	2.0	—	2.9	mA

AC ELECTRICAL CHARACTERISTICS (  $C_L = 15\text{pF}$ ,  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$ , Input  $t_r = t_f = 6\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	$t_{TLH}$ $t_{THL}$		—	4	8	ns
Propagation Delay Time (A, B, C— $\bar{Y}$ )	$t_{PLH}$ $t_{PHL}$		—	17	28	
Propagation Delay Time (G1— $\bar{Y}$ )	$t_{PLH}$ $t_{PHL}$		—	15	25	
Propagation Delay Time ( $\bar{G}2$ — $\bar{Y}$ )	$t_{PLH}$ $t_{PHL}$		—	17	28	

AC ELECTRICAL CHARACTERISTICS (  $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		UNIT	
			$V_{CC}(\text{V})$	MIN.	TYP.	MAX.	MIN.		MAX.
Output Transition Time	$t_{TLH}$ $t_{THL}$		4.5	—	8	15	—	19	ns
			5.5	—	7	14	—	18	
Propagation Delay Time (A, B, C— $\bar{Y}$ )	$t_{PLH}$ $t_{PHL}$		4.5	—	21	33	—	44	
			5.5	—	18	30	—	40	
Propagation Delay Time (G1— $\bar{Y}$ )	$t_{PLH}$ $t_{PHL}$		4.5	—	19	30	—	38	
			5.5	—	17	27	—	34	
Propagation Delay Time ( $\bar{G}2$ — $\bar{Y}$ )	$t_{PLH}$ $t_{PHL}$		4.5	—	22	33	—	41	
			5.5	—	20	30	—	37	
Input Capacitance	$C_{IN}$		—	5	10	—	10	pF	
Power Dissipation Capacitance	$C_{PD}(1)$		—	55	—	—	—		

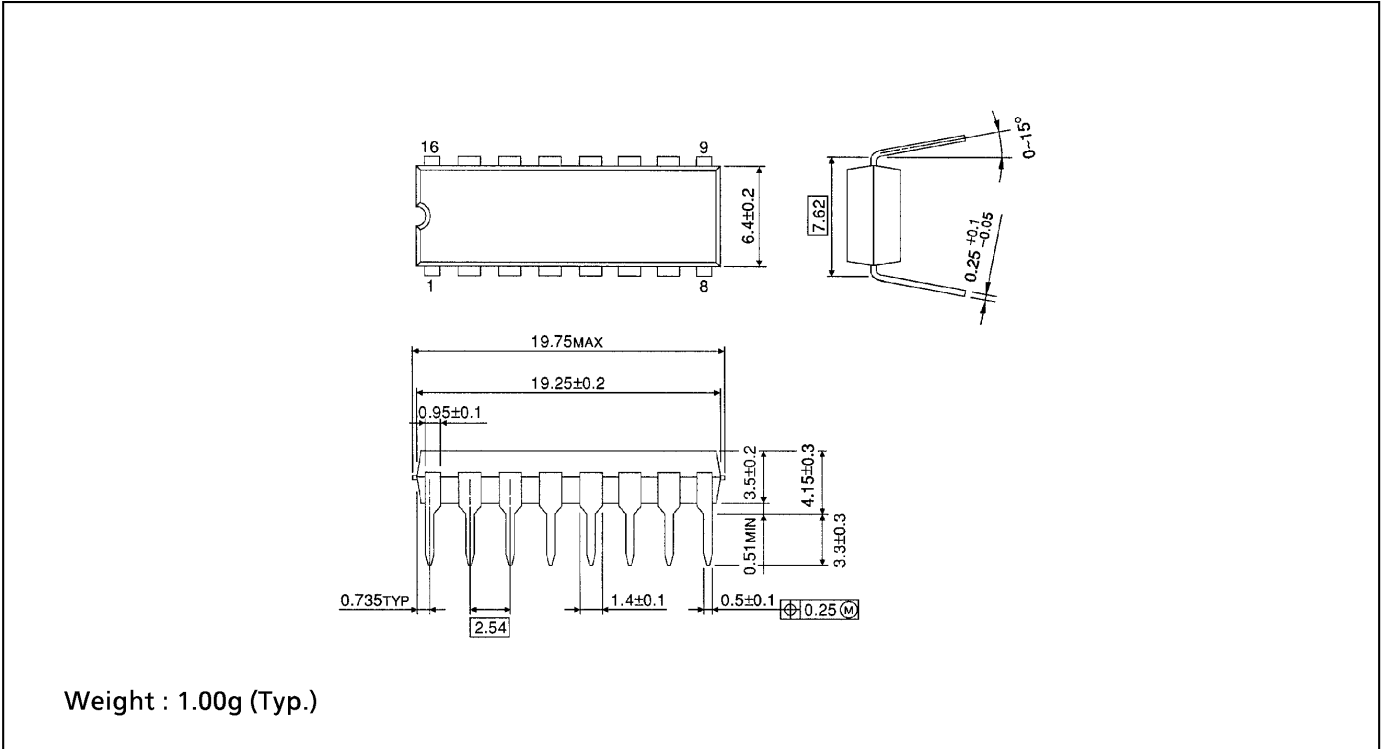
Note (1)  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

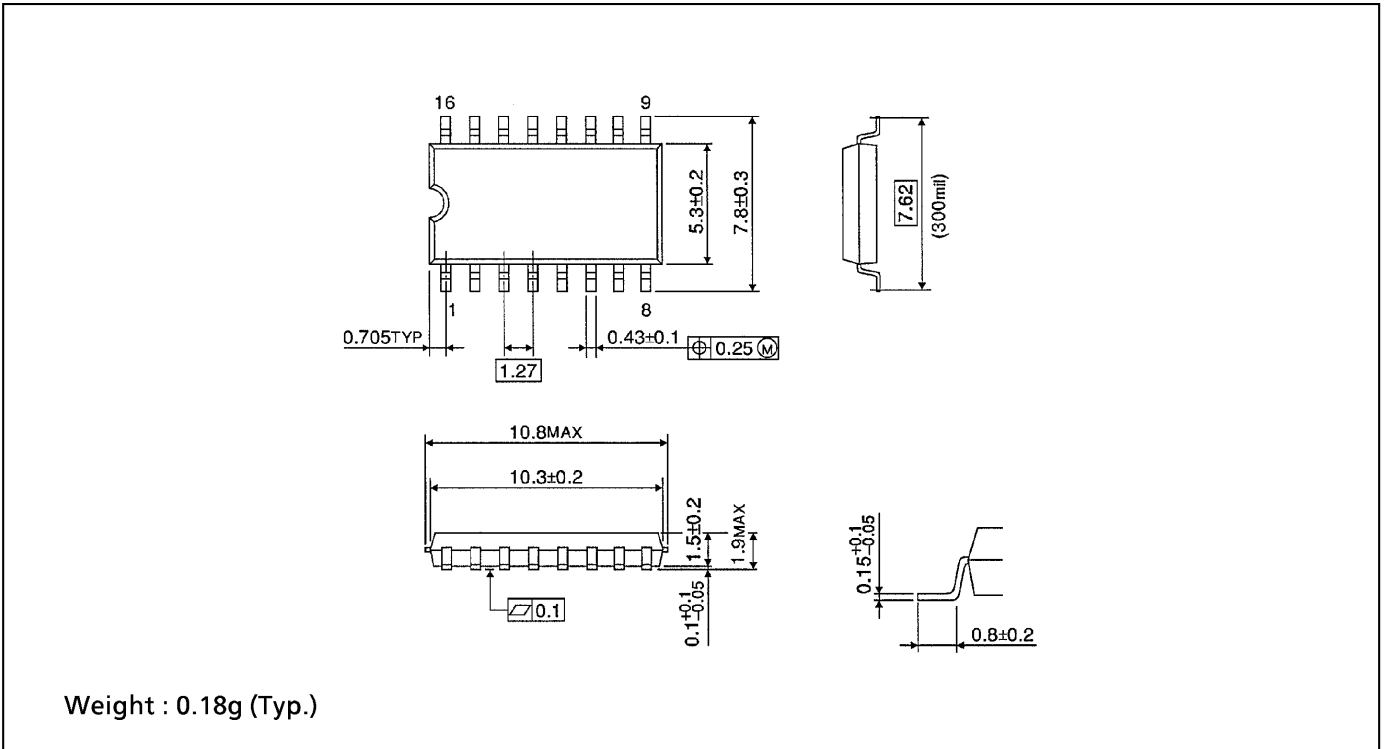
**DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)**

Unit in mm



**SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)**

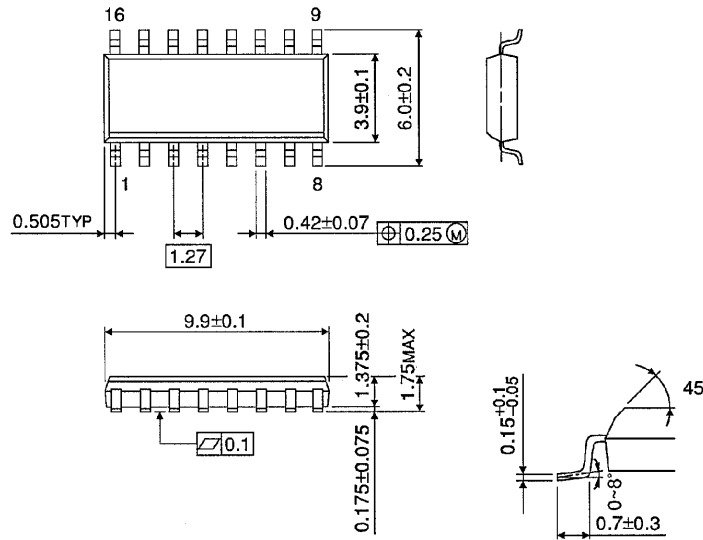
Unit in mm



**SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)**

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

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