# HMC710LC5

## GaAs MMIC I/Q UPCONVERTER 16 - 21 GHz

v03.0110

### Typical Applications

The HMC710LC5 is ideal for:

- Point-to-Point and Point-to-Multi-Point Radio
- Military Radar, EW & ELINT
- Satellite Communications
- Sensors

### Features

High Conversion Gain: 12 dB

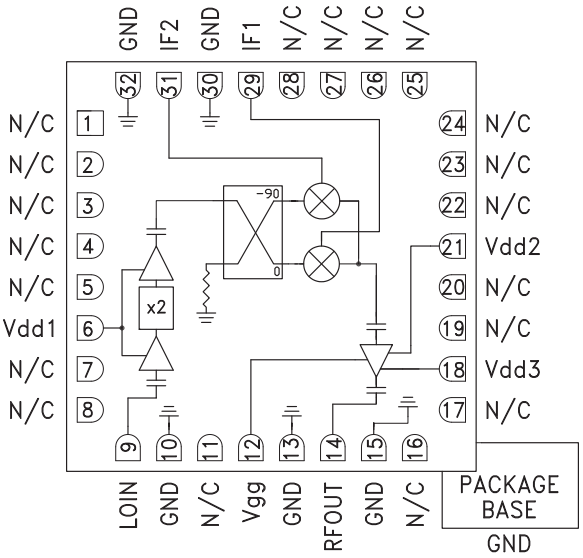
Sideband Rejection: -20 dBc

2 LO to RF Isolation: 12 dB

Output IP3: +30 dBm

32 Lead 5x5mm SMT Package: 25mm²

### Functional Diagram




### General Description

The HMC710LC5 is a compact GaAs MMIC I/Q upconverter in a leadless RoHS compliant SMT package. This device provides a small signal conversion gain of 12 dB with -20 dBc of sideband rejection. The HMC710LC5 utilizes a driver amplifier preceded by an I/Q mixer where the LO is driven by an active x2 multiplier. IF1 and IF2 mixer inputs are provided and an external 90° hybrid is needed to select the required sideband. The I/Q mixer topology reduces the need for filtering of the unwanted sideband. The HMC710LC5 is a much smaller alternative to hybrid style single sideband upconverter assemblies and it eliminates the need for wire bonding by allowing the use of surface mount manufacturing techniques.

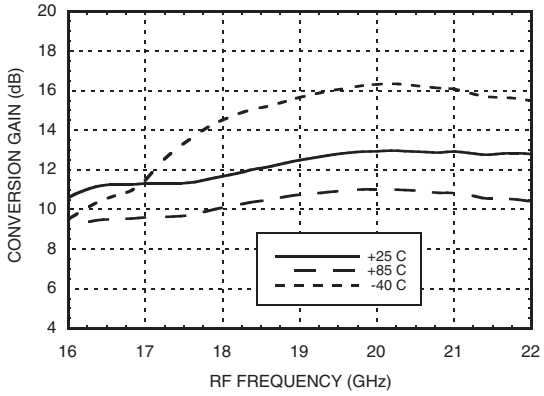
### Electrical Specifications, $T_A$ = +25 °C, IF = 1000 MHz, LO = +6 dBm, Vdd1, 2, 3 = +5V, Idd2 + Idd3 = 150 mA [1][3]

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Frequency Range, RF | | 16 - 21 | | GHz |
| Frequency Range, LO | | 7.5 - 11 | | GHz |
| Frequency Range, IF | | DC - 3.5 | | GHz |
| Conversion Gain | 7 | 12 | | dB |
| Sideband Rejection | -12 | -20 | | dBc |
| 1 dB Compression (Output) | | 20 | | dBm |
| 2 LO to RF Isolation | | 12 | | dB |
| 2 LO to IF Isolation [2] | | 20 | | dB |
| IP3 (Output) | | 30 | | dBm |
| Supply Current Idd1 | 52 | 90 | 108 | mA |
| Supply Current Idd2 | 24 | 30 | | mA |
| Supply Current Idd3 | 96 | 120 | | mA |

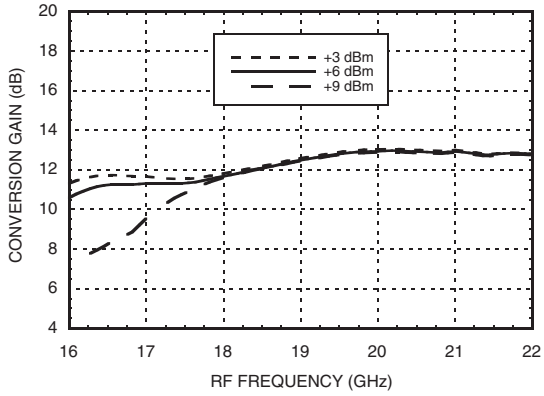
[1] Unless otherwise noted all measurements performed with high side LO, IF = 1000 MHz and external 90° IF hybrid.
[2] Data taken without external IF hybrid.
[3] Adjust Vgg between -2 to 0V to achieve Idd2 + Idd3 = 150 mA Typical.

## Data Taken as SSB Upconverter with External IF Hybrid

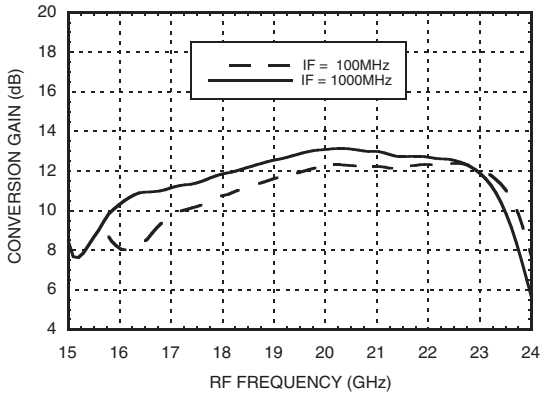
### Conversion Gain vs. Temperature



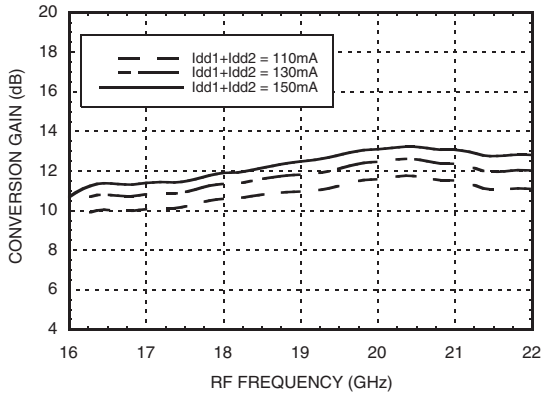

### Conversion Gain vs. LO Drive



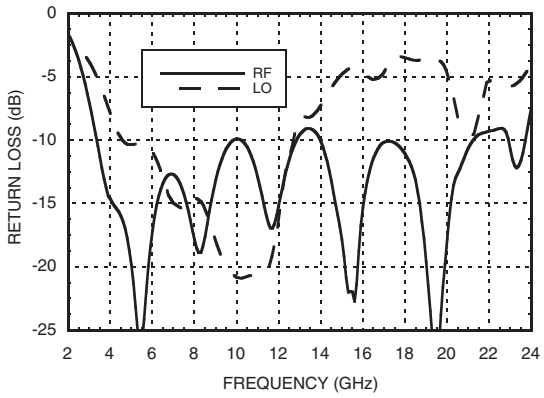

### Conversion Gain vs. IF Frequency



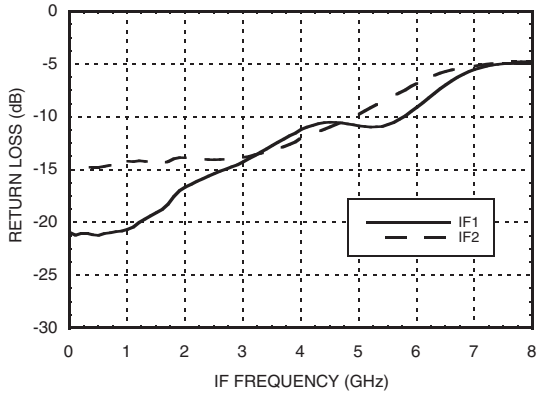

### Conversion Gain vs. Idd2 + Idd3




### RF, LO Return Loss



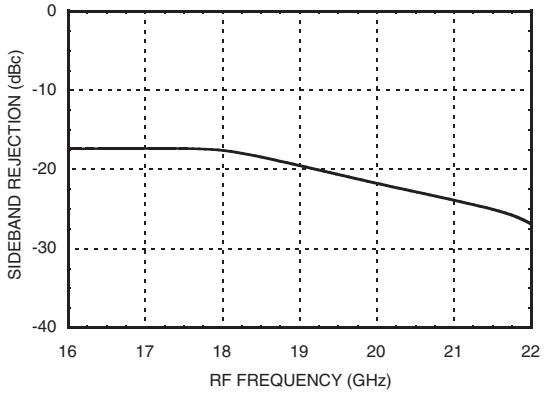

### IF Return Loss [1]



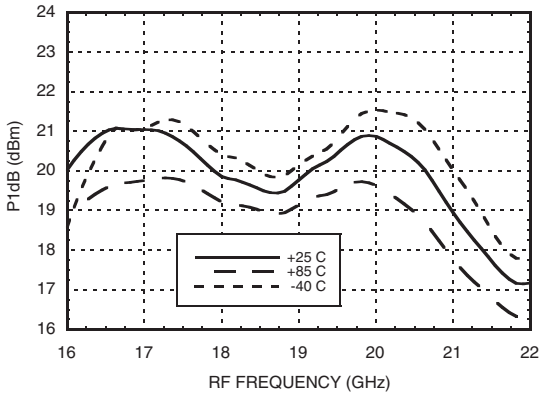

[1] Data taken without external IF hybrid

## Data Taken as SSB Upconverter with External IF Hybrid

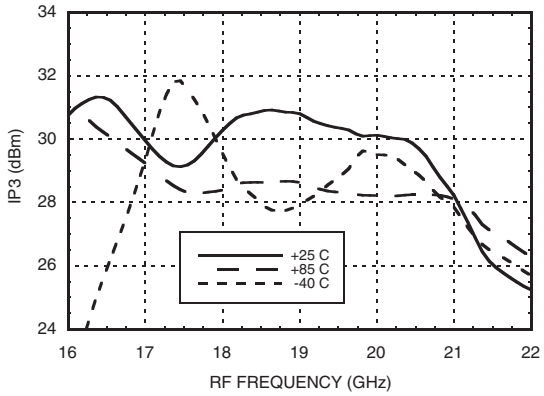
### Side Band Rejection



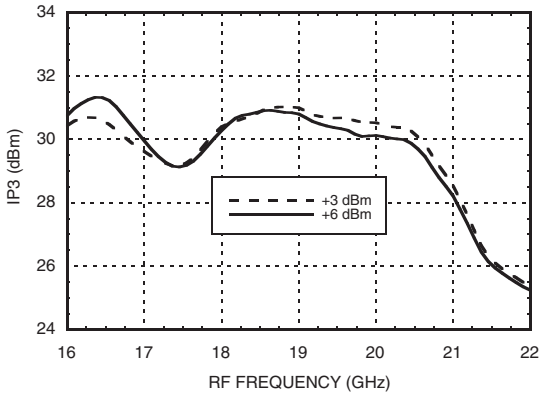

### Output P1dB vs. Temperature



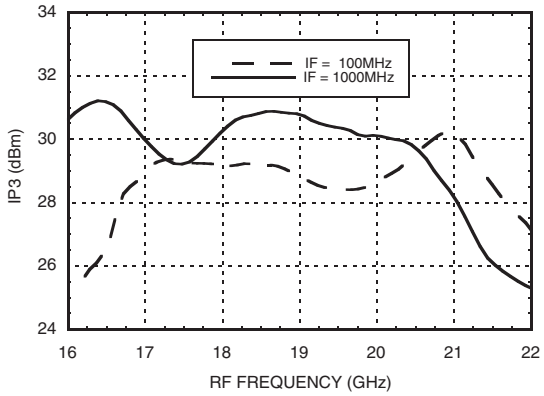

### Output IP3 vs. Temperature



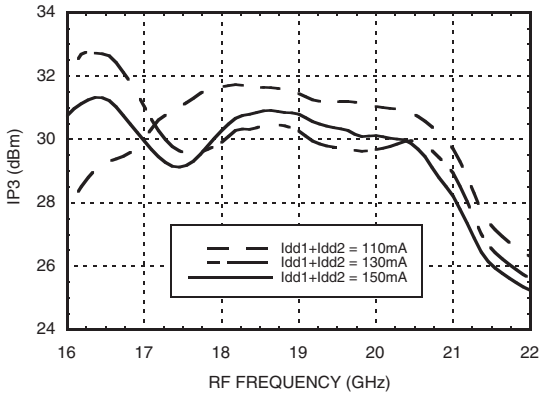

### Output IP3 vs. LO Drive



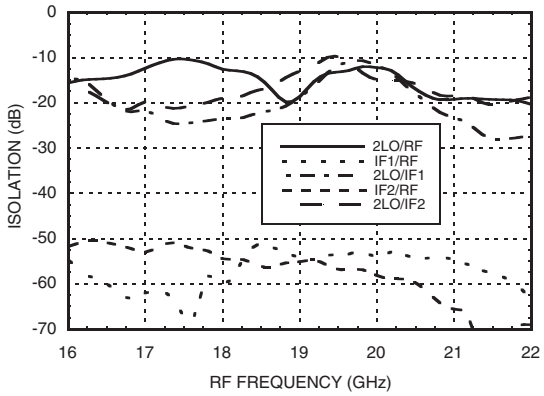

### Output IP3 vs. IF Frequency



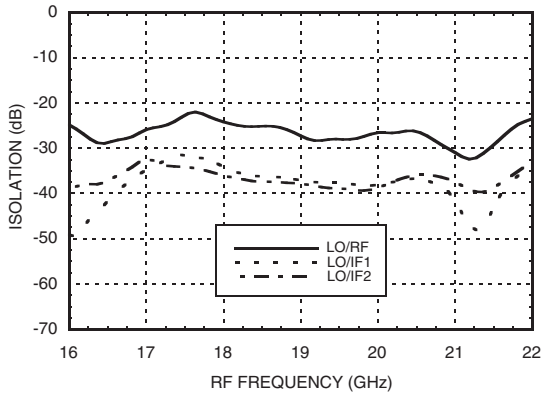

### Output IP3 vs. Idd2 + Idd3



### Isolations with 2LO [1]




### Isolations with LO [1]




### MxN Spurious Outputs [1]

| | nLO | | | | |
|---|---|---|---|---|---|
| mIF | 0 | 1 | 2 | 3 | 4 |
| 0 | xx | 19 | 48 | xx | xx |
| 1 | 61 | 0 | 66 | xx | xx |
| 2 | 35 | 32 | 53 | xx | xx |
| 3 | 61 | 38 | 72 | xx | xx |
| 4 | 52 | 62 | 73 | xx | xx |

IF = 1 GHz @ 0 dBm
LO = 9.75 GHz @ +6 dBm
Data taken without IF hybrid
All values in dBc below RF power level (-1IF + 2LO)

### Harmonics of LO

| LO Freq. (GHz) | nLO Spur @ IF Port | | | |
|---|---|---|---|---|
| | 1 | 2 | 3 | 4 |
| 8 | 42 | 21 | 25 | 64 |
| 9 | 35 | 24 | 47 | 50 |
| 10 | 38 | 19 | 49 | 47 |
| 11 | 42 | 25 | 44 | 51 |
| 12 | 34 | 18 | 50 | xx |
| 13 | 39 | 32 | 55 | xx |
| 14 | 22 | 35 | 52 | xx |

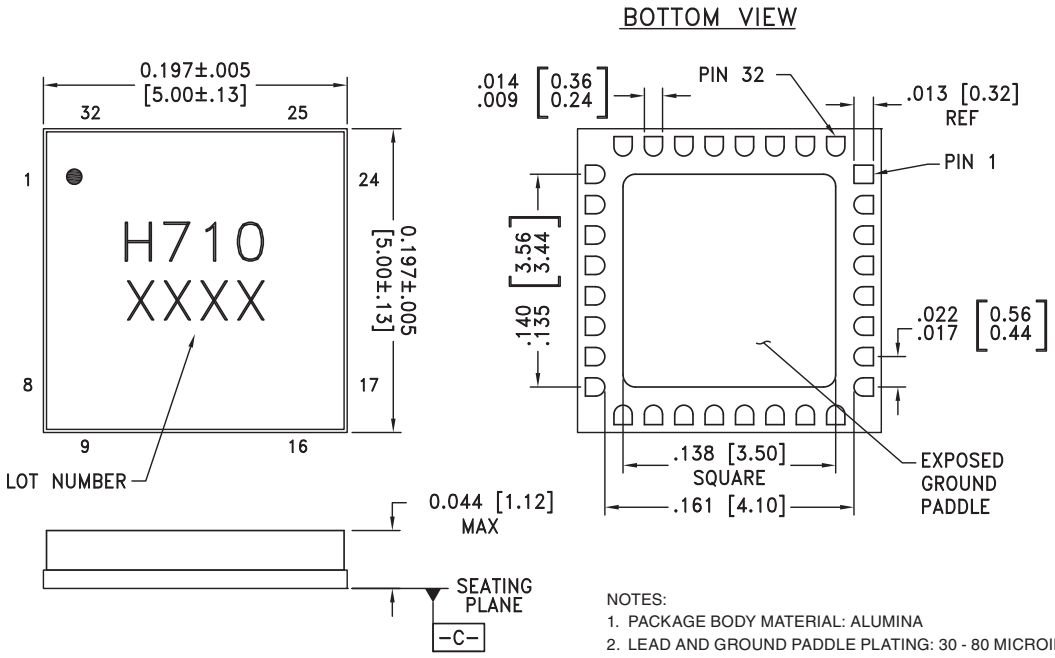
[1] Data taken without external IF hybrid

## Absolute Maximum Ratings

| | |
|---|---|
| Drain Bias Voltage (Vdd1, 2, 3) | 5.25V |
| Gate Bias Voltage (Vgg) | -3 to 0V |
| IF Input Power (IF1, IF2) | 20 dBm |
| LO Drive (LO IN) | 20 dBm |
| Channel Temperature | 175 °C |
| Continuous Pdiss (T = 85°C) (derate 16.2 mW/°C above 85°C) | 1.46 mW |
| Thermal Resistance (channel to ground paddle) | 61.8 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -55 to +85 °C |
| ESD Sensitivity (HBM) | Class 1A |

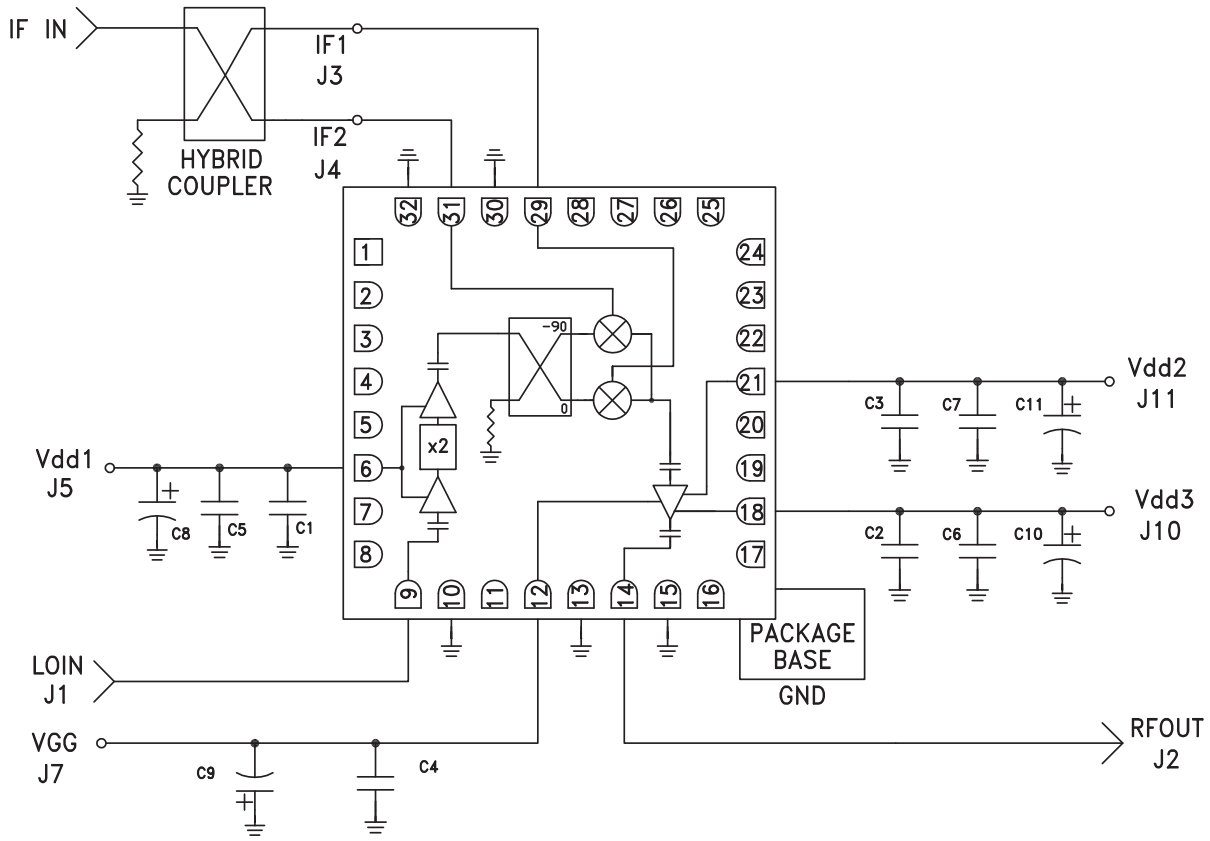
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

## Outline Drawing



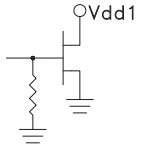
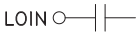
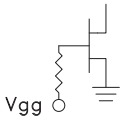
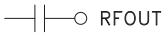
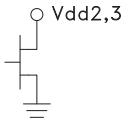
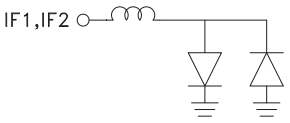

NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30 - 80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKLE
3. DIMENSIONS ARE IN INCHES [MILLIMETERS]
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND

## Typical Application

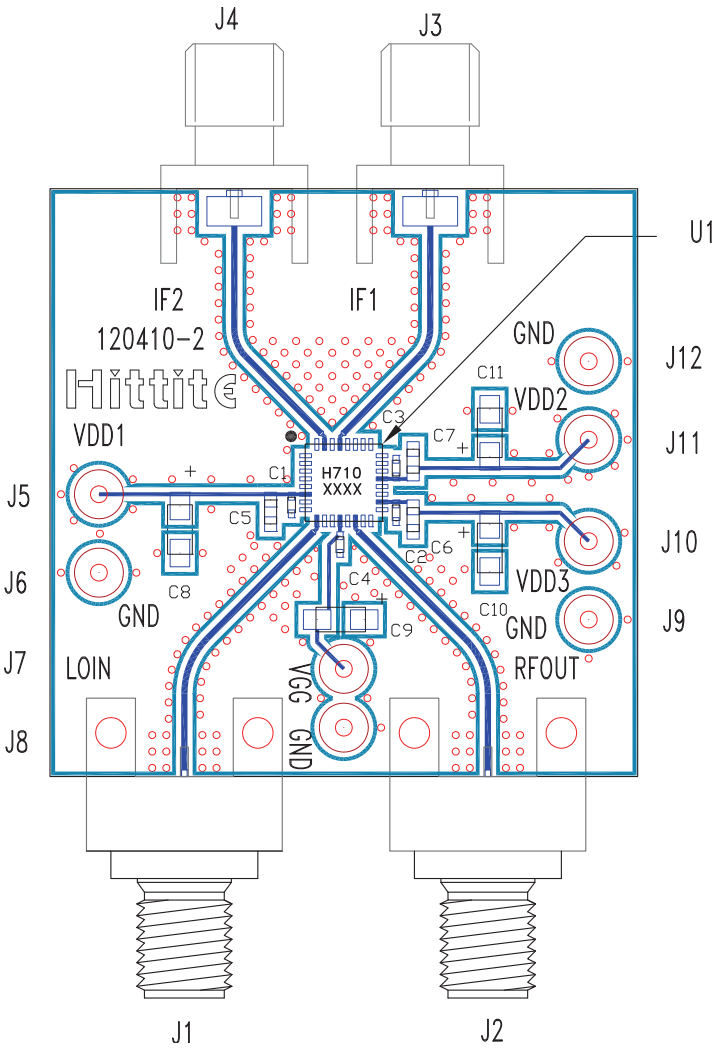



| | |
|---|---|
| C1 - C3 | 100 pF |
| C4 - C7 | 1000 pF |
| C8 - C11 | 2.2 µF |

## Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1 - 5, 7, 8, 11, 16, 17, 19, 20, 22 - 28 | N/C | No Connection required. These pins may be connected to RF/DC ground without affecting performance. | |
| 6 | Vdd1 | Power supply voltage for x2 multiplier. See application circuit for required external components. |   |
| 9 | LOIN | This pin is AC coupled and matched to 50 Ohms. |   |
| 10, 13, 15, 30, 32 | GND | These pins and package bottom must be connected to RF/DC ground. |   |
| 12 | Vgg | Gate control for RF amplifier, please follow “MMIC Amplifier Biasing Procedure” application note. See application circuit for required external components |   |
| 14 | RFOUT | This pin is AC coupled and matched to 50 Ohms. |   |
| 18, 21 | Vdd2, Vdd3 | Power supply voltage for RF amplifier. See application circuit for required external components. |   |
| 29 | IF1 | Differential IF input pins. For applications not requiring operation to DC, an off chip DC blocking capacitor should be used. For operation to DC this pin must not source/sink more than 3mA of current or part non function and possible part failure will result. |   |
| 31 | IF2 | | |

## Evaluation PCB




## List of Materials for Evaluation PCB 120412 [1]

| Item | Description |
|---|---|
| J1, J2 | PCB Mount SMA SRI Connector |
| J3, J4 | PCB Mount SMA Connector |
| J5 - J12 | DC Pin |
| C1 - C3 | 100 pF Capacitor, 0402 Pkg. |
| C4 | 1000 pF Capacitor, 0402 Pkg. |
| C5 - C7 | 1000 pF Capacitor, 0603 Pkg. |
| C8 - C11 | 2.2 µF Tantalum Capacitor Case A |
| U1 | HMC710LC5 Upconverter |
| PCB [2] | 120410 Evaluation Board |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR, FR4

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.