

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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# HAT2042T

## Silicon N Channel Power MOS FET High Speed Power Switching

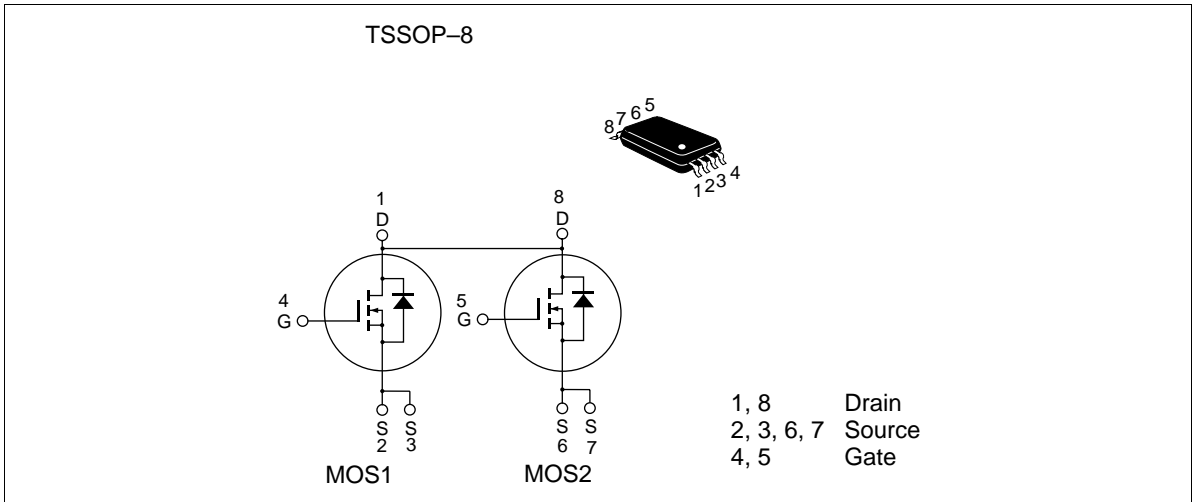
# RENESAS

ADE-208-669F (Z)  
7th. Edition  
Feb. 1999

### Features

- Low on-resistance
- Capable of 2.5 V gate drive
- Low drive current
- High density mounting

### Outline



## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	28	V
Gate to source voltage	$V_{GSS}$	$\pm 12$	V
Drain current	$I_D$	5.0	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	40	A
Body-drain diode reverse drain current	$I_{DR}$	5.0	A
Channel dissipation	Pch <sup>Note2</sup>	1.0	W
Channel dissipation	Pch <sup>Note3</sup>	1.5	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	- 55 to + 150	°C

Note: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$

2. 1 Drive operation ; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm),  $PW \leq 10 s$

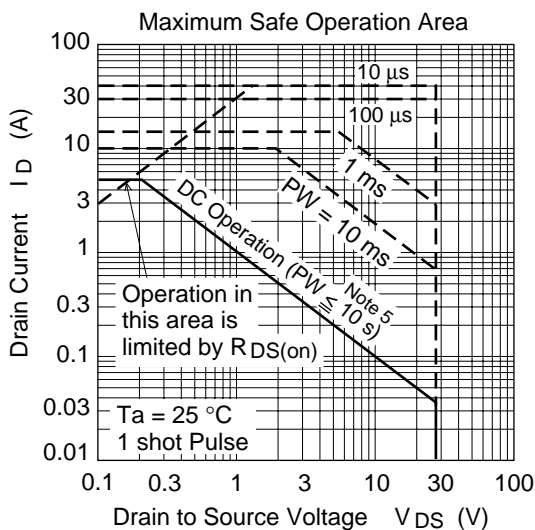
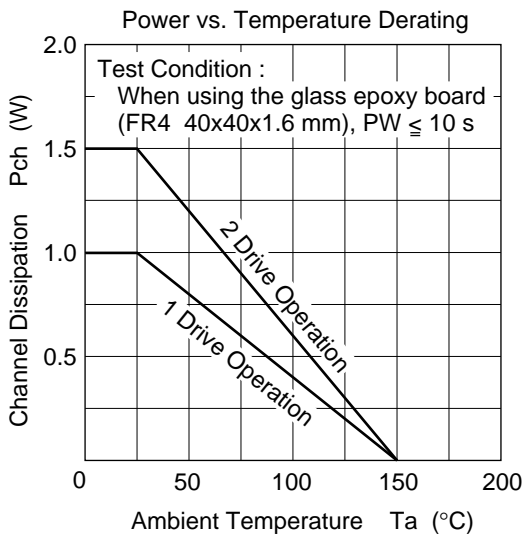
3. 2 Drive operation ; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm),  $PW \leq 10 s$

## Electrical Characteristics (Ta = 25°C)

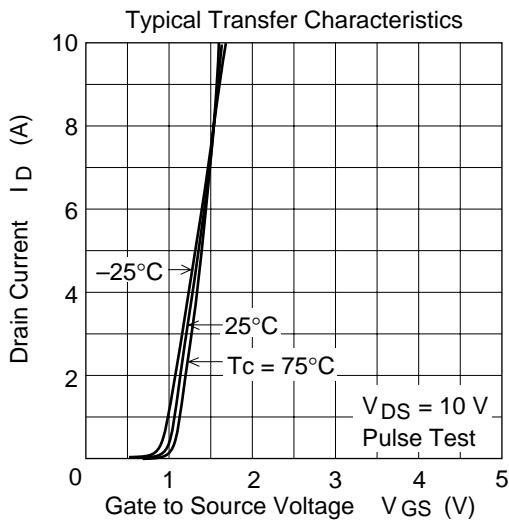
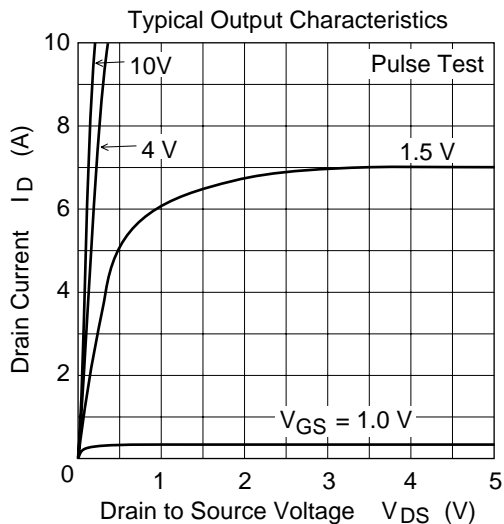
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	28	—	—	V	$I_D = 10mA, V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu A$	$V_{GS} = \pm 12 V, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu A$	$V_{DS} = 28 V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.4	—	1.4	V	$V_{DS} = 10 V, I_D = 1 mA$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.027	0.034	$\Omega$	$I_D = 3 A, V_{GS} = 4 V$ <sup>Note4</sup>
	$R_{DS(on)}$	—	0.037	0.044	$\Omega$	$I_D = 3 A, V_{GS} = 2.5 V$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	7	11	—	S	$I_D = 3 A, V_{DS} = 10 V$ <sup>Note4</sup>
Input capacitance	Ciss	—	510	—	pF	$V_{DS} = 10 V$
Output capacitance	Coss	—	190	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	140	—	pF	$f = 1 MHz$
Total gate charge	Qg	—	8.5	—	nc	$V_{DD} = 10 V$
Gate to source charge	Qgs	—	4.5	—	nc	$V_{GS} = 4 V$
Gate to drain charge	Qgd	—	4	—	nc	$I_D = 5 A$
Turn-on delay time	$t_{d(on)}$	—	14	—	ns	$V_{GS} = 4 V, I_D = 3 A$
Rise time	$t_r$	—	120	—	ns	$V_{DD} \cong 10 V$
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	
Fall time	$t_f$	—	120	—	ns	
Body–drain diode forward voltage	$V_{DF}$	—	0.85	1.1	V	$IF = 5.0 A, V_{GS} = 0$ <sup>Note4</sup>
Body–drain diode reverse recovery time	$t_{rr}$	—	40	—	ns	$IF = 5.0 A, V_{GS} = 0$ $diF/dt = 20 A/\mu s$

Note: 4. Pulse test

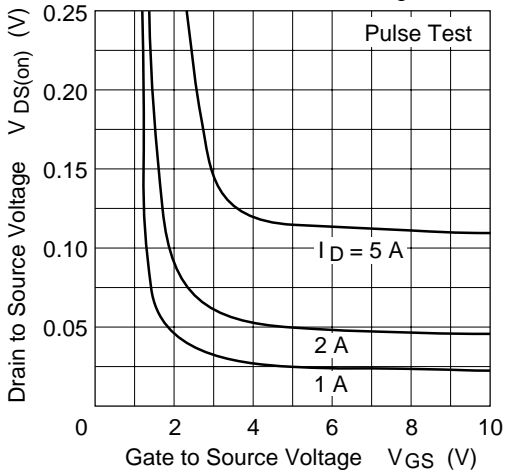
Main Characteristics



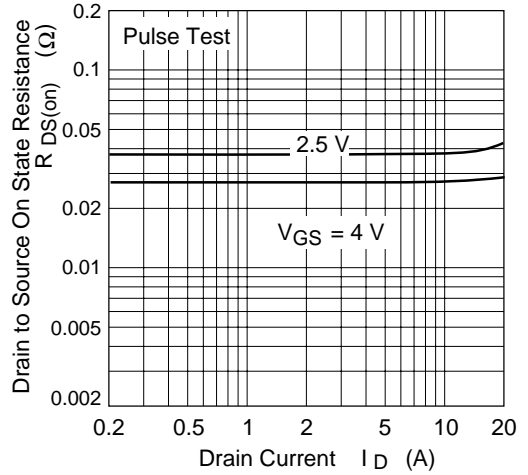
Note 5 :  
When using the glass epoxy board (FR4 40x40x1.6 mm)



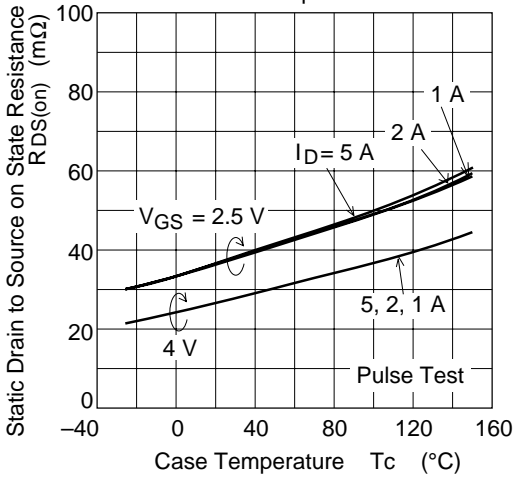
Drain to Source Saturation Voltage vs. Gate to Source Voltage



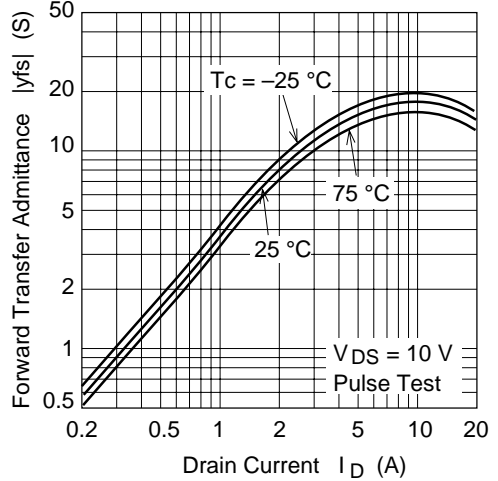
Static Drain to Source on State Resistance vs. Drain Current



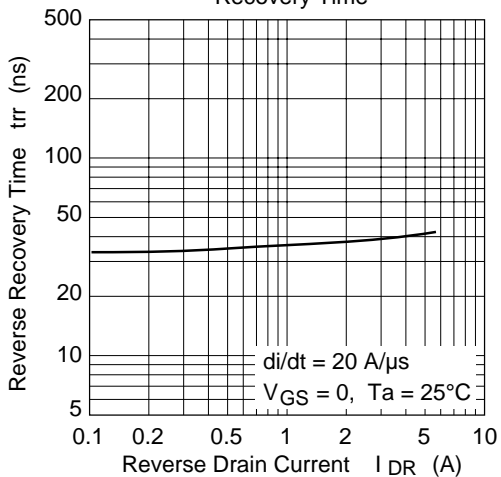
Static Drain to Source on State Resistance vs. Temperature



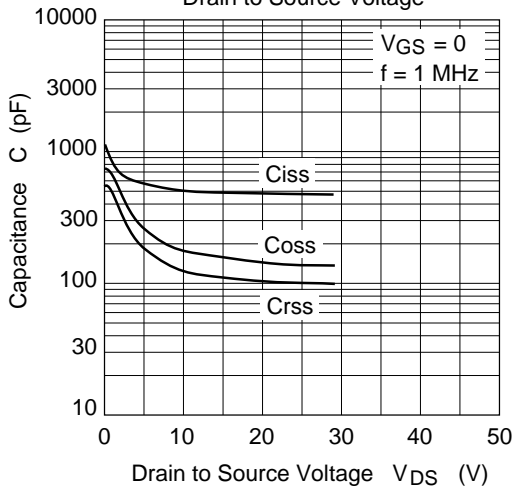
Forward Transfer Admittance vs. Drain Current



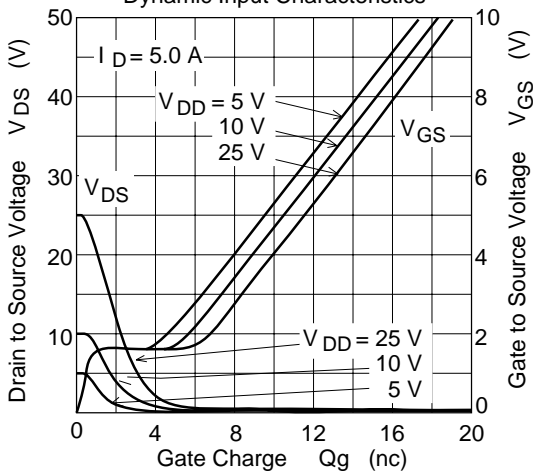
Body-Drain Diode Reverse Recovery Time



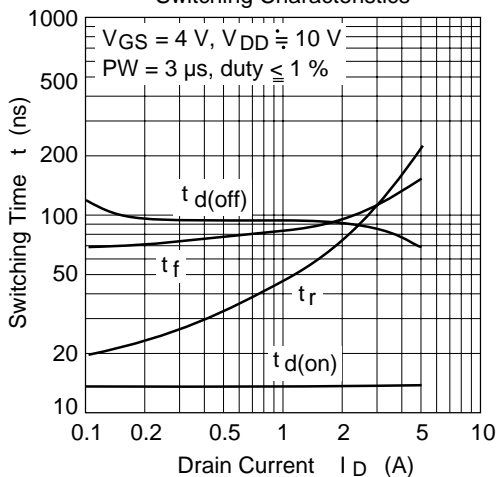
Typical Capacitance vs. Drain to Source Voltage

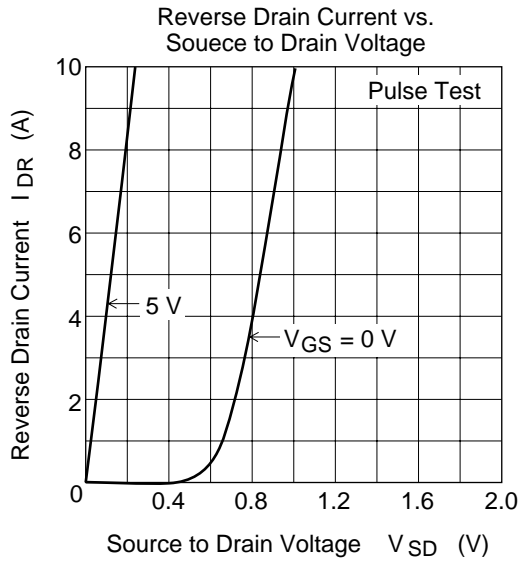


Dynamic Input Characteristics

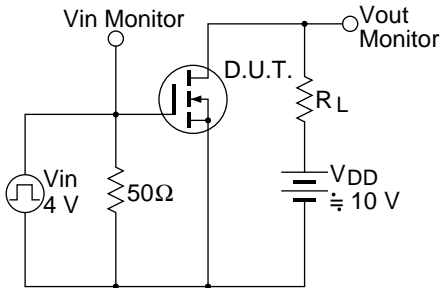


Switching Characteristics

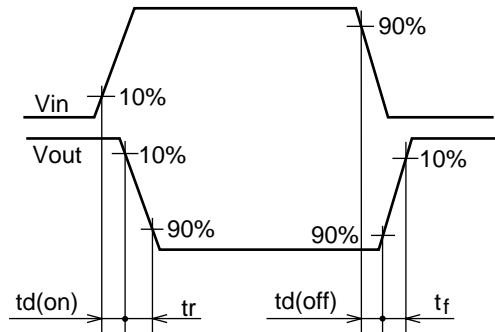




Switching Time Test Circuit

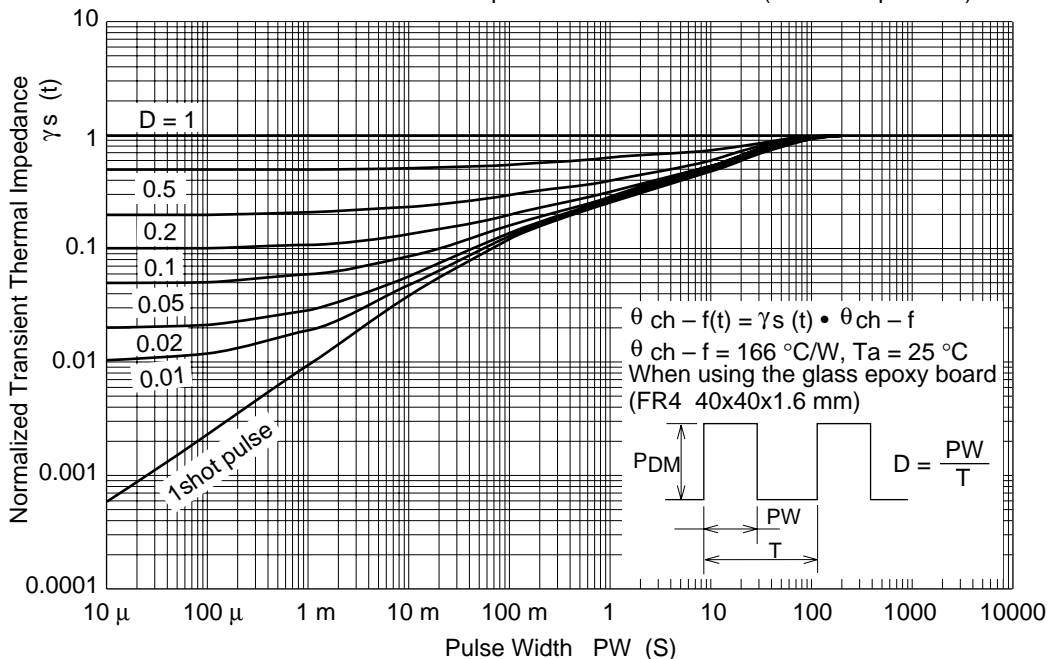


Switching Time Waveform

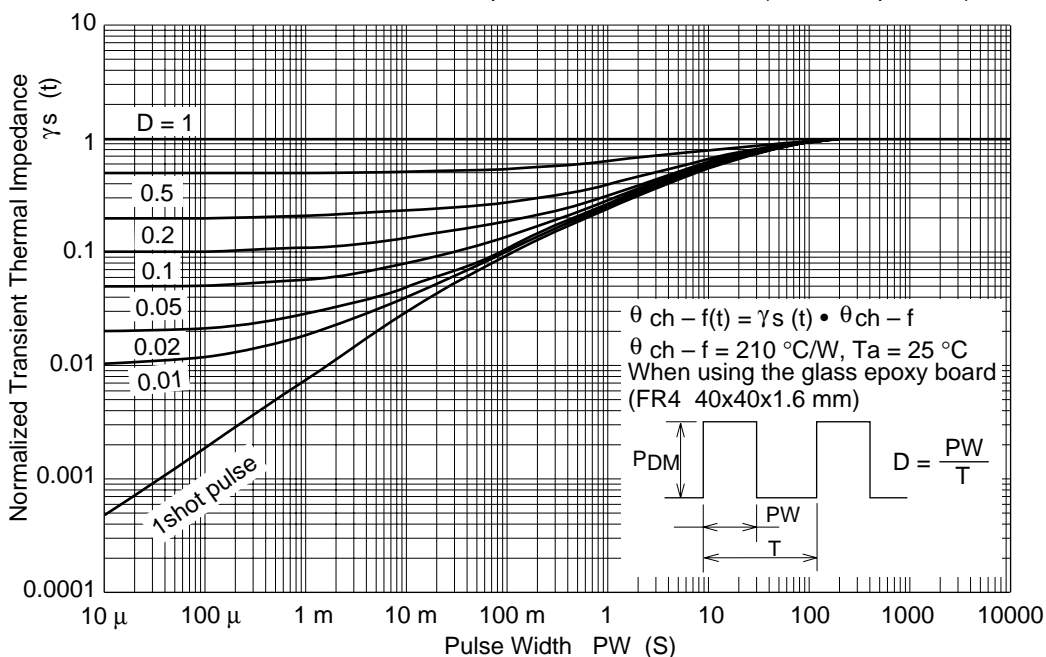




Normalized Transient Thermal Impedance vs. Pulse Width ( 1 Drive Operation)



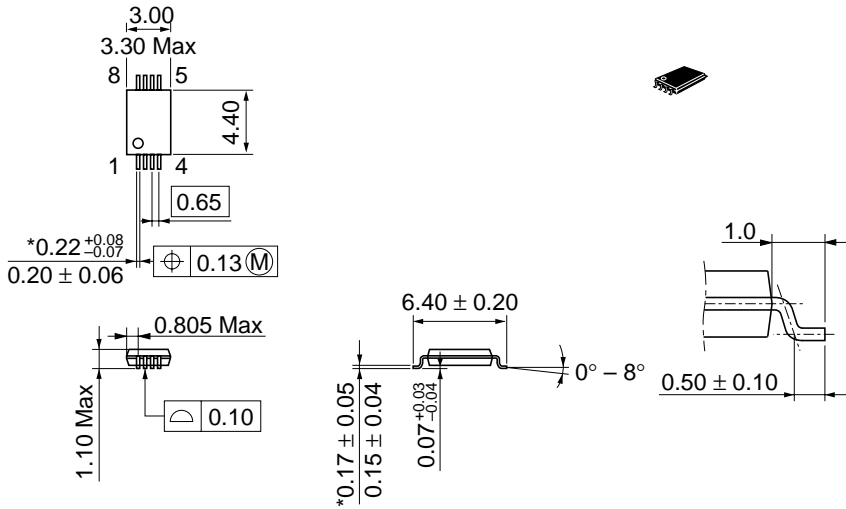
Normalized Transient Thermal Impedance vs. Pulse Width ( 2 Drive Operation)



## Package Dimensions

As of January, 2001

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-8D
JEDEC	—
EIAJ	—
Mass (reference value)	—

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# HITACHI

## Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	: <a href="http://semiconductor.hitachi.com/">http://semiconductor.hitachi.com/</a>
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### For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive,  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1> (408) 433-0223

Hitachi Europe GmbH  
Electronic Components Group  
Dornacher Straße 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Group.  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 585160

Hitachi Asia Ltd.  
Hitachi Tower  
16 Collyer Quay #20-00,  
Singapore 049318  
Tel : <65>-538-6533/538-8577  
Fax : <65>-538-6933/538-3877  
URL : <http://www.hitachi.com.sg>

Hitachi Asia Ltd.  
(Taipei Branch Office)  
4/F, No. 167, Tun Hwa North Road,  
Hung-Kuo Building,  
Taipei (105), Taiwan  
Tel : <886>-(2)-2718-3666  
Fax : <886>-(2)-2718-8180  
Telex : 23222 HAS-TP  
URL : <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower,  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon,  
Hong Kong  
Tel : <852>-(2)-735-9218  
Fax : <852>-(2)-730-0281  
URL : <http://www.hitachi.com.hk>