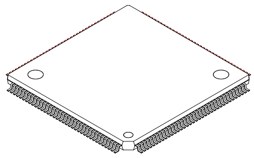
SONY

CXD2586R/-1

CD Digital Signal Processor with Built-in Digital Servo and DAC

144 pin LQFP (Plastic)



Description
The CXD2586R/-1 is a digital signal processor LSI for CD players. This LSI incorporates the digital servo, digital filter and 1-bit DAC.

Features
- All digital signal processing during playback is performed with a single chip
- Highly integrated mounting possible due to a built-in RAM

Digital Signal Processor Block
- Playback mode which supports CAV (Constant Angular Velocity)
  - Frame jitter free
  - Half-speed to octuple-speed continuous playback possible with a low external clock (only CXD2586R-1 supports up to octuple speed)
  - Allows relative rotational velocity readout
- Wide capture range playback mode
  - Spindle rotational velocity following method
  - Supports normal-speed, double-speed, quadruple-speed, sextuple-speed and octuple-speed playback (only CXD2586R-1)
- Wide frame jitter margin (±28 frames) due to a built-in 32K RAM
- The bit clock, which strobes the EFM signal, is generated by the digital PLL
- EFM data demodulation
- Enhanced EFM frame sync signal protection
- Refined super strategy-based powerful error correction C1: double correction, C2: quadruple correction
- Octuple-speed (only CXD2586R-1), sextuple-speed, quadruple-speed and double-speed playback (digital signal processor and digital servo blocks)
- Noise reduction during track jumps
- Auto zero-cross mute
- Subcode demodulation and Sub Q data error detection
- Digital spindle servo (with oversampling filter)
- 16-bit traverse counter
- Asymmetry compensation circuit
- CPU interface on serial bus
- Error correction monitor signal, etc. output from a new CPU interface
- Servo auto sequencer
- Fine search performs track jumps with high accuracy
- Digital audio interface outputs
- Digital level meter, peak meter
- Bilingual compatible

Digital Servo Block
- Microcomputer software-based flexible servo control
- Servo error signal, offset cancel function
- Servo loop, auto gain control function
- E:F balance, focus bias adjustment function

Digital Filters (DAC and LPF blocks)
- Low-pass filter for DAC
- Digital de-emphasis
- Digital attenuation
- 4fs oversampling filter
- Adopts secondary $\Delta\Sigma$ noise shaper
- LPF for DAC analog output

Structure
Silicon gate CMOS IC

Absolute Maximum Ratings
- Supply voltage V_{DD} –0.3 to +7.0 V
- Input voltage V_I –0.3 to +7.0 V (V_{SS} – 0.3V to V_{DD} +0.3V)
- Output voltage V_O –0.3 to +7.0 V
- Storage temperature Tstg –40 to +125 °C
- Supply voltage difference V_{SS} – AV_{SS} –0.3 to +0.3 V; V_{DD} – AV_{DD} –0.3 to +0.3 V

Recommended Operating Conditions
- Supply voltage
- Operating temperature

* The V_{DD} (min.) for the CXD2586R/-1 varies according to the playback speed and built-in VCO selection. The V_{DD} (min.) is 4.5V when high-speed VCO and quadruple-speed playback are selected (variable pitch off). The V_{DD} (min.) for the CXD2586R/-1 under various conditions are as shown in the following table.

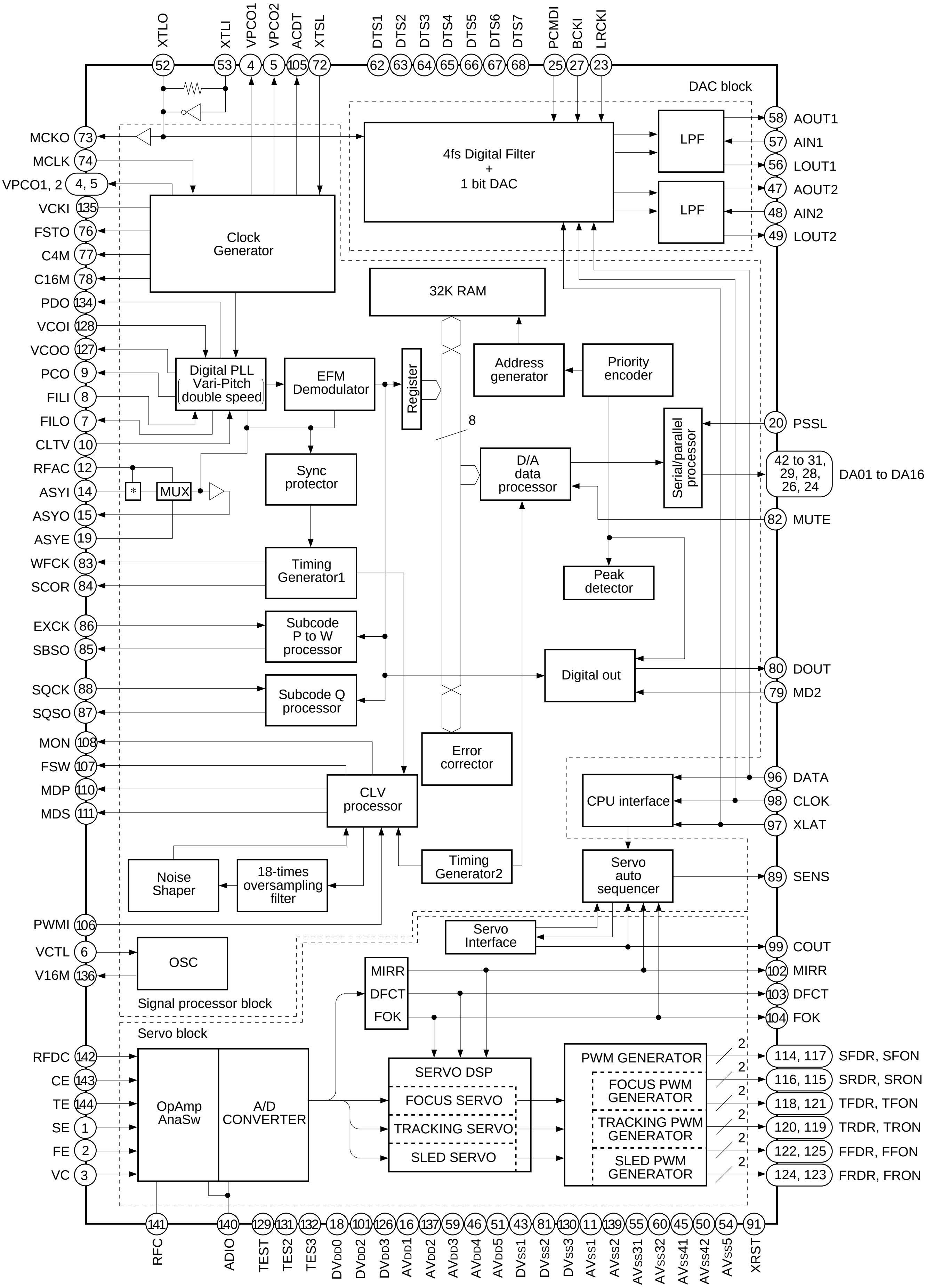
Playback speed	V_{DD} (min.) [V]		
	VCO1 high speed	VCO1 normal speed	DAC block
×8 (only CXD2586R-1)	4.75	—	—
×6	4.50	—	—
×4	4.50	—	—
×2 *1	4.00	—	—
×2	3.40	4.00	—
×1 *2	3.40	3.40	—
×1	3.40	3.40	4.50

—: Dashes indicate that there is no assurance of the processor operating. All values are for variable pitch off.

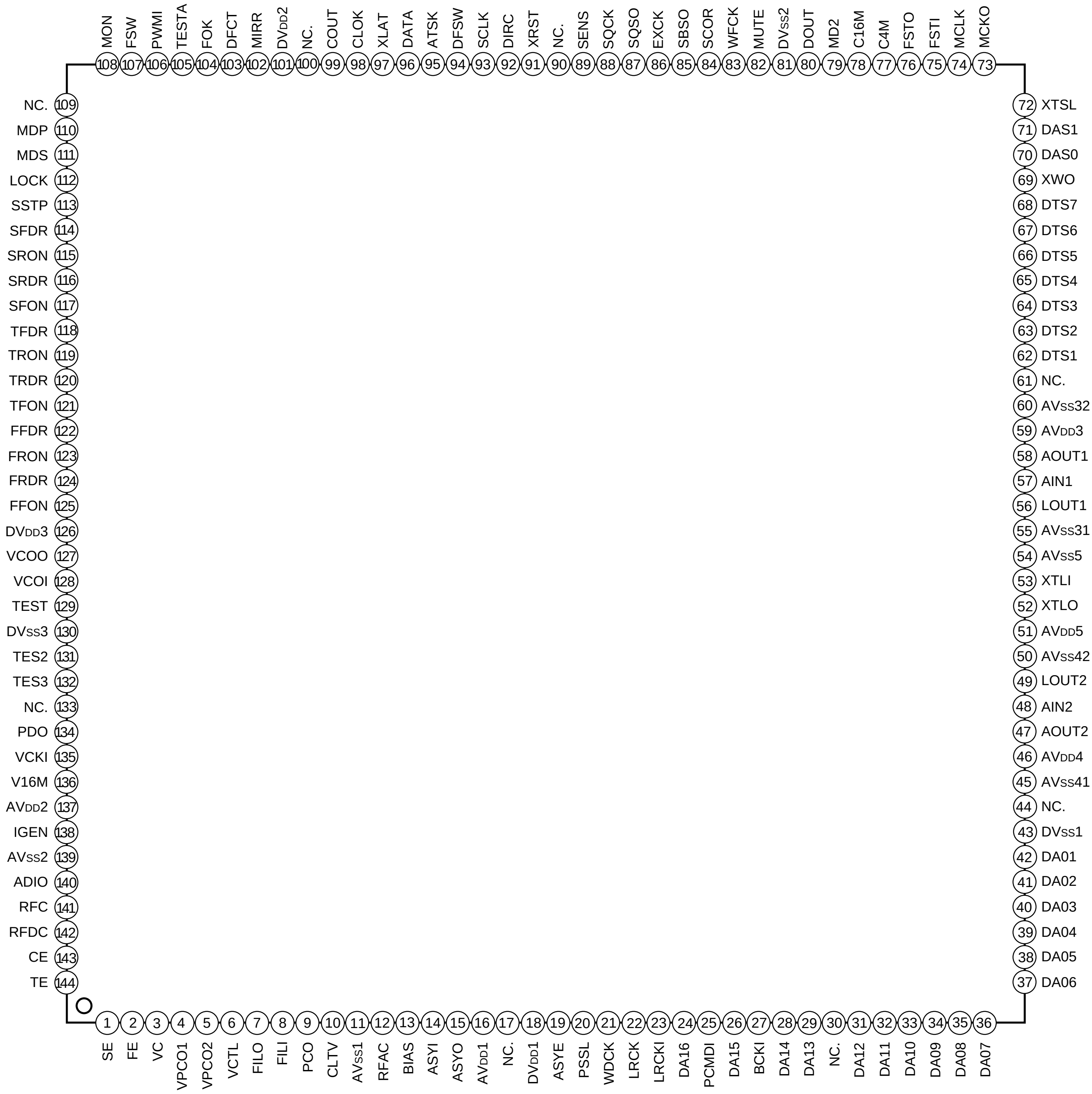
*1 When the internal operation of the LSI is set to normal-speed playback and the operating clock of the signal processor is doubled, double-speed playback results.

*2 When the internal operation of the LSI is set to double-speed mode and the crystal oscillating frequency is halved in low power consumption mode, normal-speed playback results.

Block Diagram



Pin Configuration



Pin Description

Pin No.	Symbol	I/O		Description
1	SE	I		Sled error signal input.
2	FE	I		Focus error signal input.
3	VC	I		Center voltage input.
4	VPCO1	O	1, Z, 0	Wide-band EFM PLL VCO2 charge pump output.
5	VPCO2	O	1, Z, 0	Wide-band EFM PLL VCO2 charge pump output.
6	VCTL	I		Wide-band EFM PLL VCO2 control voltage input.
7	FILO	O	Analog	Master PLL filter output (slave = digital PLL).
8	FILI	I		Master PLL filter input.
9	PCO	O	1, Z, 0	Master PLL charge pump output.
10	CLTV	I		Master VCO control voltage input.
11	$AV_{SS}1$			Analog GND.
12	RFAC	I		EFM signal input.
13	BIAS	I		Asymmetry circuit constant current input.
14	ASYI	I		Asymmetry comparator voltage input.
15	ASYO	O	1, 0	EFM full-swing output (low = V_{SS}, high = V_{DD}).
16	$AV_{DD}1$			Analog power supply.
18	$DV_{DD}1$			Digital power supply.
19	ASYE	I		Asymmetry circuit on/off (low = off, high = on).
20	PSSL	I		Audio data output mode switching input (low = serial, high = parallel).
21	WDCK	O	1, 0	D/A interface for 48-bit slot. Word clock f = 2Fs.
22	LRCK	O	1, 0	D/A interface for 48-bit slot. LR clock f = Fs.
23	LRCKI	I		LR clock input to DAC (48-bit slot).
24	DA16	O	1, 0	DA16 (MSB) output when PSSL = 1, 48-bit slot serial data output (two's complement, MSB first) when PSSL = 0.
25	PCMDI	I		Audio data input to DAC (48-bit slot).
26	DA15	O	1, 0	DA15 output when PSSL = 1, 48-bit slot bit clock output when PSSL = 0.
27	BCKI	I		Bit clock input to DAC (48-bit slot).
28	DA14	O	1, 0	DA14 output when PSSL = 1, 64-bit slot serial data output (two's complement, LSB first) when PSSL = 0.
29	DA13	O	1, 0	DA13 output when PSSL = 1, 64-bit slot bit clock output when PSSL = 0.
31	DA12	O	1, 0	DA12 output when PSSL = 1, 64-bit slot LR clock output when PSSL = 0.
32	DA11	O	1, 0	DA11 output when PSSL = 1, GTOP output when PSSL = 0.
33	DA10	O	1, 0	DA10 output when PSSL = 1, XUGF output when PSSL = 0.
34	DA09	O	1, 0	DA09 output when PSSL = 1, XPLCK output when PSSL = 0.
35	DA08	O	1, 0	DA08 output when PSSL = 1, GFS output when PSSL = 0.
36	DA07	O	1, 0	DA07 output when PSSL = 1, RFCK output when PSSL = 0.

Pin No.	Symbol	I/O		Description
37	DA06	O	1, 0	DA06 output when PSSL = 1, C2PO output when PSSL = 0.
38	DA05	O	1, 0	DA05 output when PSSL = 1, XRAOF output when PSSL = 0.
39	DA04	O	1, 0	DA04 output when PSSL = 1, MNT3 output when PSSL = 0.
40	DA03	O	1, 0	DA03 output when PSSL = 1, MNT2 output when PSSL = 0.
41	DA02	O	1, 0	DA02 output when PSSL = 1, MNT1 output when PSSL = 0.
42	DA01	O	1, 0	DA01 output when PSSL = 1, MNT0 output when PSSL = 0.
43	DVss1			Digital GND.
45	AVss41			Analog GND.
46	AVdd4			Analog power supply.
47	AOUT2	O	Analog	Channel 2 analog output.
48	AIN2	I		Channel 2 analog input.
49	LOUT2	O	Analog	Channel 2 LINE output.
50	AVss42			Analog GND.
51	AVdd5			Master clock power supply.
52	XTLO	O	1, 0	Master clock 33.8688MHz crystal oscillation circuit output.
53	XTLI	I		Master clock 33.8688MHz crystal oscillation circuit output.
54	AVss5			Master clock GND.
55	AVss31			Analog GND.
56	LOUT1	O	Analog	Channel 1 LINE output pin.
57	AIN1	I		Channel 1 analog input pin.
58	AOUT1	O	Analog	Channel 1 analog output pin.
59	AVdd3			Analog power supply.
60	AVss32			Analog GND.
62	DTS1	I		DAC test pin. Normally fixed to high.
63	DTS2	I		DAC test pin. Normally fixed to high.
64	DTS3			DAC test pin. Leave this open.
65	DTS4			DAC test pin. Leave this open
66	DTS5			DAC test pin. Leave this open.
67	DTS6			DAC test pin. Leave this open.
68	DTS7	I		DAC test pin. Normally fixed to low.
69	XWO	I		DAC sync window open input. Normally high, window open when low.
70	DAS0	I		DAC test pin. Normally fixed to low.
71	DAS1	I		DAC test pin. Normally fixed to low.
72	XTSL	I		Crystal selection input.
73	MCKO	O	1, 0	DSP clock output.
74	MCLK	I		DSP clock input.
75	FSTI	I		2/3 frequency division input for MCLK pin.

Pin No.	Symbol	I/O		Description
76	FSTO	O	1, 0	2/3 frequency division output for MCLK pin. Does not change with variable pitch.
77	C4M	O	1, 0	1/4 frequency division output for MCLK pin. Changes with variable pitch.
78	C16M	O	1, 0	16.9344MHz output. Changes simultaneously with variable pitch.
79	MD2	I		Digital Out on/off control. (low: off, high: on)
80	DOUT	O	1, 0	Digital Out output pin.
81	$DV_{SS}2$			Digital GND.
82	MUTE	I		Mute (low: off, high: on)
83	WFCK	O	1, 0	WFCK (Write Flame Clock) output.
84	SCOR	O	1, 0	Outputs a high signal when either subcode sync S0 or S1 is detected.
85	SBSO	O	1, 0	Sub P to W serial output.
86	EXCK	I		SBSO readout clock input.
87	SQSO	O	1, 0	Sub Q 80-bit and PCM peak and level data 16-bit output.
88	SQCK	I		SQSO readout clock input.
89	SENS	O	1, 0	SENS output to CPU.
91	XRST	I		System reset. Reset when low.
92	DIRC	I		Used during 1-track jumps.
93	SCLK	I		SENS serial data readout clock input.
94	DFSW	I		DFCT switching pin. High: DFCT countermeasure circuit off.
95	ATSK	I		Anti-shock pin.
96	DATA	I		Serial data input from CPU.
97	XLAT	I		Latch input from CPU. Serial data is latched at the falling edge.
98	CLOK	I		Serial data transfer clock input from CPU.
99	COUT	O	1, 0	Track count signal output.
101	$DV_{DD}2$			Digital power supply.
102	MIRR	O	1, 0	Mirror signal output.
103	DFCT	O	1, 0	Defect signal output.
104	FOK	O	1, 0	Focus OK signal output.
105	TESTA			Test pin. Not connected.
106	PWMI	I		Spindle motor external pin input.
107	FSW	O	Z, 0	Spindle motor output filter switching output.
108	MON	O	1, 0	Spindle motor on/off control output.
110	MDP	O	1, 0	Spindle motor servo control output.
111	MDS	O	1, 0	Spindle motor servo control output.
112	LOCK	O	1, 0	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low.
113	SSTP	I		Disc innermost track detection signal input.
114	SFDR	O	1, 0	Sled drive output.
115	SRON	O	1, 0	Sled drive output.

Pin No.	Symbol	I/O		Description
116	SRDR	O	1, 0	Sled drive output.
117	SFON	O	1, 0	Sled drive output.
118	TFDR	O	1, 0	Tracking drive output.
119	TRON	O	1, 0	Tracking drive output.
120	TRDR	O	1, 0	Tracking drive output.
121	TFON	O	1, 0	Tracking drive output.
122	FFDR	O	1, 0	Focus drive output.
123	FRON	O	1, 0	Focus drive output.
124	FRDR	O	1, 0	Focus drive output.
125	FFON	O	1, 0	Focus drive output.
126	$DV_{DD}3$			Digital power supply.
127	VCOO	O	1, 0	Analog EFM PLL oscillation circuit output.
128	VCOI	I		Analog EFM PLL oscillation circuit input. flock = 8.6436MHz.
129	TEST	I		Test pin. Normally fixed to low.
130	$DV_{SS}3$			Digital GND.
131	TES2	I		Test pin. Normally fixed to low.
132	TES3	I		Test pin. Normally fixed to low.
134	PDO	O	1, Z, 0	Analog EFM PLL charge pump output.
135	VCKI	I		Variable pitch clock input from the external VCO. fcenter = 16.9344MHz.
136	V16M	O	1, 0	Wide-band EFM PLL VCO2 oscillation output.
137	$AV_{DD}2$			Analog power supply.
138	IGEN	I		Operational amplifier current source reference resistance connection.
139	$AV_{SS}2$			Analog GND.
140	ADIO	O		Operational amplifier output.
141	RFC	I		RF signal LPF time constant capacitor connection.
142	RFDC	I		RF signal input.
143	CE	I		Center servo analog input.
144	TE	I		Tracking error signal input.

* In the 144-pin LQFP, the following pins are NC:
Pins 17, 30, 44, 61, 90, 100, 109, and 133

Notes)
- The 64-bit slot is an LSB first, two's complement output. The 48-bit slot is an MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window released.)
- XUGF is the negative pulse for the frame sync obtained from the EFM signal. It is the signal before sync protection.
- XPLCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- The GFS signal goes high when the frame sync and the insertion protection timing match.
- RFCK is derived from the crystal accuracy, and has a cycle of 136µs.
- C2PO represents the data error status.
- XRAOF is generated when the 32K RAM exceeds the ±28F jitter margin.

Electrical Characteristics

1. DC Characteristics (V_{DD} = AV_{DD} = 5.0V ± 10%, Vss = AVss = 0V, Topr = –20 to +75°C)

Item			Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Input voltage (1)	High level input voltage	V_{IH} (1)		0.7V_{DD}			V	*1
	Low level input voltage	V_{IL} (1)				0.3V_{DD}	V	
Input voltage (2)	High level input voltage	V_{IH} (2)	Schmitt input	0.8V_{DD}			V	*2
	Low level input voltage	V_{IL} (2)				0.2V_{DD}	V	
Input voltage (3)	Input voltage	V_{IN} (3)	Analog input	Vss		V_{DD}	V	*3, 11, 12
Output voltage (1)	High level output voltage	V_{OH} (1)	I_{OH} = –4mA	V_{DD} – 0.8		V_{DD}	V	*4
	Low level output voltage	V_{OL} (1)	I_{OL} = 4mA	0		0.4	V	
Output voltage (2)	High level output voltage	V_{OH} (2)	I_{OH} = –2mA	V_{DD} – 0.8		V_{DD}	V	*5
	Low level output voltage	V_{OL} (2)	I_{OL} = 4mA	0		0.4	V	
Output voltage (1)	Low level output voltage	V_{OL} (3)	I_{OL} = 4mA	0		0.4	V	*6
Output voltage (4)	High level output voltage	V_{OH} (4)	I_{OH} = –0.28mA	V_{DD} – 0.5		V_{DD}	V	*7
	Low level output voltage	V_{OL} (4)	I_{OL} = 0.36mA	0		0.4	V	
Output voltage (5)	High level output voltage	V_{OH} (5)	I_{OH} = –2mA	V_{DD} – 0.5		V_{DD}	V	*13
	Low level output voltage	V_{OL} (5)	I_{OL} = 8mA	0		0.4	V	
Input leak current (1)		I_{LI} (1)	V_I = 0 to 5.5V	–10		10	µA	*1, 2, 3, 12
Input leak current (2)		I_{LI} (2)	V_I = 1.5 to 3.5V	–20		20	µA	*8
Input leak current (3)		I_{LI} (3)	V_I = 0 to 5.0V	–40		600	µA	*9
Tri-state pin output leak current		I_{LO}	V_O = 0 to 5.5V	–5		5	µA	*10

Applicable pins

*1 XTSL, DATA, XLAT, MD2, PSSL, TEST, TES2, TES3, DFSW, DIRC, SSTP, ATSK, BCKI, LRCKI, PCMDI, DTS1, DTS2, DTS7, DAS0, DAS1, XWO, PWMI

*2 CLOK, XRST, EXCK, SQCK, MUTE, VCKI, ASYE, FSTI, SCLK, MCLK

*3 CLTV, FILI, RFAC, ASYI, RFDC, TE, SE, FE, VC, VCTL

*4 MDP, PDO, PCO, VPCO1, VPCO2

*5 ASYO, DOUT, FSTO, C4M, C16M, SBSO, SQSO, SCOR, MON, LOCK, WDCK, SENS, MDS, DA01 to DA16, LRCK, WFCK, FOK, COUT, MIRR, DFCT, FFON, FRDR, FRON, FFDR, TFON, TRDR, TRON, TFDR, SFON, SRDR, SRON, SFDR, MCKO, V16M

*6 FSW

*7 FILO

*8 TE, SE, FE, VC

*9 RFDC

*10 SENS, MDS, MDP, FSW, PDO, PCO, VPCO1, VPCO2

*11 RFC

*12 AIN1, AIN2

*13 AOUT1, AOUT2, LOUT1, LOUT2

2. AC Characteristics

(1) XTLI pin, VCOI pin

(a) When using self-excited oscillation

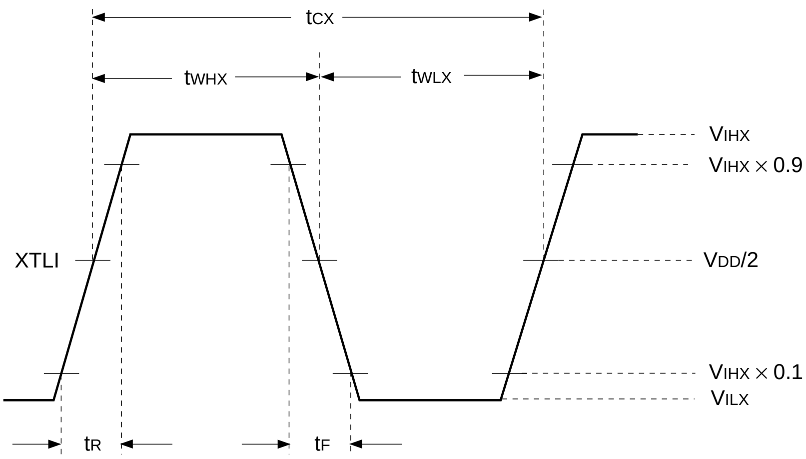
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ±10%)

Item	Symbol	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{MAX}	7		34	MHz

(b) When inputting pulses to XTLI and VCOI pins

(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ±10%)

Item	Symbol	Min.	Typ.	Max.	Unit
High level pulse width	t_{WHX}	13		500	ns
Low level pulse width	t_{WLX}	13		500	ns
Pulse cycle	t_{CX}	26		1000	ns
Input high level	V_{IHX}	V_{DD} – 1.0			V
Input low level	V_{ILX}			0.8	V
Rise time, fall time	t_R, t_F			10	ns



(c) When inputting sine waves to XTLI and VCOI pins via a capacitor

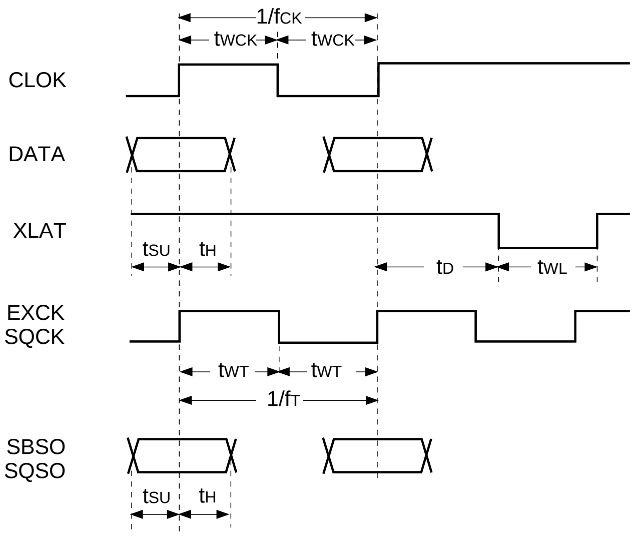
(Topr = –20 to +75°C, V_{DD} = AV_{DD} = 5.0V ±10%)

Item	Symbol	Min.	Typ.	Max.	Unit
Input amplitude	V_I	2.0		V_{DD} + 0.3	Vp-p

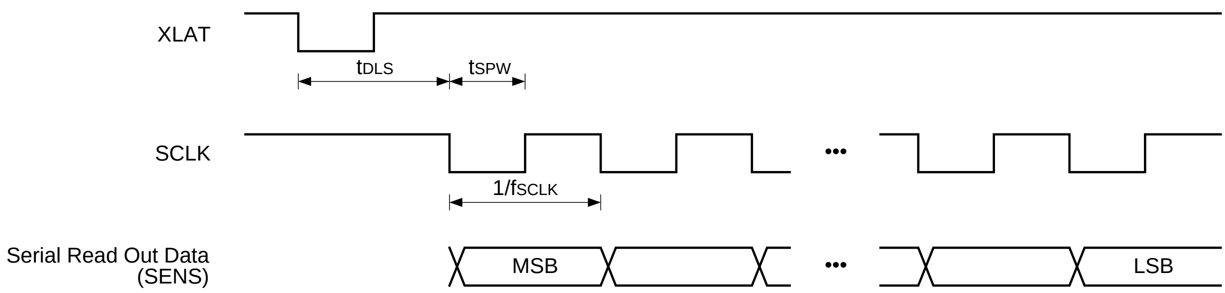
(2) CLOK, DATA, XLAT, SQCK, and EXCK pins

(V_{DD} = AV_{DD} = 5.0V ±10%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CK}			0.65	MHz
Clock pulse width	t_{WCK}	750			ns
Setup time	t_{SU}	300			ns
Hold time	t_H	300			ns
Delay time	t_D	300			ns
Latch pulse width	t_{WL}	750			ns
EXCK SQCK frequency	f_T			0.65	MHz
EXCK SQCK pulse width	t_{WT}	750			ns



(3) SCLK pin



Item	Symbol	Min.	Typ.	Max.	Unit
SCLK frequency	f_{SCLK}			1	MHz
SCLK pulse width	t_{SPW}	500			ns
Delay time	t_{DLS}	15			µs

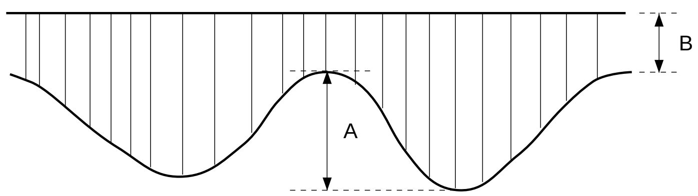
(4) COUT, MIRR and DFCT pins

Operating frequency ($V_{DD} = AV_{DD} = 5.0V \pm 10\%$, $V_{SS} = AV_{SS} = 0V$, Topr = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
COUT maximum operating frequency	f_{COUT}	40			kHz	*1
MIRR maximum operating frequency	f_{MIRR}	40			kHz	*2
DFCT maximum operating frequency	f_{DFCTH}	5			kHz	*3

*1 When using a high-speed traverse TZC.

*2



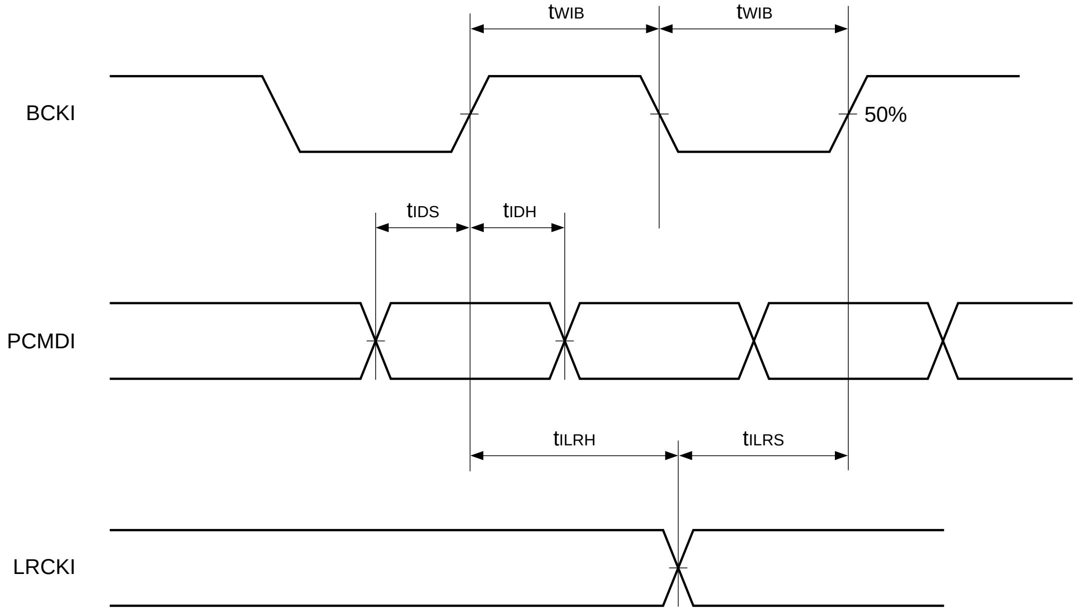
When the RF signal continuously satisfies the following conditions during the above traverse.

- A = 0.6 to A1.3V
- $\frac{B}{A + B}$ = less than 25%

*3 During complete RF signal omission.
When settings related to DFCT signal generation are Typ.

(5) BCKI, LRCKI and PCMDI pins (V_{DD} = 5.0V ±10%, Topr = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Input BCKI frequency	t_{BCK}			4.5	MHz
Input BCKI pulse width	t_{WIB}	100			ns
Input data setup time	t_{IDS}	10			
Input data hold time	t_{IDH}	15			
Input LRCK setup time	t_{ILRH}	10			
Input LRCK hold time	t_{ILRS}	15			



(6) AOUT1, AOUT2, LOUT1 and LOUT2 pins
(V_{DD} = AV_{DD} =5.0V ±5%, V_{SS} = AV_{SS} = 0V, Topr = –20 to +75°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Applicable pins
Output voltage (1)	V_{OUT} (1)	$0.1V_{DD}$*		$0.9V_{DD}$*	V	*1
Output voltage (2)	V_{OUT} (2)	V_{SS}		V_{DD}	V	*2
Load resistance	R_L	10			kΩ	*1, *2

* When a sine wave of 1kHz and 0dB is output.

Applicable pins

*1 AOUT1, AOUT2

*2 LOUT1, LOUT2

DAC Analog Characteristics

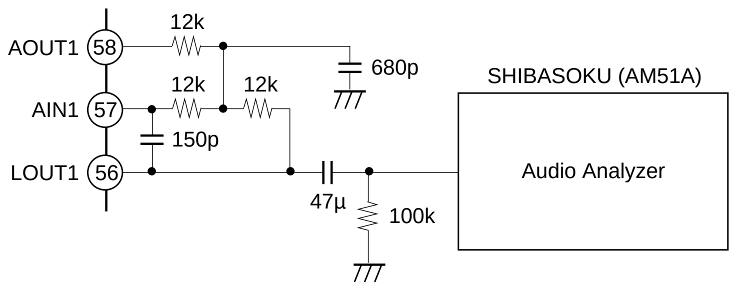
Measurement conditions

(Ta = 25°C, V_{DD} = 5.0V, F_S = 44.1kHz, signal frequency = 1kHz, measurement band = 4Hz to 20kHz, master clock = 768fs)

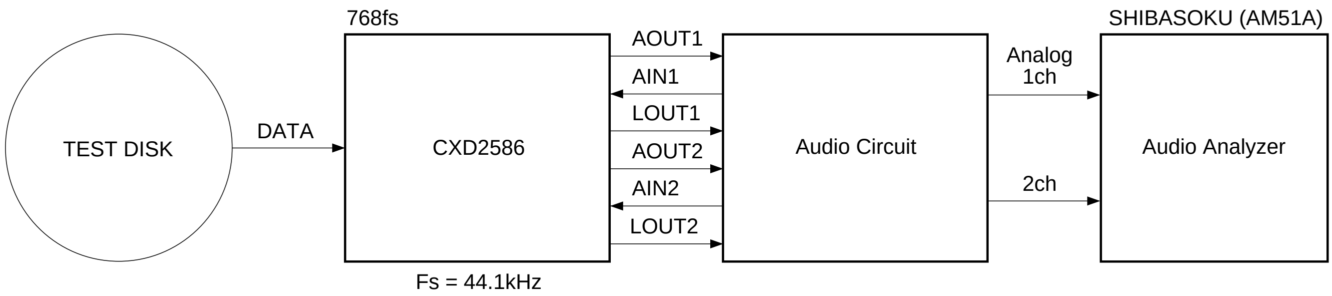
Item	Typ.	Unit	Remarks
S/N ratio	93	dB	(EIAJ) *1
THD + N	0.01	%	(EIAJ)
Dynamic range	91	dB	(EIAJ) *1, *2
Channel separation	91	dB	(EIAJ)
Output level	1.31	V (rms)	
Difference in gain between channels	0.1	dB	

*1 Using "A" weighting filter
*2 –60dB, 1kHz input

The analog characteristics measurement circuit is shown below.



LPF external circuit diagram



Block diagram of analog characteristics measurement

Contents

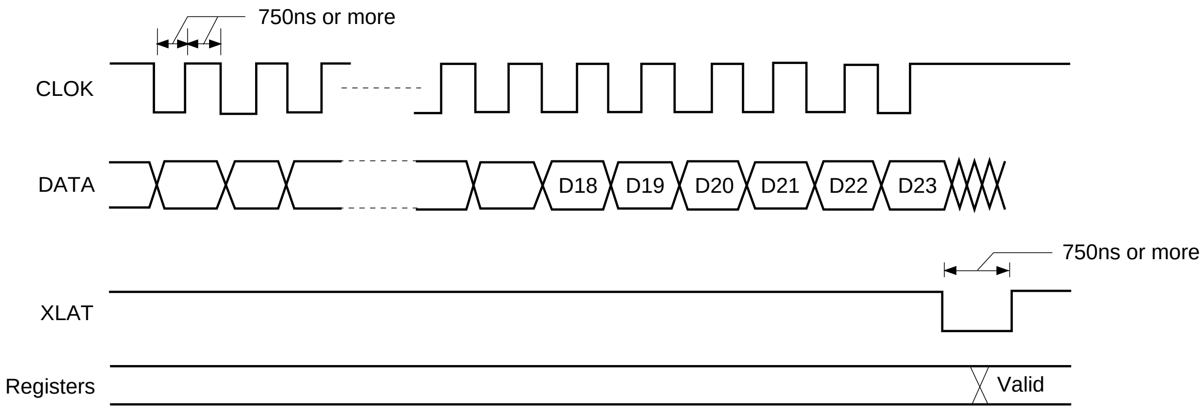
Explanation of abbreviations

AVRG:	Average
AGCNTL:	Automatic gain control
FCS:	Focus
TRK:	Tracking
SLD:	Sled
DFCT:	Defect

[1] CPU Interface

§1-1. CPU Interface Timing

• CPU interface
  This interface uses DATA, CLOK, and XLAT to set the modes.
  The interface timing chart is shown below.



• The internal registers are initialized by a reset when XRST = 0.

§1-2. CPU Interface Command Table

Total bit length for each register

Register	Total bit length
0 to 2	8bit
3	8 to 24bit
4 to 6	16bit
7	20bit
8	24bit
9	20bit
A	28bit
B	20bit
C to D	16bit
E	20bit

Command Table ($0X to 1X)

Register	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	FOCUS CONTROL	0 0 0 0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO ON (FOCUS GAIN NORMAL)
			1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO ON (FOCUS GAIN DOWN)
			—	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, 0V OUT
			—	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT
			—	—	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SEARCH VOLTAGE DOWN
			—	—	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SEACH VOLTAGE UP
1	TRACKING CONTROL	0 0 0 1	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANTI SHOCK ON
			0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ANTI SHOCK OFF
			—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BRAKE ON
			—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BRAKE OFF
			—	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN NORMAL
			—	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP
			—	—	—	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 1
			—	—	—	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 2

—: Don't care

Command Table ($2X to 3X)

Register	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
2	TRACKING MODE	0 0 1 0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO OFF
			0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO ON
			1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FORWARD TRACK JUMP
			1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REVERSE TRACK JUMP
			—	—	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED SERVO OFF
			—	—	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED SERVO ON
			—	—	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FORWARD SLED MOVE
			—	—	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REVERSE SLED MOVE

Register	Command	Address			Data 1		Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±1 × basic value) (Default)
			0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±2 × basic value)
			0	0	1	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±3 × basic value)
			0	0	1	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±4 × basic value)

—: Don't care

Command Table ($340X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	0 0 0 0	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K00) SLED INPUT GAIN
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K01) SLED LOW BOOST FILTER A-H
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K02) SLED LOW BOOST FILTER A-L
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K03) SLED LOW BOOST FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K04) SLED LOW BOOST FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K05) SLED OUTPUT GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K06) FOCUS INPUT GAIN
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K07) SLED AUTO GAIN
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K08) FOCUS HIGH CUT FILTER A
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K09) FOCUS HIGH CUT FILTER B
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0A) FOCUS LOW BOOST FILTER A-H
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0B) FOCUS LOW BOOST FILTER A-L
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0C) FOCUS LOW BOOST FILTER B-H
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0D) FOCUS LOW BOOST FILTER B-L
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0E) FOCUS PHASE COMPENSATE FILTER A
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K0F) FOCUS DEFECT HOLD GAIN

Command Table ($341X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	0 0 0 1	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K10) FOCUS PHASE COMPENSATE FILTER B
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K11) FOCUS OUTPUT GAIN
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K12) ANTI SHOCK INPUT GAIN
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K13) FOCUS AUTO GAIN
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K14) HPTZC / AUTO GAIN HIGH PASS FILTER A
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K15) HPTZC / AUTO GAIN HIGH PASS FILTER B
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K16) ANTI SHOCK HIGH PASS FILTER A
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K17) HPTZC / AUTO GAIN LOW PASS FILTER B
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K18) FIX
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K19) TRACKING INPUT GAIN
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1A) TRACKING HIGH CUT FILTER A
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1B) TRACKING HIGH CUT FILTER B
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1C) TRACKING LOW BOOST FILTER A-H
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1D) TRACKING LOW BOOST FILTER A-L
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1E) TRACKING LOW BOOST FILTER B-H
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K1F) TRACKING LOW BOOST FILTER B-L

Command Table ($342X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	0 0 1 0	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K20) TRACKING PHASE COMPENSATE FILTER A
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K21) TRACKING PHASE COMPENSATE FILTER B
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K22) TRACKING OUTPUT GAIN
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K23) TRACKING AUTO GAIN
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K24) FOCUS GAIN DOWN HIGH CUT FILTER A
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K25) FOCUS GAIN DOWN HIGH CUT FILTER B
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K26) FOCUS GAIN DOWN LOW BOOST FILTER A-H
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K27) FOCUS GAIN DOWN LOW BOOST FILTER A-L
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K28) FOCUS GAIN DOWN LOW BOOST FILTER B-H
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K29) FOCUS GAIN DOWN LOW BOOST FILTER B-L
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2A) FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2B) FOCUS GAIN DOWN DEFECT HOLD GAIN
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2C) FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2D) FOCUS GAIN DOWN OUTPUT GAIN
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2E) NOT USED
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K2F) NOT USED

Command Table ($343X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	0 0 1 1	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K30) FIX
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K31) ANTI SHOCK LOW PASS FILTER B
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K32) NOT USED
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K33) ANTI SHOCK HIGH PASS FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K34) ANTI SHOCK HIGH PASS FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K35) ANTI SHOCK FILTER COMPARATE GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K36) TRACKING GAIN UP2 HIGH CUT FILTER A
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K37) TRACKING GAIN UP2 HIGH CUT FILTER B
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K38) TRACKING GAIN UP2 LOW BOOST FILTER A-H
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K39) TRACKING GAIN UP2 LOW BOOST FILTER A-L
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3A) TRACKING GAIN UP2 LOW BOOST FILTER B-H
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3B) TRACKING GAIN UP2 LOW BOOST FILTER B-L
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3C) TRACKING GAIN UP PHASE COMPENSATE FILTER A
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3D) TRACKING GAIN UP PHASE COMPENSATE FILTER B
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3E) TRACKING GAIN UP OUTPUT GAIN
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K3F) NOT USED

Command Table ($344X)

Register	Command	Address 1	Address 2	Address 3	Address 4				Data 1				Data 2				
		D23 to D20	D19 to D16	D15 to D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0 1 0 0	0 1 0 0	0	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K40) TRACKING HOLD FILTER INPUT GAIN
					0	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K41) TRACKING HOLD FILTER A-H
					0	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K42) TRACKING HOLD FILTER A-L
					0	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K43) TRACKING HOLD FILTER B-H
					0	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K44) TRACKING HOLD FILTER B-L
					0	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K45) TRACKING HOLD FILTER OUTPUT GAIN
					0	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K46) NOT USED
					0	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K47) NOT USED
					1	0	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K48) FOCUS HOLD FILTER INPUT GAIN
					1	0	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K49) FOCUS HOLD FILTER A-H
					1	0	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4A) FOCUS HOLD FILTER A-L
					1	0	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4B) FOCUS HOLD FILTER B-H
					1	1	0	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4C) FOCUS HOLD FILTER B-L
					1	1	0	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4D) FOCUS HOLD FILTER OUTPUT GAIN
					1	1	1	0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4E) NOT USED
					1	1	1	1	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	KRAM DATA (K4F) NOT USED

Command Table ($34FX to 3FX)

Register	Command	Address 1					Address 2						Data 1		Data 2				Data 3				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	1	0	0	1	1	1	1	1	0	FBL9	FBL8	FBL7	FBL6	FBL5	FBL4	FBL3	FBL2	FBL1	—	FOCUS BIAS LIMIT
			0	1	0	0	1	1	1	1	0	1	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	—	FOCUS BIAS DATA
			0	1	0	0	1	1	1	1	0	0	TV9	TV8	TV7	TV6	TV5	TV4	TV3	TV2	TV1	TV0	TRVSC DATA
		Address					Data 1				Data 2				Data 3				Data 4				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0 0 1 1	0	1	0	1	FT1	FT0	FS5	FS4	FS3	FS2	FS1	FS0	FTZ	FG6	FG5	FG4	FG3	FG2	FG1	FG0	FOCUS SEARCH SPEED/ VOLTAGE/AUTO GAIN
			0	1	1	0	0	DTZC	TJ5	TJ4	TJ3	TJ2	TJ1	TJ0	SFJP	TG6	TG5	TG4	TG3	TG2	TG1	TG0	DTZC/TRACK JUMP VOLTAGE/AUTO GAIN
			0	1	1	1	FZSH	FZSL	SM5	SM4	SM3	SM2	SM1	SM0	AGS	AGJ	AGGF	AGGT	AGV1	AGV2	AGHS	AGHT	FZSL/SLED MOVE/ Voltage/AUTO GAIN
			1	0	0	0	VCLM	VCLC	FLM	FLC0	RFLM	RFLC	AGF	AGT	DFSW	LKSW	TBLM	TCLM	FLC1	TLC2	TLC1	TLC0	LEVEL/AUTO GAIN/ DFSW/ (Initialize)
			1	0	0	1	DAC	SD6	SD5	SD4	SD3	SD2	SD1	SD0	0	0	0	0	0	0	0	0	SERIAL DATA READ MODE/SELECT
			1	0	1	0	0	FBON	FBSS	FBUP	FBV1	FBV0	0	TJD0	FPS1	FPS0	TPS1	TPS0	CEIT	SJHD	INBK	MTI0	FOCUS BIAS
			1	0	1	1	SFO2	SFO1	SDF2	SDF1	MAX2	MAX1	SFOX	BTF	D2V2	D2V1	D1V2	D1V1	RINT	0	0	0	Operation for MIRR/ DFCT/FOK
		Address				Data 1					Data 2				Data 3				Data 4				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0 0 1 1	1	1	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TZC for COUT SLCT HPTZC (Default)
			1	1	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TZC for COUT SLCT DTZC
		Address					Data 1				Data 2				Data 3				Data 4				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0 0 1 1	1	1	1	0	F1NM	F1DM	F3NM	F3DM	T1NM	T1UM	T3NM	T3UM	DFIS	TLCD	RFLP	0	0	0	MIRI	XT1D	Filter
			1	1	1	1	0	AGG4	XT4D	XT2D	0	DRR2	DRR1	DRR0	0	ASFG	0	LPAS	SRO1	SRO0	AGHF	COT2	Others

—: Don't care

Command Table ($4X to EX)

Register	Command	Address				Data 1				Data 2				Data 3				Data 4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	AS3	AS2	AS1	AS0	MT3	MT2	MT1	MT0	LSSL	0	0	0	—	—	—	—
5	Blind (A, E), Overflow (C, G), Brake (B)	0	1	0	1	TR3	TR2	TR1	TR0	0	0	0	0	0	0	0	0	—	—	—	—
6	Sled KICK, KICK (F), BRAKE (D)	0	1	1	0	SD3	SD2	SD1	SD0	KF3	KF2	KF1	KF0	0	0	0	0	—	—	—	—
7	Auto sequence (N) track jump count setting	0	1	1	1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
8	MODE setting	1	0	0	0	CD-ROM	DOUT Mute	DOUT Mute-F	WSEL	VCO SEL	ASHS	SOCT	VCO SEL2	KSL3	KSL2	KSL1	KSL0	0	0	1	0
9	Function specification	1	0	0	1	DCLV ON/OFF	DSPB ON/OFF	ASEQ ON/OFF	DPLL ON/OFF	BiliGL MAIN	BiliGL SUB	FLFC	0	DAC EMP	DAC ATT	0	0	PLM3	PLM2	PLM1	PLM0
A	Audio CTRL	1	0	1	0	0	0	Mute	ATT	PCT1	PCT2	DADS	SOC2	AT1D7	AT1D6	AT1D5	AT1D4	AT1D3	AT1D2	AT1D1	AT1D0
B	Traverse monitor counter setting	1	0	1	1	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1
C	Spindle servo coefficient setting	1	1	0	0	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	Gain DCLV1	Gain DCLV0	0	0	0	0	0	0	—	—	—	—
D	CLV CTRL	1	1	0	1	DCLV PWM MD	TB	TP	CLVS Gain	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	—	—	—	—
E	SPD MODE	1	1	1	0	CM3	CM2	CM1	CM0	EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON	Gain CAV1	Gain CAV0	FCSW	0

—: Don't care

Register	Command	Address	Data 1	Data 2	Data 3	Data 4	Data 5				Data 6			
							D3	D2	D1	D0	D3	D2	D1	D0
A	Audio CTRL	1 0 1 0					AT2D7	AT2D6	AT2D5	AT2D4	AT2D3	AT2D2	AT2D1	AT2D0

§1-3. CPU Command Presets

Command Preset Table ($0X to 34X)

Register	Command	Address	Data 1				Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	FOCUS CONTROL	0 0 0 0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FOCUS SERVO OFF, 0V OUT
1	TRACKING CONTROL	0 0 0 1	0	0	0	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING GAIN UP FILTER SELECT 1
2	TRACKING MODE	0 0 1 0	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRACKING SERVO OFF SLED SERVO OFF
Register	Command	Address			Data 1		Data 2				Data 3				Data 4				Data 5				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D0	D0	
3	SELECT	0 0 1 1	0	0	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SLED KICK LEVEL (±1 + basic value) (Default)
		Address 1					Address 2				Address 3				Data 1				Data 2				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D0	D0	
		0 0 1 1	0	1	0	0	0	See the coefficient preset values table.															KRAM DATA ($3400XX to $344fXX)

—: Don't care

Command Preset Table ($34FX to 3FX)

Register	Command	Address 1					Address 2						Data 1		Data 2				Data 3				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
3	SELECT	0 0 1 1	0	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	FOCUS BIAS LIMIT
			0	1	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	FOCUS BIAS DATA
			0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	TRVSC DATA
		Address					Data 1				Data 2				Data 3				Data 4				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0 0 1 1	0	1	0	1	0	1	0	1	1	0	0	0	0	0	1	0	1	1	0	1	FOCUS SEARCH SPEED/ VOLTAGE AUTO GAIN
			0	1	1	0	0	0	0	0	1	1	1	0	0	0	1	0	1	1	1	0	DTZC/TRACK JUMP VOLTAGE AUTO GAIN
			0	1	1	1	0	1	0	1	0	0	0	0	1	0	1	1	1	0	1	0	FZSL/SLED MOVE/ Voltage/AUTO GAIN
			1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LEVEL/AUTO GAIN/ DFSW/ (Initialize)
			1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SERIAL DATA READ MODE/SELECT
			1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FOCUS BIAS
			1	0	1	1	1	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	Operation for MIRR/ DFCT/FOK
		Address				Data 1					Data 2				data 3				Data 4				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0 0 1 1	1	1	0	0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TZC for COUT SLCT HPTZC (Default)
		Address					Data 1				Data 2				data 3				Data 4				
		D23 to D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		0 0 1 1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Filter
			1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Others

—: Don't care

Command Preset Table ($4X to EX)

Register	Command	Address				Data 1				Data 2				Data 3				Data 4			
		D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
4	Auto sequence	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—
5	Blind (A, E), Brake (B), Overflow (C, G)	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	—	—	—	—
6	Sled KICK, BRAKE (D), KICK (F)	0	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	—	—	—	—
7	Auto sequence (N) track jump count setting	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
8	MODE setting	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
9	Function specification	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1
A	Audio CTRL	1	0	1	0	0	0	1	1	0	0	0	0	1	1	1	1	1	1	1	1
B	Traverse monitor counter setting	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
C	Spindle servo coefficient setting	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—
D	CLV CTRL	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—	—
E	SPD MODE	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

—: Don't care

Register	Command	Address	Data 1	Data 2	Data 3	Data 4	Data 5				Data 6			
							D3	D2	D1	D0	D3	D2	D1	D0
A	Audio CTRL	1 0 1 0					1	1	1	1	1	1	1	1

<Coefficient ROM Preset Values Table (1)>

ADDRESS	DATA	CONTENTS
K00	E0	SLED INPUT GAIN
K01	81	SLED LOW BOOST FILTER A-H
K02	23	SLED LOW BOOST FILTER A-L
K03	7F	SLED LOW BOOST FILTER B-H
K04	6A	SLED LOW BOOST FILTER B-L
K05	10	SLED OUTPUT GAIN
K06	14	FOCUS INPUT GAIN
K07	30	SLED AUTO GAIN
K08	7F	FOCUS HIGH CUT FILTER A
K09	46	FOCUS HIGH CUT FILTER B
K0A	81	FOCUS LOW BOOST FILTER A-H
K0B	1C	FOCUS LOW BOOST FILTER A-L
K0C	7F	FOCUS LOW BOOST FILTER B-H
K0D	58	FOCUS LOW BOOST FILTER B-L
K0E	82	FOCUS PHASE COMPENSATE FILTER A
K0F	7F	FOCUS DEFECT HOLD GAIN
K10	4E	FOCUS PHASE COMPENSATE FILTER B
K11	32	FOCUS OUTPUT GAIN
K12	20	ANTI SHOCK INPUT GAIN
K13	30	FOCUS AUTO GAIN
K14	80	HPTZC / Auto Gain HIGH PASS FILTER A
K15	77	HPTZC / Auto Gain HIGH PASS FILTER B
K16	80	ANTI SHOCK HIGH PASS FILTER A
K17	77	HPTZC / Auto Gain LOW PASS FILTER B
K18	00	Fix*
K19	F1	TRACKING INPUT GAIN
K1A	7F	TRACKING HIGH CUT FILTER A
K1B	3B	TRACKING HIGH CUT FILTER B
K1C	81	TRACKING LOW BOOST FILTER A-H
K1D	44	TRACKING LOW BOOST FILTER A-L
K1E	7F	TRACKING LOW BOOST FILTER B-H
K1F	5E	TRACKING LOW BOOST FILTER B-L
K20	82	TRACKING PHASE COMPENSATE FILTER A
K21	44	TRACKING PHASE COMPENSATE FILTER B
K22	18	TRACKING OUTPUT GAIN
K23	30	TRACKING AUTO GAIN
K24	7F	FOCUS GAIN DOWN HIGH CUT FILTER A
K25	46	FOCUS GAIN DOWN HIGH CUT FILTER B
K26	81	FOCUS GAIN DOWN LOW BOOST FILTER A-H
K27	3A	FOCUS GAIN DOWN LOW BOOST FILTER A-L
K28	7F	FOCUS GAIN DOWN LOW BOOST FILTER B-H
K29	66	FOCUS GAIN DOWN LOW BOOST FILTER B-L
K2A	82	FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
K2B	44	FOCUS GAIN DOWN DEFECT HOLD GAIN
K2C	4E	FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
K2D	1B	FOCUS GAIN DOWN OUTPUT GAIN
K2E	00	NOT USED
K2F	00	NOT USED

<Coefficient ROM Preset Values Table (2)>

ADDRESS	DATA	CONTENTS
K30	80	Fix*
K31	66	ANTI SHOCK LOW PASS FILTER B
K32	00	NOT USED
K33	7F	ANTI SHOCK HIGH PASS FILTER B-H
K34	6E	ANTI SHOCK HIGH PASS FILTER B-L
K35	20	ANTI SHOCK FILTER COMPARATE GAIN
K36	7F	TRACKING GAIN UP2 HIGH CUT FILTER A
K37	3B	TRACKING GAIN UP2 HIGH CUT FILTER B
K38	80	TRACKING GAIN UP2 LOW BOOST FILTER A-H
K39	44	TRACKING GAIN UP2 LOW BOOST FILTER A-L
K3A	7F	TRACKING GAIN UP2 LOW BOOST FILTER B-H
K3B	77	TRACKING GAIN UP2 LOW BOOST FILTER B-L
K3C	86	TRACKING GAIN UP PHASE COMPENSATE FILTER A
K3D	0D	TRACKING GAIN UP PHASE COMPENSATE FILTER B
K3E	57	TRACKING GAIN UP OUTPUT GAIN
K3F	00	NOT USED
K40	04	TRACKING HOLD FILTER INPUT GAIN
K41	7F	TRACKING HOLD FILTER A-H
K42	7F	TRACKING HOLD FILTER A-L
K43	79	TRACKING HOLD FILTER B-H
K44	17	TRACKING HOLD FILTER B-L
K45	6D	TRACKING HOLD FILTER OUTPUT GAIN
K46	00	NOT USED
K47	00	NOT USED
K48	02	FOCUS HOLD FILTER INPUT GAIN
K49	7F	FOCUS HOLD FILTER A-H
K4A	7F	FOCUS HOLD FILTER A-L
K4B	79	FOCUS HOLD FILTER B-H
K4C	17	FOCUS HOLD FILTER B-L
K4D	54	FOCUS HOLD FILTER OUTPUT GAIN
K4E	00	NOT USED
K4F	00	NOT USED

* Fix indicates that normal preset values should be used.

§1-4. Description of SENS Signals

SENS output

Microcomputer serial register (latching not required)	ASEQ = 0	ASEQ = 1	Output data length
$0X	Z	FZC	—
$1X	Z	AS	—
$2X	Z	TZC	—
$38	Z	AGOK*	—
$38	Z	XAVEBSY*	—
$30 to 37	Z	SSTP	—
$3A	Z	FBIAS Count STOP	—
$3B to 3F	Z	SSTP	—
$3904	Z	TE Avrg Reg.	9 bit
$3908	Z	FE Avrg Reg.	9 bit
$390C	Z	VC Avrg Reg.	9 bit
$391C	Z	TRVSC Reg.	9 bit
$391D	Z	FB Reg.	9 bit
$391F	Z	RFDC Avrg Reg.	8 bit
$4X	Z	XBUSY	—
$5X	Z	FOK	—
$6X	Z	0	—
$AX	GFS	GFS	—
$BX	COMP	COMP	—
$CX	COUT	COUT	—
$EX	$\overline{\text{OV64}}$	$\overline{\text{OV64}}$	—
$7X, 8X, 9X, DX, FX	Z	0	—

* $38 outputs AGOK during AGT and AGF command settings, and XAVEBSY during AVRG measurement. SSTP is output in all other cases.

Description of SENS Signals

SENS output	
Z	The SENS pin is high impedance.
XBUSY	Low while the auto sequencer is in operation, high when operation terminates.
FOK	Outputs the same signal as the FOK pin. High for "focus OK".
GFS	High when the regenerated frame sync is obtained with the correct timing.
COMP	Counts the number of tracks set with Reg B. High when Reg B is latched, low when the initial Reg B number is input by CNIN.
COUT	Counts the number of tracks set with Reg B. High when Reg B is latched, toggles each time the Reg B number is input by CNIN. While $44 and $45 are being executed, toggles with each CNIN 8-count instead of the Reg B number.
$\overline{\text{OV64}}$	Low when the EFM signal is lengthened by 64 channel clock pulses or more after passing through the sync detection filter.

The meaning of the data for each address is explained below.

$4X commands

Register name	Data 1				Data 2				Data 3			
4	Command				MAX timer value				Timer range			
	AS3	AS2	AS1	AS0	MT3	MT2	MT1	MT0	LSSL	0	0	0

Command	AS3	AS2	AS1	AS0
Cancel	0	0	0	0
Fine Search	0	1	0	RXF
Focus-On	0	1	1	1
1 Track Jump	1	0	0	RXF
10 Track Jump	1	0	1	RXF
2N Track Jump	1	1	0	RXF
M Track Move	1	1	1	RXF

RXF = 0 Forward
RXF = 1 Reverse

- When the Focus-on command ($47) is canceled, $02 is sent and the auto sequence is interrupted.
- When the Track jump commands ($44 to $45, $48 to $4D) are canceled, $25 is sent and the auto sequence is interrupted.

MAX timer value				Timer range			
MT3	MT2	MT1	MT0	LSSL	0	0	0
23.2ms	11.6ms	5.8ms	2.9ms	0	0	0	0
1.49s	0.74s	0.37s	0.18s	1	0	0	0

- To disable the MAX timer, set the MAX timer value to 0.

$5X commands

Timer	TR3	TR2	TR1	TR0
Blind (A, E), Overflow (C, G)	0.18ms	0.09ms	0.045ms	0.022ms
Brake (B)	0.36ms	0.18ms	0.09ms	0.045ms

$6X commands

Register name	Data 1				Data 2			
6	KICK (D)				KICK (F)			
	SD3	SD2	SD1	SD0	KF3	KF2	KF1	KF0

Timer	SD3	SD2	SD1	SD0
When executing KICK (D) $44 or $45	23.2ms	11.6ms	5.8ms	2.9ms
When executing KICK (D) $4C or $4D	11.6ms	5.8ms	2.9ms	1.45ms

Timer	KF3	KF2	KF1	KF0
KICK (F)	0.72ms	0.36ms	0.18ms	0.09ms

$7X commands

Auto sequence track jump count setting

Command	Data 1				Data 2				Data 3				Data 4			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Auto sequence track jump count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

This command is to set N when a 2N track jump is executed, to set M when an M track move is executed and to set the jump count when fine search is executed for auto sequence.

- The maximum track count is 65,535, but note that with a 2N-track jump the maximum track jump count depends on the mechanical limitations of the optical system.
- When the track jump count is from 0 to 15, the COUT signal is used to count tracks for 2N-track jump/M track move; when the count is 16 or over, the MIRR signal is used. For fine search, the COUT signal is used to count tracks.

$8X commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Mode specification	CD-ROM	DOUT Mute	DOUT Mute-F	WSEL	VCO SEL1	ASHS	SOCT	VCO SEL2	KSL3	KSL2	KSL1	KSL0

Command bit	C2PO timing	Processing
CDROM = 1	See the Timing Chart 1-3	CDROM mode; average value interpolation and pre-value hold are not performed.
CDROM = 0	See the Timing Chart 1-3	Audio mode; average value interpolation and pre-value hold are performed.

Command bit	Processing
DOUT Mute = 1	When Digital Out is on (MD2 pin = 1), DOUT output is muted.
DOUT Mute = 0	When Digital Out is on, DOUT output is not muted.

Command bit	Processing
D. out Mute F = 1	When Digital Out is on (MD2 pin = 1), DA output is muted.
D. out Mute F = 0	DA output mute is not affected when Digital Out is either on or off.

<table>
<tr><th>MD2</th><th>Other mute conditions*</th><th>DOUT Mute</th><th>D.out Mute F</th><th>DOUT output</th><th>DA output</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="8">OFF</td><td rowspan="4">0dB</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="4">–∞dB</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="2">0dB</td><td>0dB</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>–∞dB</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td rowspan="6">–∞dB</td><td>0dB</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="5">–∞dB</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>

* See mute conditions (1), (2), and (4) to (6) under $AX commands for other mute conditions.

Command bit	Sync protection window width	Application
WSEL = 1	±26 channel clock*	Anti-rolling is enhanced.
WSEL = 0	±6 channel clock	Sync window protection is enhanced.

* In normal-speed playback, channel clock = 4.3218MHz.

Command bit	Function
ASHS = 0	The command transfer rate to SSP is set to normal speed.
ASHS = 1	The command transfer rate to SSP is set to half speed.

* See "§4-8. Playback Speed" for settings.

Command bit	Function
SOCT = 0	Sub Q is output from the SQSO pin.
SOCT = 1	Each output signal is output from the SQSO pin. Input the readout clock to SQCK. (See the Timing Chart 2-4.)

Command bit			Processing
VCOSEL1	KSL3	KSL2	
0	0	0	Multiplier PLL VCO1 is set to normal speed, and the output is 1/1 frequency-divided.
0	0	1	Multiplier PLL VCO1 is set to normal speed, and the output is 1/2 frequency-divided.
0	1	0	Multiplier PLL VCO1 is set to normal speed, and the output is 1/4 frequency-divided.
0	1	1	Multiplier PLL VCO1 is set to normal speed, and the output is 1/8 frequency-divided.
1	0	0	Multiplier PLL VCO1 is set to high speed*, and the output is 1/1 frequency-divided.
1	0	1	Multiplier PLL VCO1 is set to high speed*, and the output is 1/2 frequency-divided.
1	1	0	Multiplier PLL VCO1 is set to high speed*, and the output is 1/4 frequency-divided.
1	1	1	Multiplier PLL VCO1 is set to high speed*, and the output is 1/8 frequency-divided.

* Approximately twice the normal speed

Command bit			Processing
VCOSEL2	KSL1	KSL0	
0	0	0	Wide-band PLL VCO2 is set to normal speed, and the output is 1/1 frequency-divided.
0	0	1	Wide-band PLL VCO2 is set to normal speed, and the output is 1/2 frequency-divided.
0	1	0	Wide-band PLL VCO2 is set to normal speed, and the output is 1/4 frequency-divided.
0	1	1	Wide-band PLL VCO2 is set to normal speed, and the output is 1/8 frequency-divided.
1	0	0	Wide-band PLL VCO2 is set to high speed*, and the output is 1/1 frequency-divided.
1	0	1	Wide-band PLL VCO2 is set to high speed*, and the output is 1/2 frequency-divided.
1	1	0	Wide-band PLL VCO2 is set to high speed*, and the output is 1/4 frequency-divided.
1	1	1	Wide-band PLL VCO2 is set to high speed*, and the output is 1/8 frequency-divided.

* Approximately twice the normal speed

$9X commands

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
Function specifications	DCLV ON-OFF	DSPB ON-OFF	A.SEQ ON-OFF	D.PLL ON-OFF	BiliGL MAIN	BiliGL SUB	FLFC	0

<table>
<tr><th>Command bit</th><th>CLV mode</th><th colspan="2">Contents</th></tr>
<tr><td rowspan="2">DCLV on/off = 0</td><td>In CLVS mode</td><td colspan="2">FSW = low, MON = high, MDS = Z; MDP = servo control signal, carrier frequency of 230Hz at TB = 0, and 460Hz at TB = 1.</td></tr>
<tr><td>In CLVP mode</td><td colspan="2">FSW = Z, MON = high; MDS = speed control signal, carrier frequency of 7.35kHz; MDP = phase control signal, carrier frequency of 1.8kHz.</td></tr>
<tr><td rowspan="2">DCLV on/off = 1
(FSW, MON not required)</td><td rowspan="2">In CLVS and CLVP modes</td><td>When DCLV PWM and MD = 1
(Prohibited in CLV-W and CAV-W modes)</td><td>MDS = PWM polarity signal, carrier frequency of 132kHz.
MDP = PWM absolute value output (binary), carrier frequency of 132kHz.</td></tr>
<tr><td>When DCLV PWM and MD = 0</td><td>MDS = Z
MDP = ternary PWM output, carrier frequency of 132kHz.</td></tr>
</table>

When DCLV on/off = 1 for the Digital CLV servo, the sampling frequency of the internal digital filter switches simultaneously with the CLVP/CLVS switching.
Therefore, the cut-off frequency for the CLVS is fc = 70Hz when T_B = 0, and fc = 140Hz when T_B = 1.

Command bit	Processing
DSPB = 0	Normal-speed playback, C2 error correction quadruple correction.
DSPB = 1	Double-speed playback, C2 error correction double correction.

FLFC is normally 0.
FLFC is 1 in CAV-W mode, for any playback speed.

Command bit	Meaning
DPLL = 0 *	RFPLL is analog. PDO, VCOI and VCOO are used.
DPLL = 1	RFPLL is digital. PDO is high impedance.

* External parts for the FILI, FILO, PCO pins are required even when analog PLL is selected.

Command bit	BiliGL MAIN = 0	BiliGL MAIN = 1
BiliGL SUB = 0	STEREO	MAIN
BiliGL SUB = 1	SUB	Mute

Definition of bilingual capable MAIN, SUB and STEREO:

The left channel input is output to the left and right channels for MAIN.

The right channel input is output to the left and right channels for SUB.

The left and right channel inputs are output to the left and right channels for STEREO.

Command	Data 3				Data 4			
	D11	D10	D9	D8	D7	D6	D5	D4
Function specifications	DAC EMPH	DAC ATT	0	0	PLM3	PLM2	PLM1	PLM0

The command bits control the DAC.

Note) For normal stereo, channel 1 is the left channel and channel 2 is the right channel.

Command bit	Processing
DAC EMPH = 1	Applies digital de-emphasis. When Fs = 44.1kHz, the emphasis constants are $\tau 1$ = 50µs and $\tau 2$ = 15µs.
DAC EMPH = 0	Turns digital de-emphasis off.

Command bit	Processing
DAC ATT = 1	Identical digital attenuation control is used for both channels 1 and 2. When common attenuation data is specified, the attenuation values for channel 1 is used.
DAC ATT = 0	Independent digital attenuation control is used for both channels 1 and 2.

• DAC PLAY MODE

Command	D7	D6	D5	D4
DAC play mode	PLM3	PLM2	PLM1	PLM0

By controlling these command bits, the DAC outputs channel 1 and channel 2 can be output in 16 different combinations of left channel, right channel, left + right channel, and mute.

The relationship between the commands and the outputs is shown on the table on the following page.

PLM3	PLM2	PLM1	PLM0	Channel 1 output	Channel 2 output	Remarks
0	0	0	0	Mute	Mute	Mute
0	0	0	1	L	Mute	
0	0	1	0	R	Mute	
0	0	1	1	L + R	Mute	
0	1	0	0	Mute	L	
0	1	0	1	L	L	
0	1	1	0	R	L	Reverse
0	1	1	1	L + R	L	
1	0	0	0	Mute	R	
1	0	0	1	L	R	Stereo
1	0	1	0	R	R	
1	0	1	1	L + R	R	
1	1	0	0	Mute	L + R	
1	1	0	1	L	L + R	
1	1	1	0	R	L + R	
1	1	1	1	L + R	L + R	Mono

Note) For normal stereo, channel 1 is the left channel and channel 2 is the right channel.
The output data of L+R is (L+R)/2 to prevent overflow.

$AX commands

Command	Data 1				Data 2			
	D3	D2	D1	D0	D3	D2	D1	D0
Audio CTRL	0	0	Mute	ATT	PCT1	PCT2	DADS	SOC2

Command bit	Meaning
Mute = 0	Mute off if other mute conditions are not set.
Mute = 1	Mute on. Peak register reset.

Command bit	Meaning
ATT = 0	Attenuation off
ATT = 1	–12dB

Mute conditions

(1) When register A mute = 1.
(2) When Mute pin = 1.
(3) When register 8 D.out Mute F = 1 and the Digital Out is on (MD2 pin =1).
(4) When GFS stays low for over 35ms (during normal-speed).
(5) When register 9 BiliGL MAIN = Sub =1.
(6) When register A PCT1 = 1 and PCT2 = 0.

(1) to (4) perform zero-cross muting with a 1 ms time limit.

Command bit		Meaning	PCM Gain	ECC error correction ability
PCT1	PCT2			
0	0	Normal mode	× 0dB	C1: double; C2: quadruple
0	1	Level meter mode	× 0dB	C1: double; C2: quadruple
1	0	Peak meter mode	Mute	C1: double; C2: double
1	1	Normal mode	× 0dB	C1: double; C2: double

Description of level meter mode (See the Timing Chart 1-4.)

- When the LSI is set to this mode, it performs digital level meter functions.
- When the 96-bit clock is input to SQCK, 96 bits of data are output to SQSO.
  The initial 80 bits are Sub Q data. (See §2. Subcode Interface.) The last 16 bits are LSB first, which are 15-bit PCM data (absolute values) and L/R flag.
  L/R flag is high when the 15-bit PCM data is from the left channel and low from the right channel.
- PCM data is reset zero and the L/R flag is reversed after one readout.
  Then level measuring continues until the next readout.

Description of peak meter mode (See the Timing Chart 1-5.)

- When the LSI is set to this mode, the maximum PCM data value is detected regardless of if it comes from the left or right channel.
  The 96-bit clock must be input to SQCK to read out this data.
- When the 96-bit clock is input, 96 bits of data are output to SQSO and the LSI internal register is set the value again.
  In other words, the PCM maximum value detection register is not reset to zero by the readout.
- To reset the PCM maximum value register to zero, set PCT1 = PCT2 = 0 or set the $AX mute.
- The Sub Q absolute time is automatically controlled in this mode.
  In other words, after the maximum value is generated, the absolute time for CRC to become OK is retained in the memory. Normal operation is conducted for the relative time.
- The final bit (L/R flag) of the 96-bit data is normally 0.
- The pre-value hold and average value interpolation data are fixed to level (– ∞) in this mode.

Command bit	Processing
DADS = 0	Set to 0 when crystal = 33.8688MHz.
DADS = 1	Set to 1 when crystal = 16.9344MHz.

Command bit	Processing
SOC2 = 0	The SENS signal is output from the SENS pin as usual.
SOC2 = 1	The SQSO pin signal is output from the SENS pin.

SENS output switching

- This enables the SQSO pin signal to be output from the SENS pin.
  When SOC2 = 0, SENS output is performed as usual.
  When SOC2 = 1, the SQSO pin signal is output from the SENS pin.
  At this time, the readout clock is input to the SCLK pin.

Note) SOC2 should be switched when SQCK = SCLK = high.

• DAC digital attenuator

Command	Data 3				Data 4				Data 5				Data 6			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
Audio Ctrl	AT1D7	AT1D6	AT1D5	AT1D4	AT1D3	AT1D2	AT1D1	AT1D0	AT2D7	AT2D6	AT2D5	AT2D4	AT2D3	AT2D2	AT2D1	AT2D0

Note) AT1D7 to AT1D0 are the channel 1 ATT control bits.
AT2D7 to AT2D0 are the channel 2 ATT control bits.

Command bits AT1D7 to AT1D0 (AT2D7 to AT2D0)	Audio output
FF (H)	0dB
FE (H) ↓ 01 (H)	–0.034dB ↓ –48.131dB
00 (H)	– ∞

The attenuation data consists of 8 bits each for channels 1 and 2; the DAC ATT bit can be used to control channels 1 and 2 with common attenuation data. (When common attenuation data is specified, the attenuation values for channel 1 is used.)

An attenuation value, from 00(H) to FF(H), is determined according to the following expression:

ATT = 20 log [input data/255] dB

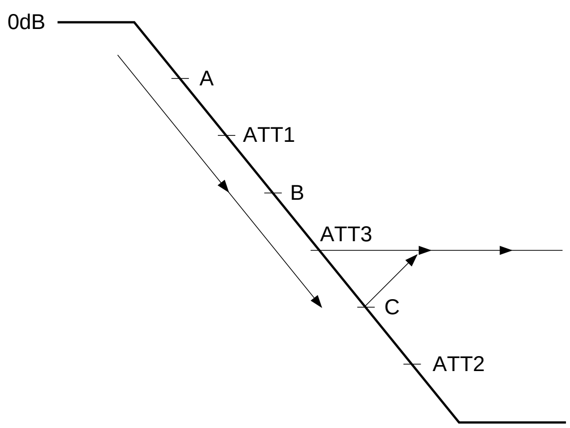
Example: When the attenuation data is FA(H):
ATT = 20 log [250/255] dB = –0.172dB

• Soft mute

With the soft mute function, when the attenuation data goes from FF(H) to 00(H) and vice versa, muting is turned on and off over the muting time of 1024fs [s] = 23.2 [ms] (Fs = 44.1kHz).

• Attenuation

Assume the attenuation data ATT1, ATT2, and ATT3, where ATT1 > ATT3 > ATT2. First, assume ATT1 is transferred and then ATT2 is transferred. If ATT2 is transferred before ATT1 is reached (state "A" in the diagram), then the value continues approaching ATT2. Next, if ATT3 is transferred before ATT2 is reached (state "B" or "C" in the diagram), the attenuation begins approaching ATT3 from the current point. Note that it takes 1024/Fs [s] (Fs = 44.1kHz for CD players) to transit between attenuation data (from 0dB to – ∞).



Handling of the Attenuation Value

• **I/O sync circuit**

Related pins: LRCK and XWO
During normal operation, the I/O sync circuit automatically synchronizes with the input LRCK, and its operation proceeds in phase with the serial input data. However, there is a chance that synchronization will not be performed if there is a great deal of jitter in LRCK, if the power has just been turned on, etc. In this case, forced synchronization is possible by setting XWO low for 2/Fs or more. The forced synchronization operation is performed at the second rising edge of LRCK after the XWO pin is set low.

$BX commands

This command sets the traverse monitor count.

Command	Data 1				Data 2				Data 3				Data 4			
	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4
Traverse monitor count setting	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

- When the set number of tracks are counted during fine search, the sled control for the traverse cycle control goes off.
- The traverse monitor count is set to monitor the traverse status from the SENS output as COMP and COUT.

$CX commands

Command	Data 1				Data 2				Explanation
	D3	D2	D1	D0	D3	D2	D1	D0	
Servo coefficient setting	Gain MDP1	Gain MDP0	Gain MDS1	Gain MDS0	Gain DCLV1	Gain DCLV0	0	0	Valid only when DCLV = 1.
CLV CTRL ($DX)				Gain CLVS					Valid when DCLV = 1 or 0.

The spindle servo gain is externally set when DCLV = 1.

• CLVS mode gain setting: GCLVS

Gain MDS1	Gain MDS0	Gain CLVS	GCLVS
0	0	0	–12dB
0	0	1	–6dB
0	1	0	–6dB
0	1	1	0dB
1	0	0	0dB
1	0	1	+6dB

Note) When DCLV = 0, the CLVS gain is as follows.
When Gain CLVS = 0, GCLVS = –12dB.
When Gain CLVS = 1, GCLVS = 0dB.

• CLVP mode gain setting: GMDP, GMDS

Gain MDP1	Gain MDP0	GMDP
0	0	–6dB
0	1	0dB
1	0	+6dB

Gain MDS1	Gain MDS0	GMDS
0	0	–6dB
0	1	0dB
1	0	+6dB

• DCLV overall gain setting: GDCLV

Gain DCLV1	Gain DCLV0	GDCLV
0	0	0dB
0	1	+6dB
1	0	+12dB

$DX commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
CLV CTRL	DCLV PWM MD	TB	TP	Gain CLVS	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0

See the $CX commands.

Command bit	Explanation
DCLV PWM MD = 1	Digital CLV PWM mode specified. Both MDS and MDP are used. CLV-W and CAV-W modes can not be used.
DCLV PWM MD = 0	Digital CLV PWM mode specified. Ternary MDP values are output. CLV-W and CAV-W modes can be used.

Command bit	Explanation
TB = 0	Bottom hold at a cycle of RFCK/32 in CLVS and CLVH modes.
TB = 1	Bottom hold at a cycle of RFCK/16 in CLVS and CLVH modes.
TP = 0	Peak hold at a cycle of RFCK/4 in CLVS mode.
TP = 1	Peak hold at a cycle of RFCK/2 in CLVS mode.

• **For the CXD2586R**

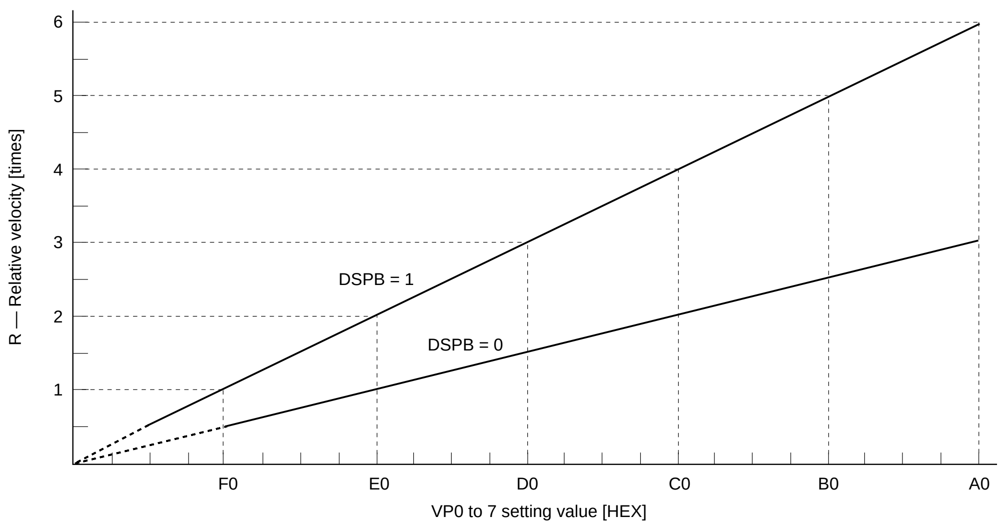
Command bit	Description
VP0 to 7 = F0 (H)	Playback at half (normal) speed
:	to
VP0 to 7 = E0 (H)	Playback at normal (double) speed
:	to
VP0 to 7 = C0 (H)	Playback at double (quadruple) speed
:	to
VP0 to 7 = A0 (H)	Playback at (sextuple) speed

The rotational velocity R of the spindle can be expressed with the following equation.

$$R = \frac{256 - n}{32}$$

R: Relative velocity at normal speed = 1
n: VP0 to 7 setting value

Note)
1. Values when MCLK is 16.9344MHz and XTSL is low or when MCLK is 33.8688MHz and XTSL is high.
2. Values in parentheses are for when DSPB is 1.

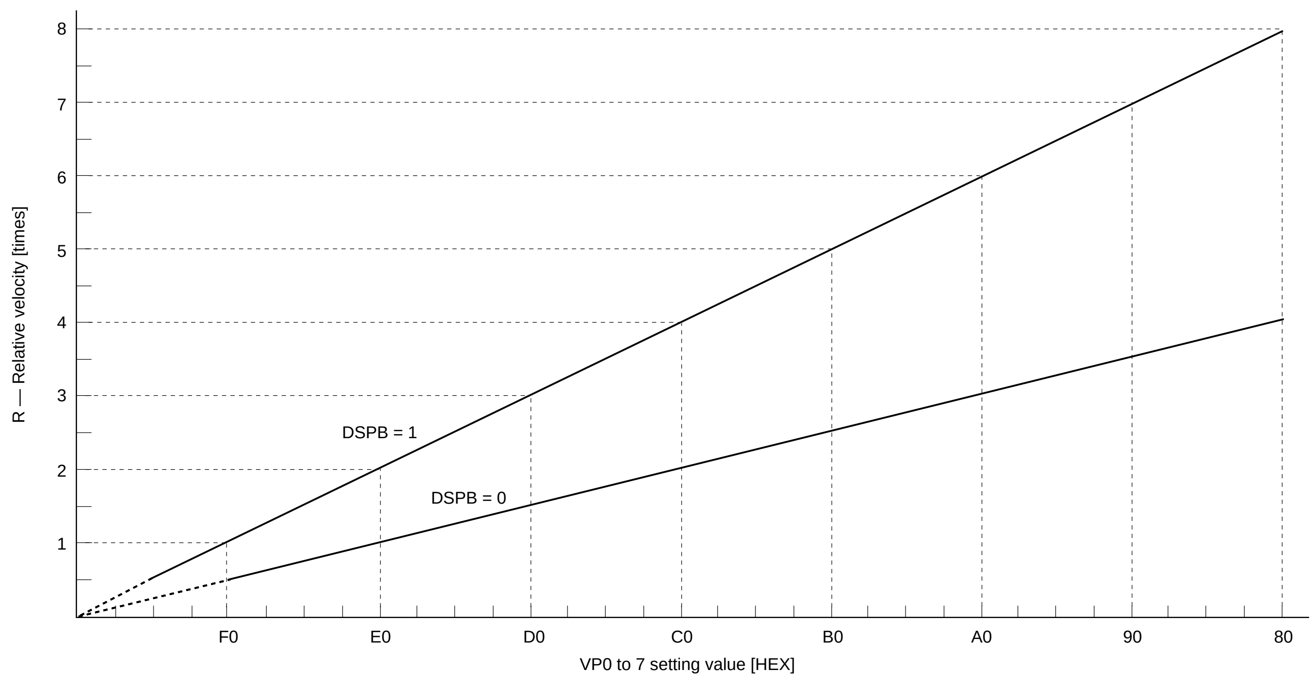


• **For the CXD2586R-1**

Command bit	Description
VP0 to 7 = F0 (H)	Playback at half (normal) speed
:	to
VP0 to 7 = E0 (H)	Playback at normal (double) speed
:	to
VP0 to 7 = C0 (H)	Playback at double (quadruple) speed
:	to
VP0 to 7 = A0 (H)	Playback at triple (sextuple) speed
:	to
VP0 to 7 = 80 (H)	Playback at (octuple) speed

Note)

1. Values when MCLK is 16.9344MHz and XTSL is low or when MCLK is 33.8688MHz and XTSL is high.
2. Values in parentheses are for when DSPB is 1.



$EX commands

Command	Data 1				Data 2				Data 3			
	D3	D2	D1	D0	D3	D2	D1	D0	D3	D2	D1	D0
SPD mode	CM3	CM2	CM1	CM0	EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON

Command bit				Mode	Explanation
CM3	CM2	CM1	CM0		
0	0	0	0	STOP	Spindle stop mode.*
1	0	0	0	KICK	Spindle forward rotation mode.*
1	0	1	0	BRAKE	Spindle reverse rotation mode. Valid only when LPWR=0, in any modes.*
1	1	1	0	CLVS	Rough servo mode. When the RF-PLL circuit isn't locked, this mode is used to pull the disc rotations within the RF-PLL capture range.
1	1	1	1	CLVP	PLL servo mode.
0	1	1	0	CLVA	Automatic CLVS/CLVP switching mode. Used for normal playback.

* See the Timing Charts 1-6 to 1-12.

Command bit								Mode	Explanation
EPWM	SPDC	ICAP	SFSL	VC2C	HIFC	LPWR	VPON		
0	0	0	0	0	0	0	0	CLV-N	Crystal reference CLV servo.
0	0	0	0	1	1	0	0	CLV-W	Used for playback in CLV-W mode.*
0	1	1	0	0	1	0	1	CAV-W	Spindle control with VP0 to 7.
1	0	1	0	0	1	0	1	CAV-W	Spindle control with the external PWM.

* Figs. 3-1 and 3-2 show the control flow with the microcomputer software in CLV-W mode.

Mode	DCLV	DCLV PWM MD	LPWR	Command	Timing chart
CLV-N	0	0	0	KICK	1-6 (a)
				BRAKE	1-6 (b)
				STOP	1-6 (c)
	1	0	0	KICK	1-7 (a)
				BRAKE	1-7 (b)
				STOP	1-7 (c)
		1	0	KICK	1-8 (a)
				BRAKE	1-8 (b)
				STOP	1-8 (c)
CLV-W	1	0	0	KICK	1-9 (a)
				BRAKE	1-9 (b)
				STOP	1-9 (c)
			1	KICK	1-10 (a)
				BRAKE	1-10 (b)
				STOP	1-10 (c)
CAV-W	1	0	0	KICK	1-11 (a)
				BRAKE	1-11 (b)
				STOP	1-11 (c)
			1	KICK	1-12 (a)
				BRAKE	1-12 (b)
				STOP	1-12 (c)

Mode	DCLV	DCLV PWM MD	LPWR	Timing chart
CLV-N	1	0	0	1-13
		1	0	1-14
CLV-W	1	0	0	1-15
			1	1-16
CAV-W	1	0	0	1-17 (CAV = 0)
			1	1-18 (CAV = 0)
			0	1-19 (CAV = 1)
			1	1-20 (CAV = 1)

Note) The CLV-W and CAV-W modes support control only by the ternary output of the MDP pin.
Therefore, set DCLV to 1 and DCLV PWM MD to 0 in CLV-W and CAV-W modes.

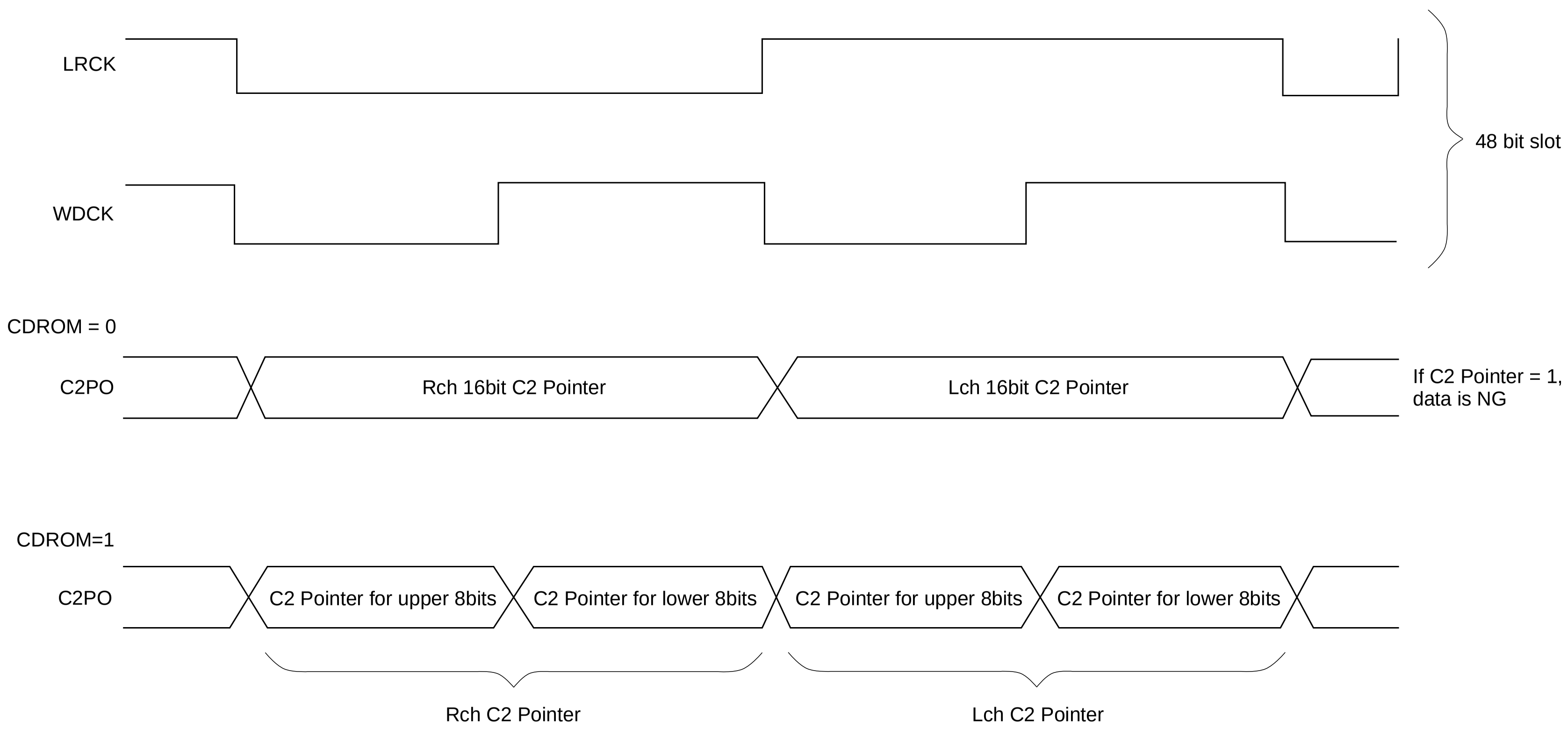
Command	Data 4			
	D3	D2	D1	D0
SPD mode	Gain CAV1	Gain CAV0	FCSW	0

Gain CAV1	Gain CAV0	Gain
0	0	0dB
0	1	–6dB
1	0	–12dB
1	1	–18dB

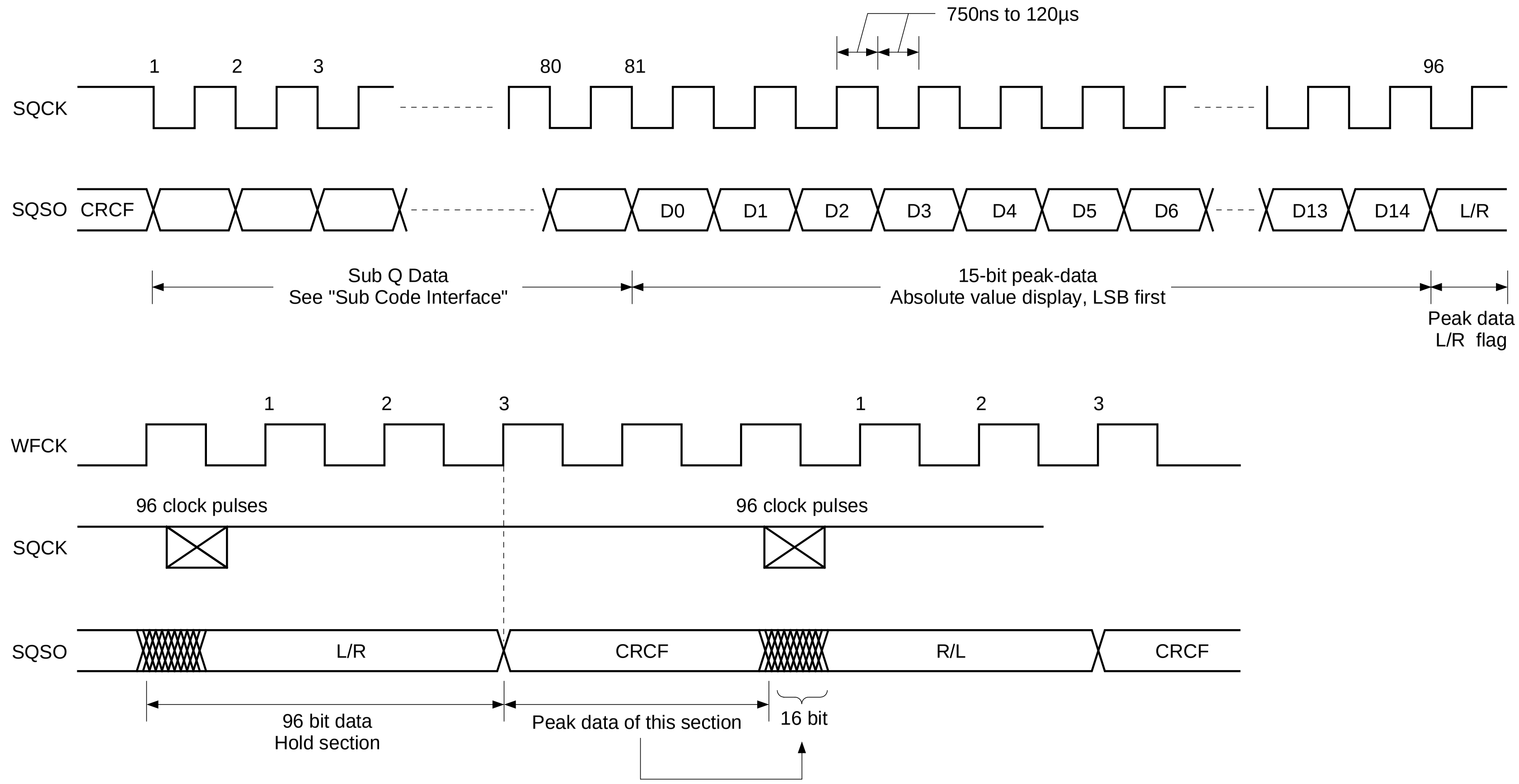
• This sets the gain when controlling the spindle with the phase comparator in CAV-W mode.

Command bit	Processing
FCSW = 0	The VPCO2 pin is not used and it is Hi-Z.
FCSW = 1	The VPCO2 pin is used and the pin signal is the same as VPCO1.

Timing Chart 1-3

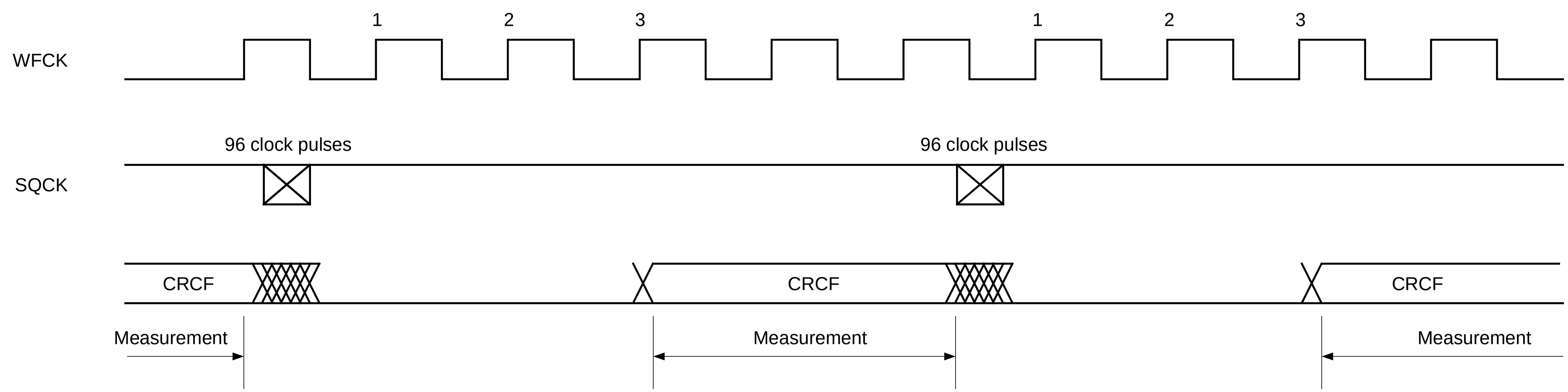


Timing Chart 1-4



Level Meter Timing

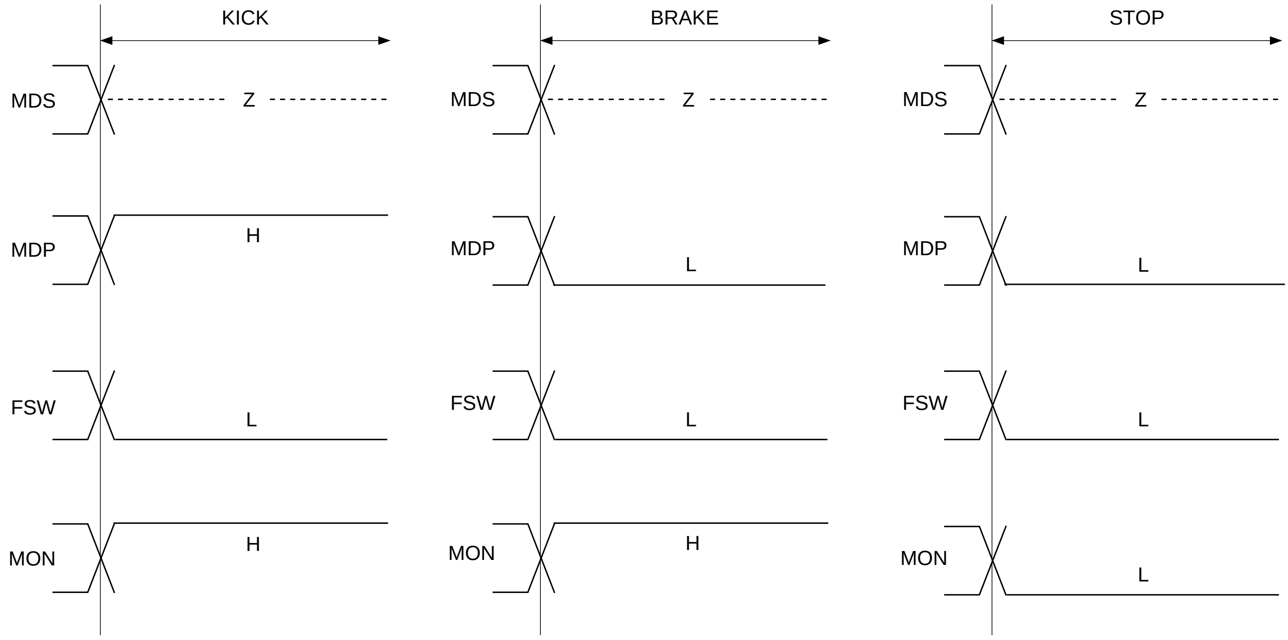
Timing Chart 1-5



Peak Meter Timing

Timing Chart 1-6

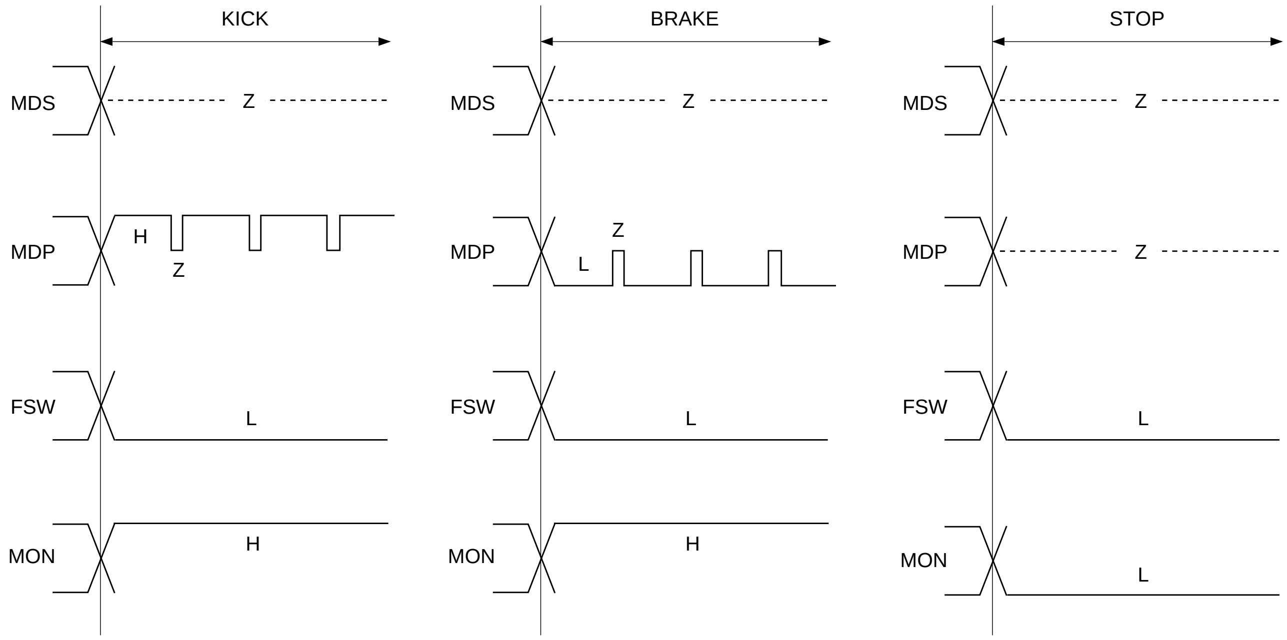
CLV-N mode DCLV = DCLV PWM MD = LPWR = 0



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-7

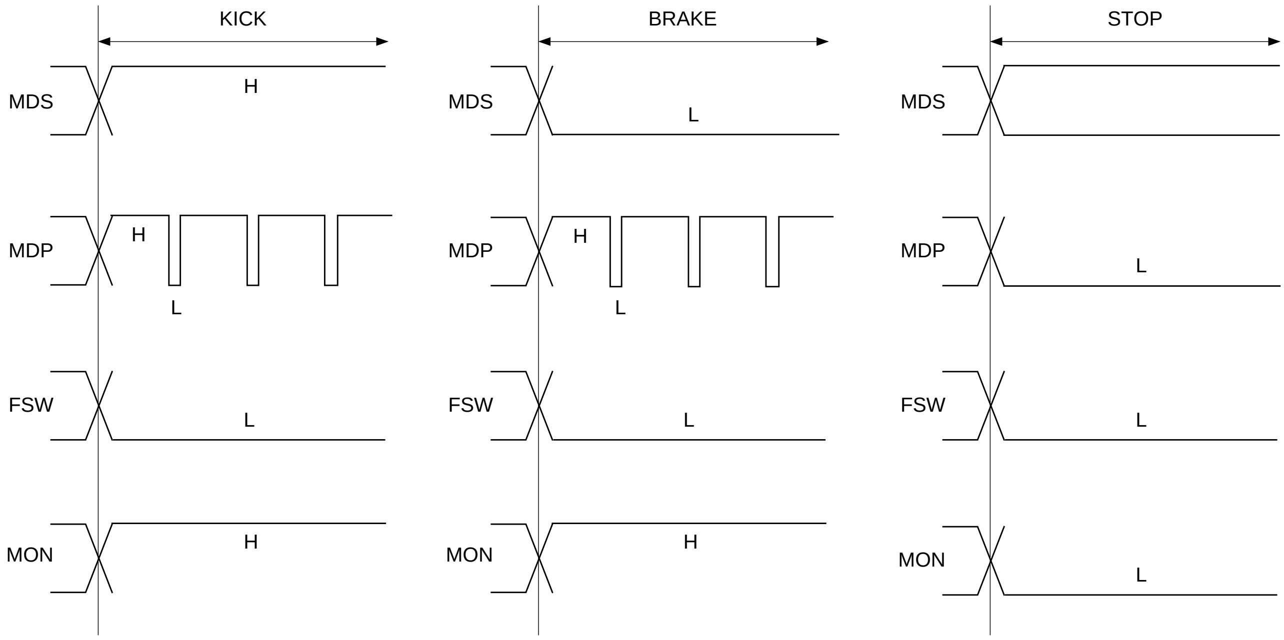
CLV-N mode DCLV = 1, DCLV PWM MD = LPWR = 0



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-8

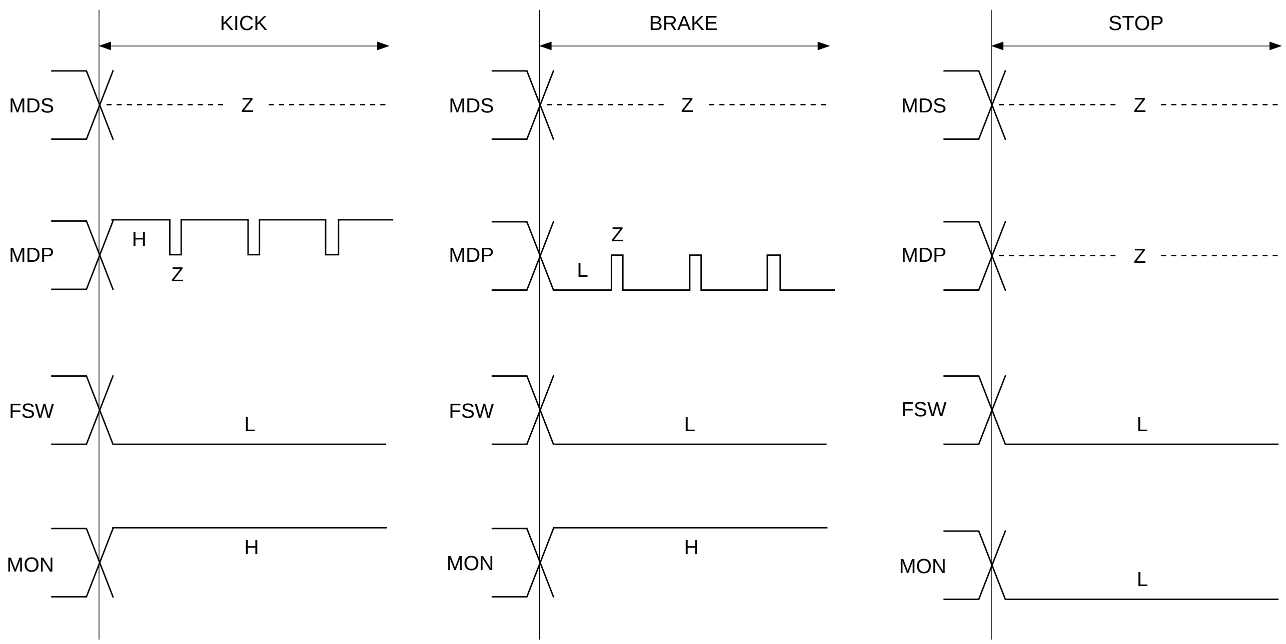
CLV-N mode DCLV = DCLV PWM MD = 1, LPWR = 0



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-9

CLV-W mode (when following the spindle rotational velocity) DCLV = 1, DCLV PWM MD = LPWR = 0



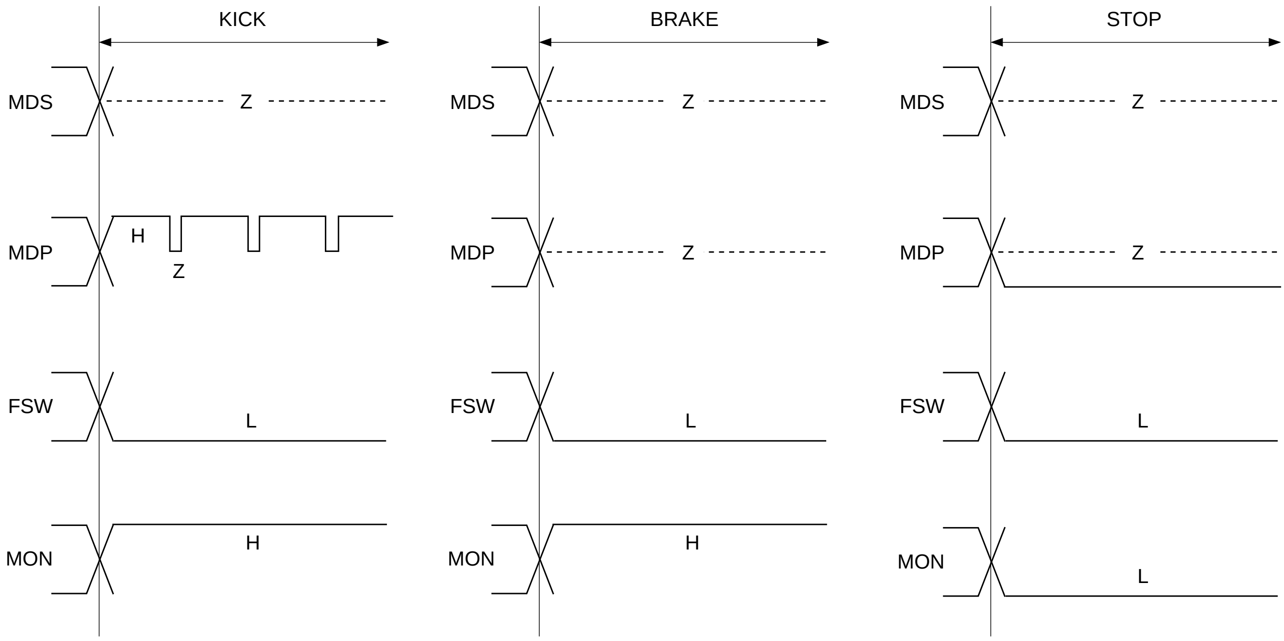
(a) KICK (b) BRAKE (c) STOP

Other than when following the velocity, the timing is the same as Timing Chart 1-6 (a).

Other than when following the velocity, the timing is the same as Timing Chart 1-6 (b).

Timing Chart 1-10

CLV-W mode (when following the spindle rotational velocity) DCLV = 1, DCLV PWM MD = 0, LPWR = 1

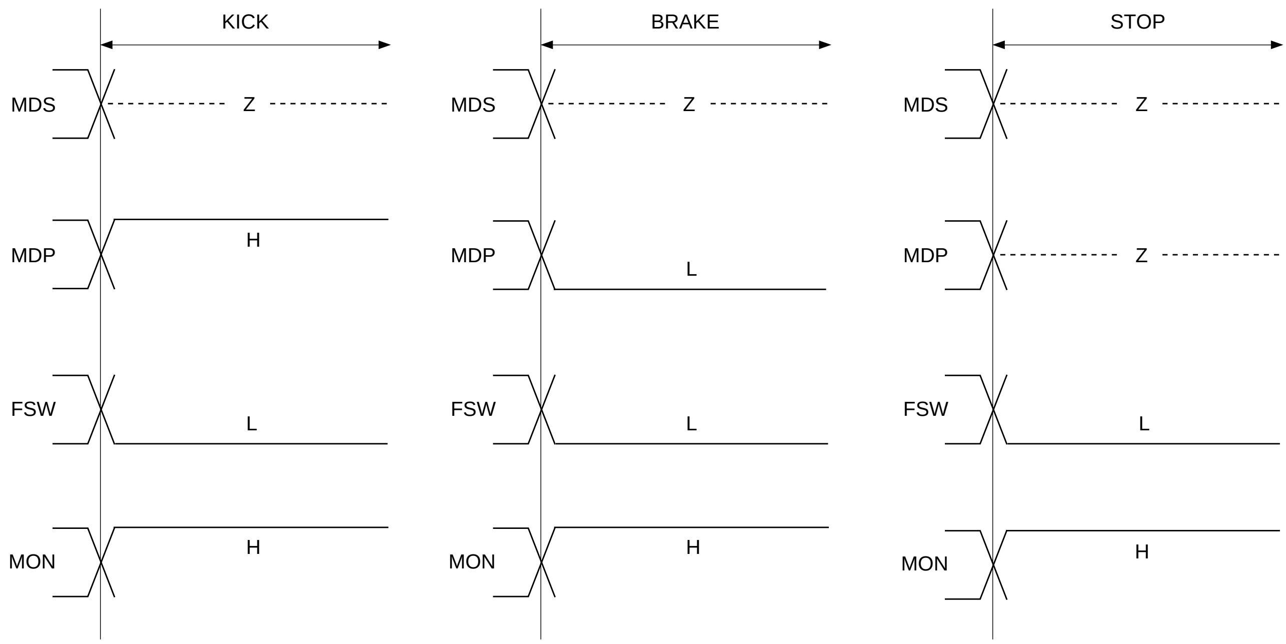


(a) KICK (b) BRAKE (c) STOP

Other than when following the velocity,
the timing is the same as Timing Chart 1-6 (a).

Timing Chart 1-11

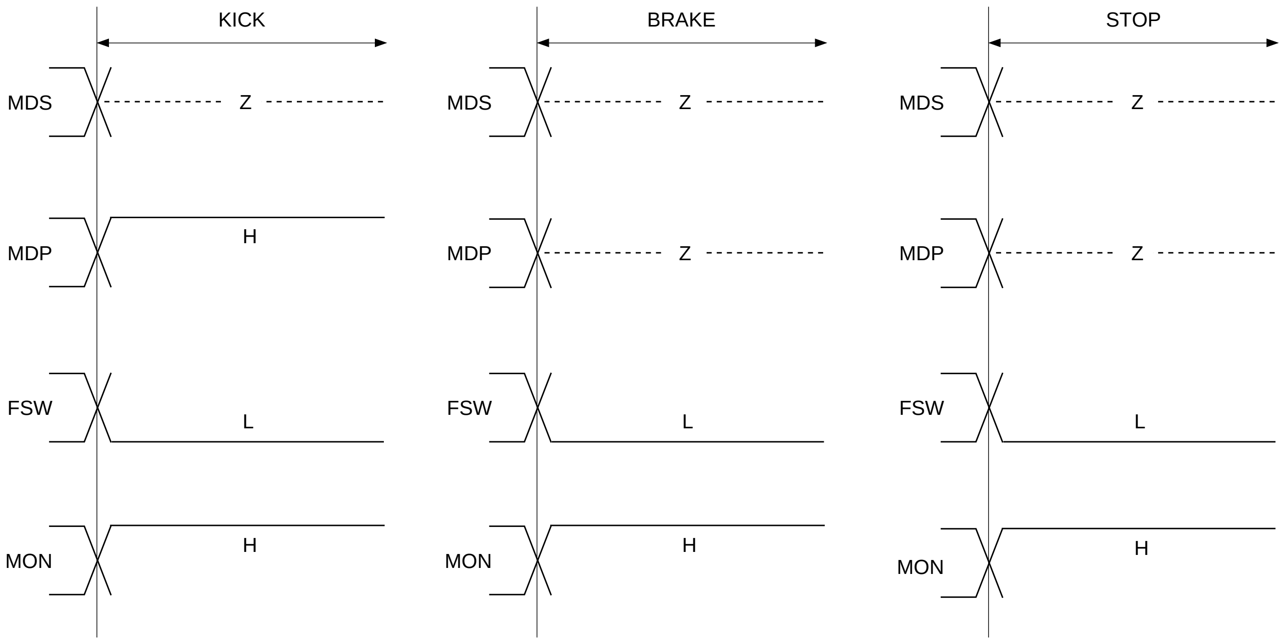
CAV-W mode DCLV = 1, DCLV PWM MD = LPWR = 0



(a) KICK (b) BRAKE (c) STOP

Timing Chart 1-12

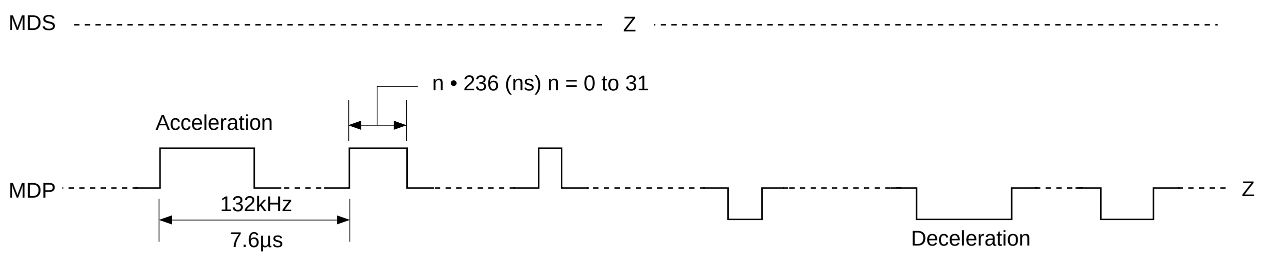
CAV-W mode DCLV = 1, DCLV PWM MD = 0, LPWR = 1



(a) KICK (b) BRAKE (c) STOP

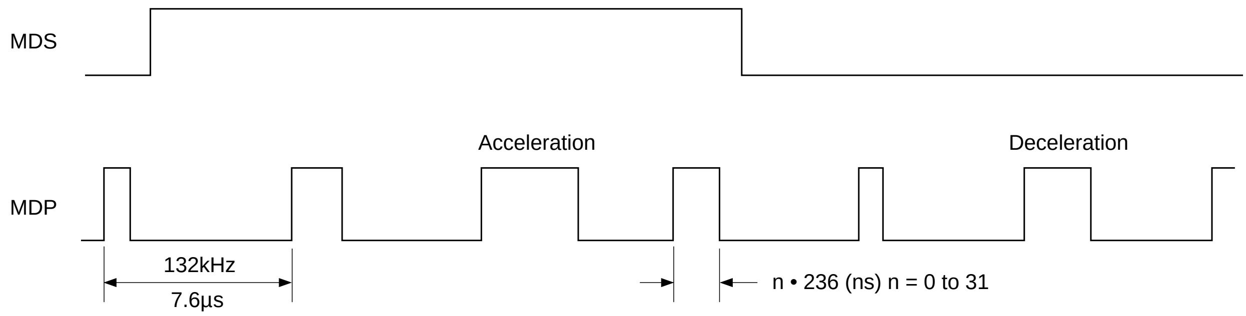
Timing Chart 1-13

CLV-N mode DCLV PWM MD = LPWR = 0



Timing Chart 1-14

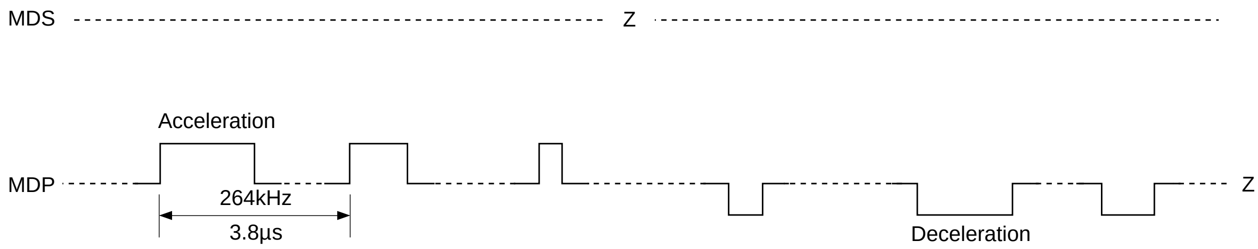
CLV-N mode DCLV PWM MD = 1, LPWR = 0



Output Waveforms with DCLV = 1

Timing Chart 1-15

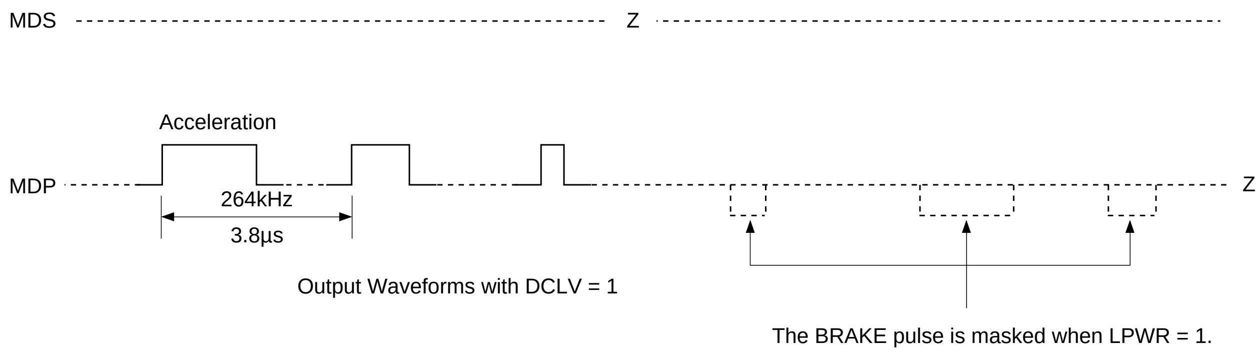
CLV-W mode DCLV PWM MD = LPWR = 0



Output Waveforms with DCLV = 1

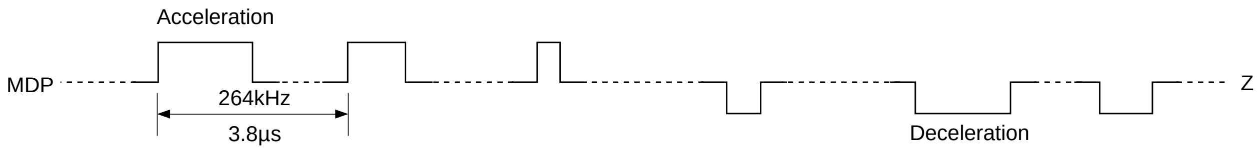
Timing Chart 1-16

CLV-W mode DCLV PWM MD = 0, LPWR = 1



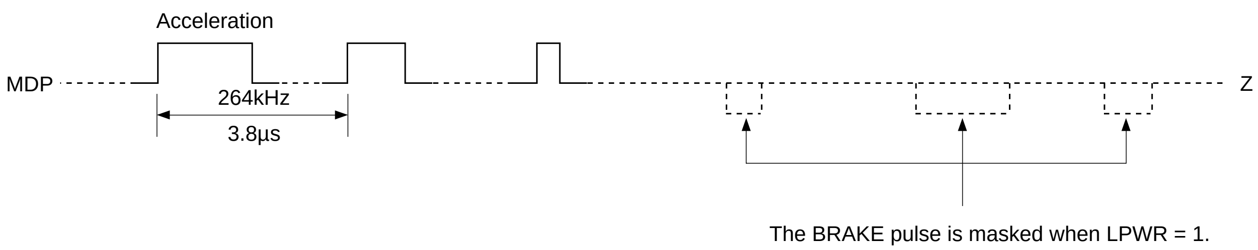
Timing Chart 1-17

CAV-W mode EPWM = DCLV PWM MD = LPWR = 0



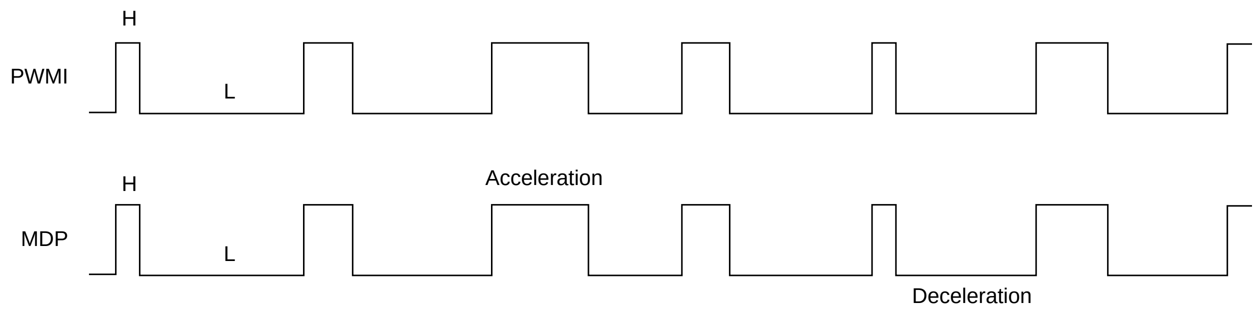
Timing Chart 1-18

CAV-W mode EPWM = 1, DCLV PWM MD = 0, LPWR = 1



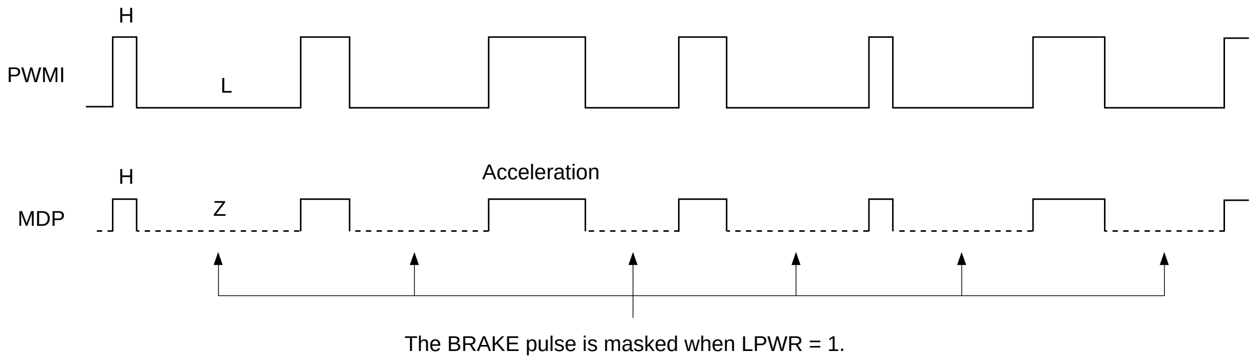
Timing Chart 1-19

CAV-W mode EPWM = 1, DCLV PWM MD = LPWR = 0



Timing Chart 1-20

CAV-W mode EPWM = 1, DCLV PWM MD = 0, LPWR = 1



Note) The CLV-W and CAV-W modes support control only by the ternary output of the MDP pin. Therefore, set DCLV PWM MD to 0 in CLV-W and CAV-W modes.

§2. Subcode Interface

There are two methods for reading out a subcode externally. The 8-bit subcodes P to W can be read from SBSO by inputting EXCK.
Sub Q can be read out after checking CRC of the 80 bits in the subcode frame.
Sub Q can be read out from the SQSO pin by inputting 80 clock pulses to SQCK pin when SCOR comes correctly and CRCF is high.

§2-1. P to W Subcode Readout

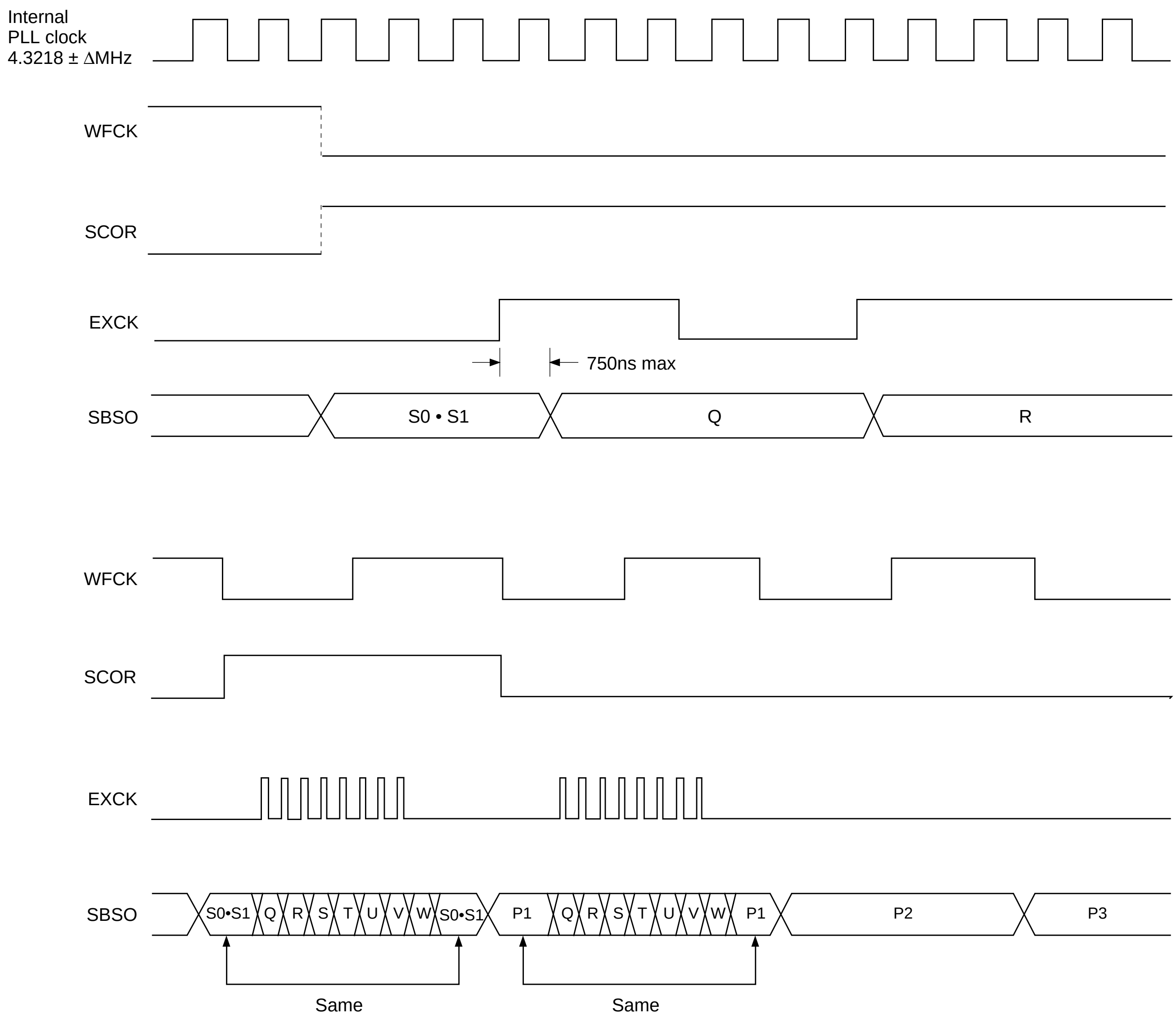
Data can be read out by inputting EXCK immediately after WFCK falls. (See the Timing Chart 2-1.)

§2-2. 80-bit Sub Q Readout

Fig. 2-2 shows the peripheral block of the 80-bit Sub Q register.

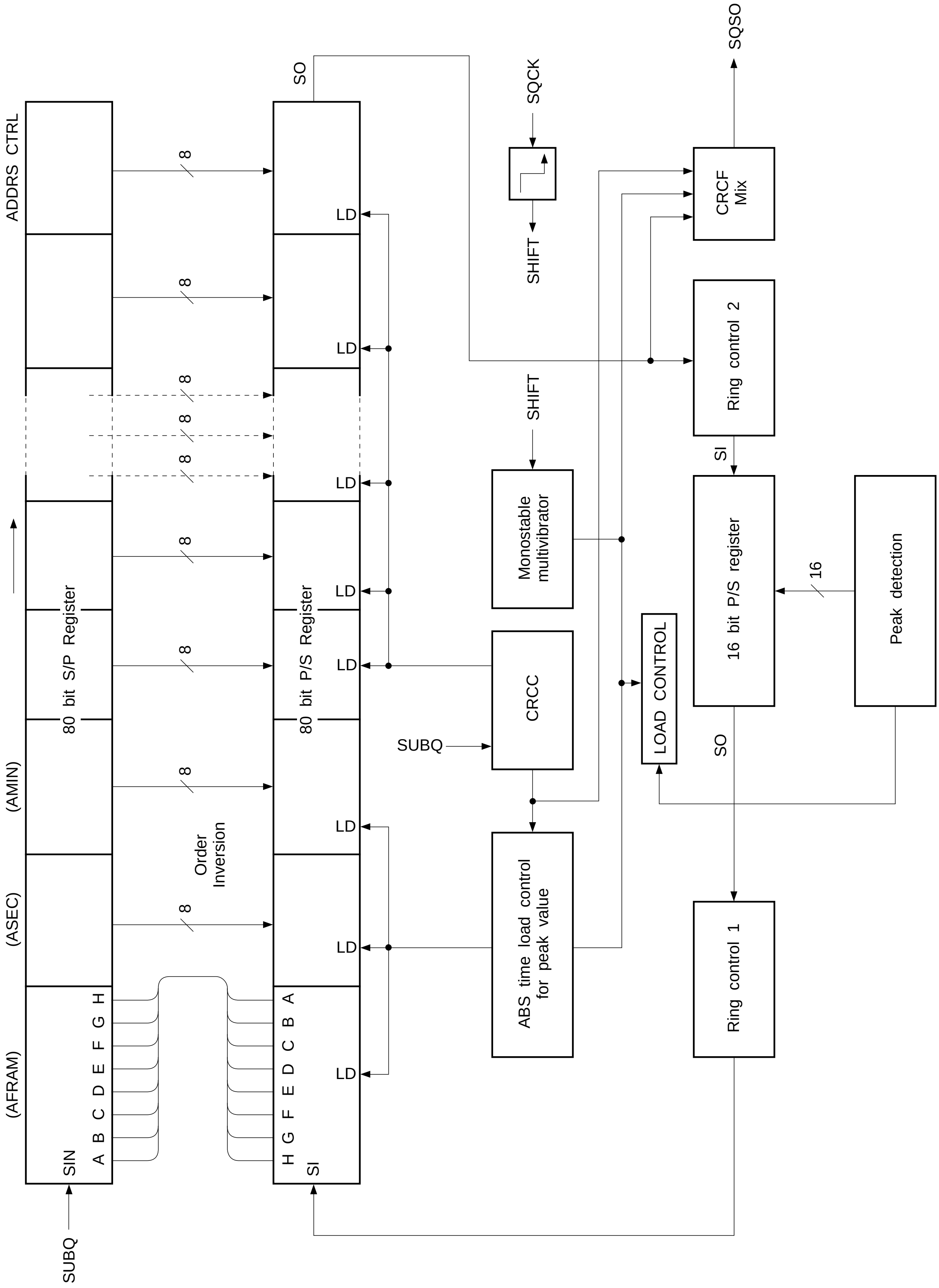
- First, Sub Q, regenerated at one bit per frame, is input to the 80-bit serial/parallel register and the CRC check circuit.
- 96-bit Sub Q has been inputted, and if the CRC is OK, it is output to SQSO with CRCF = 1. In addition, the 80 bits are loaded into the parallel/serial register.
  When SQSO goes high after SCOR is output, the CPU determines that new data (which passed the CRC check) has been loaded.
- In the CXD2586R/-1, when 80-bit data is loaded, the order of the MSB and LSB is inverted within each byte. As a result, although the sequence of the bytes is the same, the bits within the bytes are now ordered LSB first.
- Once the 80-bit data load is confirmed, SQCK is input so that the data can be read. The SQSO input is detected, and the retriggerable monostable multivibrator for low is reset.
- The retriggerable monostable multivibrator has a time constant from 270 to 400µs. When the duration when SQCK is high is less than this time constant, the monostable multivibrator is kept reset; during this interval, the S/P register is not loaded into the P/S register.
- While the monostable multivibrator is being reset, data cannot be loaded in the peak detection parallel/serial register or the 80-bit parallel/serial register.
  In other words, while reading out with a clock cycle shorter than this time constant, the register will not be rewritten by CRCOK and others.
- In this LSI, the previously mentioned peak detection register can be connected to the shift-in of the 80-bit P/S register.
  Input for ring control 1 is connected to the output of it in peak meter or level meter mode.
  Same goes for ring 2 in peak meter mode.
  This is because the register is reset with each readout in level meter mode, and to prevent readout destruction in peak meter mode.
  As a result , the 96-bit clock must be input in peak meter mode.
- The absolute time after peak is stored in the memory in peak meter mode. (See the Timing Chart 2-3.)
- The high and low intervals for SQCK should be between 750ns and 120µs.

Timing Chart 2-1

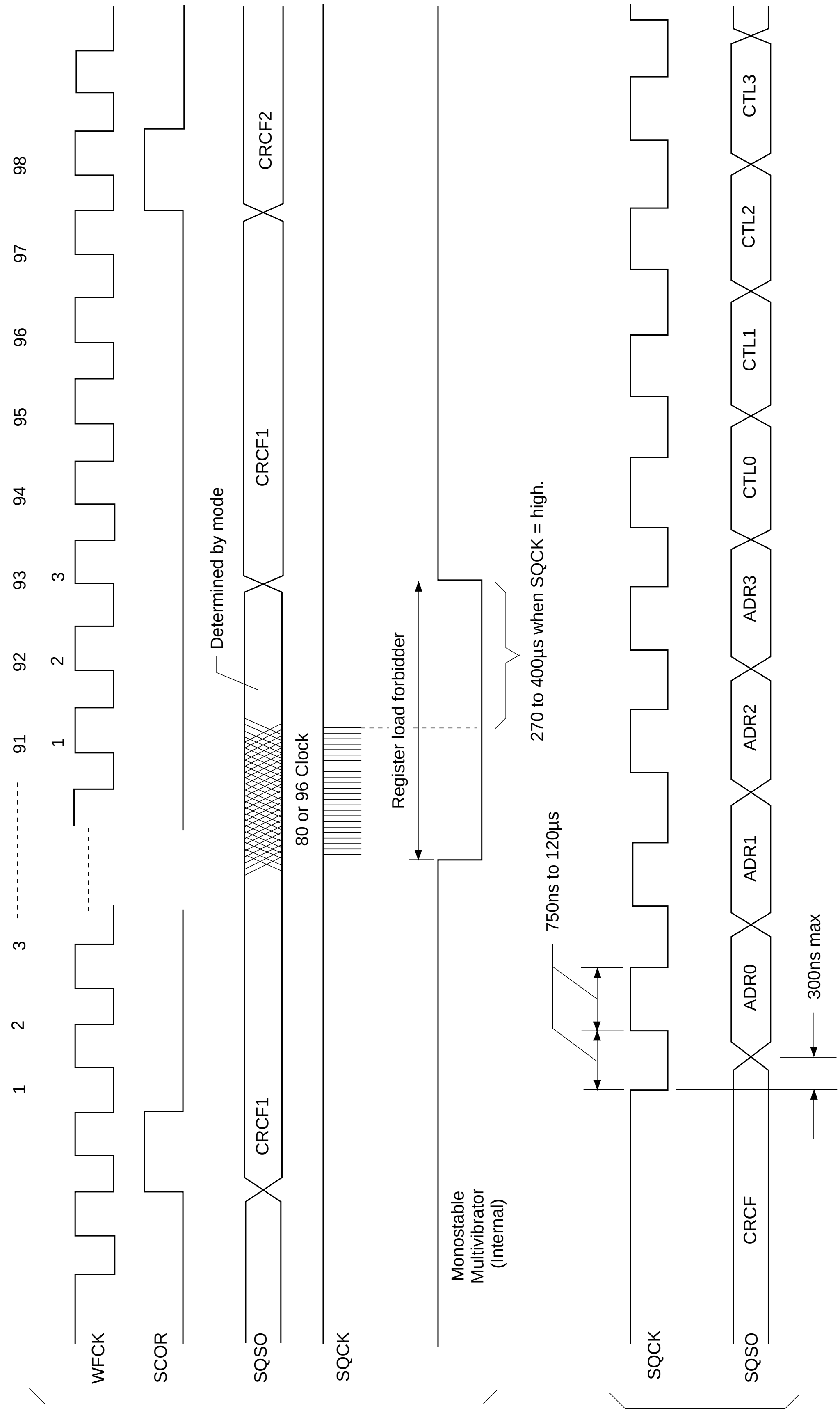


Subcode P.Q.R.S.T.U.V.W Read Timing

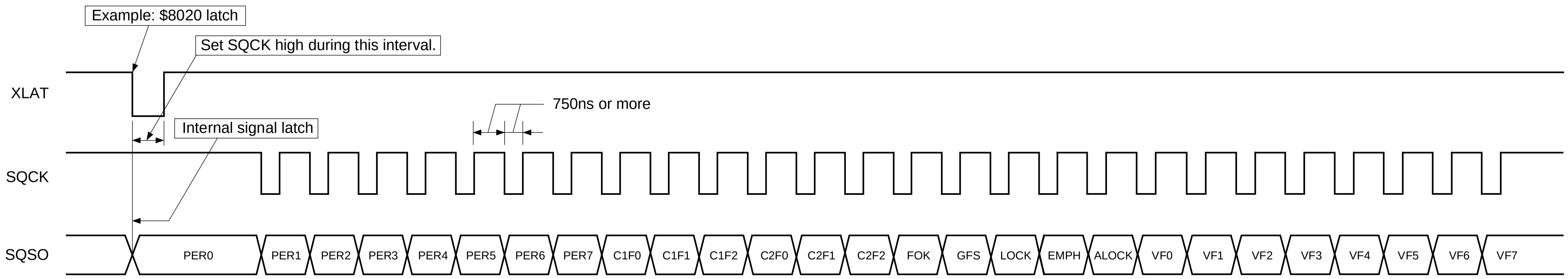
Block Diagram 2-2



Timing Chart 2-3



Timing Chart 2-4

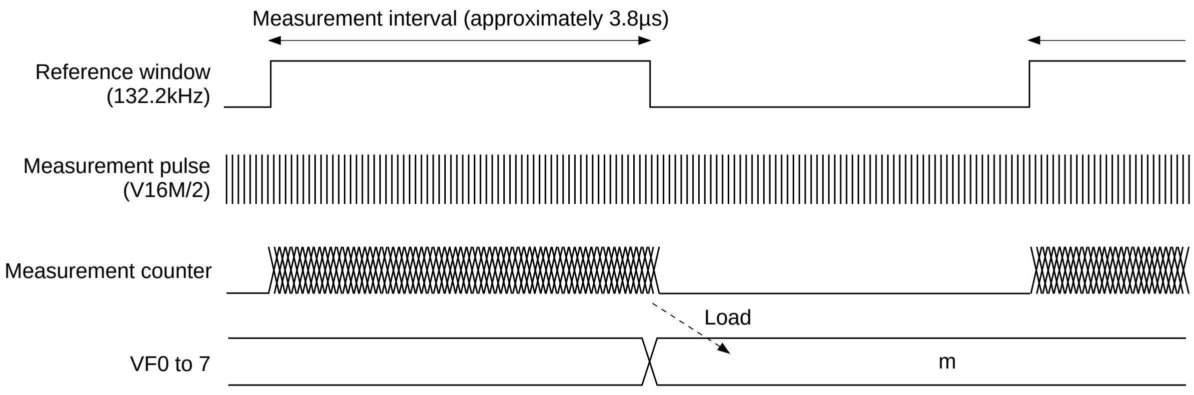


Signal	Explanation
PER0 to 7	RF jitter amount (used to adjust the focus bias). 8-bit binary data in PER0 = LSB, PER7 = MSB.
FOK	Focus OK
GFS	High when the frame sync and the insertion protection timing match.
LOCK	High when sampled value of GFS at 460Hz is high. Low when sampled value of GFS at 460Hz is low by 8 times successively.
EMPH	High when the playback disc has emphasis.
ALOCK	High when sampled value of GFS at 460Hz is high by 8 times successively. Low when sampled value of GFS at 460Hz is low by 8 times successively.
VF0 to 7	Used in CAV-W mode. The result obtained by measuring the rotational velocity of the disc. (See the Timing Chart 2-5.) VF0 = LSB, VF7 = MSB.

C1F2	C1F1	C1F0	Description
0	0	0	No C1 errors ; C1 pointer reset
0	0	1	One C1 error corrected ; C1 pointer reset
0	1	0	—
0	1	1	—
1	0	0	No C1 errors ; C1 pointer set
1	0	1	One C1 error corrected ; C1 pointer set
1	1	0	Two C1 errors corrected ; C1 pointer set
1	1	1	C1 correction impossible ; C1 pointer set

C2F2	C2F1	C2F0	Description
0	0	0	No C2 errors ; C2 pointer reset
0	0	1	One C2 error corrected ; C2 pointer reset
0	1	0	Two C2 errors corrected ; C2 pointer reset
0	1	1	Three C2 errors corrected; C2 pointer reset
1	0	0	—
1	0	1	Four C2 errors corrected ; C2 pointer reset
1	1	0	C2 correction impossible ; C1 pointer copy
1	1	1	C2 correction impossible ; C2 pointer set

Timing Chart 2-5



The relative velocity of the disc can be obtained with the following equation.

$$R = \frac{m + 1}{32} \quad \text{(R: Relative velocity, m: Measurement results)}$$

VF0 to 7 is the result obtained by counting VCKI/2 pulses while the reference signal (132.2kHz) generated from MCLK (384Fs) is high. This count is 31 when the disc is rotating at normal speed and 63 when it is rotating at double speed (when DSPB is low).

§3. Description of Modes

This LSI has three basic operating modes using a combination of spindle control and the PLL. The operations for each mode are described below.

§3-1. CLV-N Mode

This mode is compatible with the CXD2500 series, and operation is the same (however, variable pitch cannot be used). The PLL capture range is ±150kHz.

§3-2. CLV-W Mode

This is the wide capture range mode. This mode allows PLL to follow the rotational velocity of the disc. This rotational following control has two types: using the built-in VCO2 or providing an external VCO. The spindle is the same CLV servo as for the CXD2500 series. Operation using the built-in VCO2 is described below. (When using an external VCO, input the signal from the VPCO pin to the low-pass filter, use the output from the low-pass filter as the control voltage for the external VCO, and input the oscillation from the VCO to the VCKI pin.)
While starting to rotate a disc and/or speeding up to the lock range from the condition that a disc stops, CAV-W mode should be used. Concretely saying, firstly send $E665X to set CAV-W mode and kick a disc, secondly send $E60CX to set CLV-W mode if ALOCK is high, which can be read serially from SQSO pin. CLV-W mode can be used while ALOCK is high. The microcomputer monitors the serial data output, and must return to adjust speed operation (CAV-W mode) when ALOCK becomes low. The control flow according to the microcomputer software in CLV-W mode is shown in Fig. 3-2.
In CLV-W mode (normal), low power consumption is achieved by setting LPWR to high. Control was formerly performed by applying acceleration and deceleration pulses to the spindle motor. However, when LPWR is set to high, deceleration pulses are not output, thereby achieving low power consumption mode.
CLV-W mode supports control only by the ternary output of the MDP pin. Therefore, when using CLV-W mode, set DCLV PWM MD to low.

Note) The capture range for this mode is theoretically up to the signal processing limit.

§3-3. CAV-W Mode

This is the CAV mode. In this mode, it is possible to control spindle to variable rotational velocity, the external crystal is fixed though. The rotational velocity is determined by the VP0 to 7 setting values or the external PWM. When controlling the spindle with VP0 to 7, setting the CAV-W mode with $E665X command and controlling VP0 to 7 with the $DX commands allows the rotational velocity to be varied from low speed to sextuple-speed. (See $DX Commands.) Also, when controlling the spindle with the external PWM, the PWMI pin is binary input which becomes KICK during high intervals and BRAKE during low intervals.
The microcomputer can know the rotational velocity using V16M. And the reference for the velocity measurement is a signal of 132.2kHz obtained by 1/128 of MCLK (384Fs). The velocity is obtained by counting V16M/2 pulses while the reference is high, and the result is output from the new CPU interface as 8 bits (VP0 to 7). These measurement results are 31 when the disc is rotating at normal speed or 127 when it is rotating at quadruple speed. These values match those of the 256-n for control with VP0 to 7. (See Table 2-5 and Fig. 2-6.)
In CAV-W mode, the spindle is set to the desired rotational velocity and the operation speed for the entire system follows this rotational velocity. Therefore, the cycles for the Fs system clock, PCM data and all other output signals from this LSI change according to the rotational velocity of the disc.

Note) The capture range for this mode is theoretically up to the signal processing limit.
Note) Set FLFC to 1 for this mode.

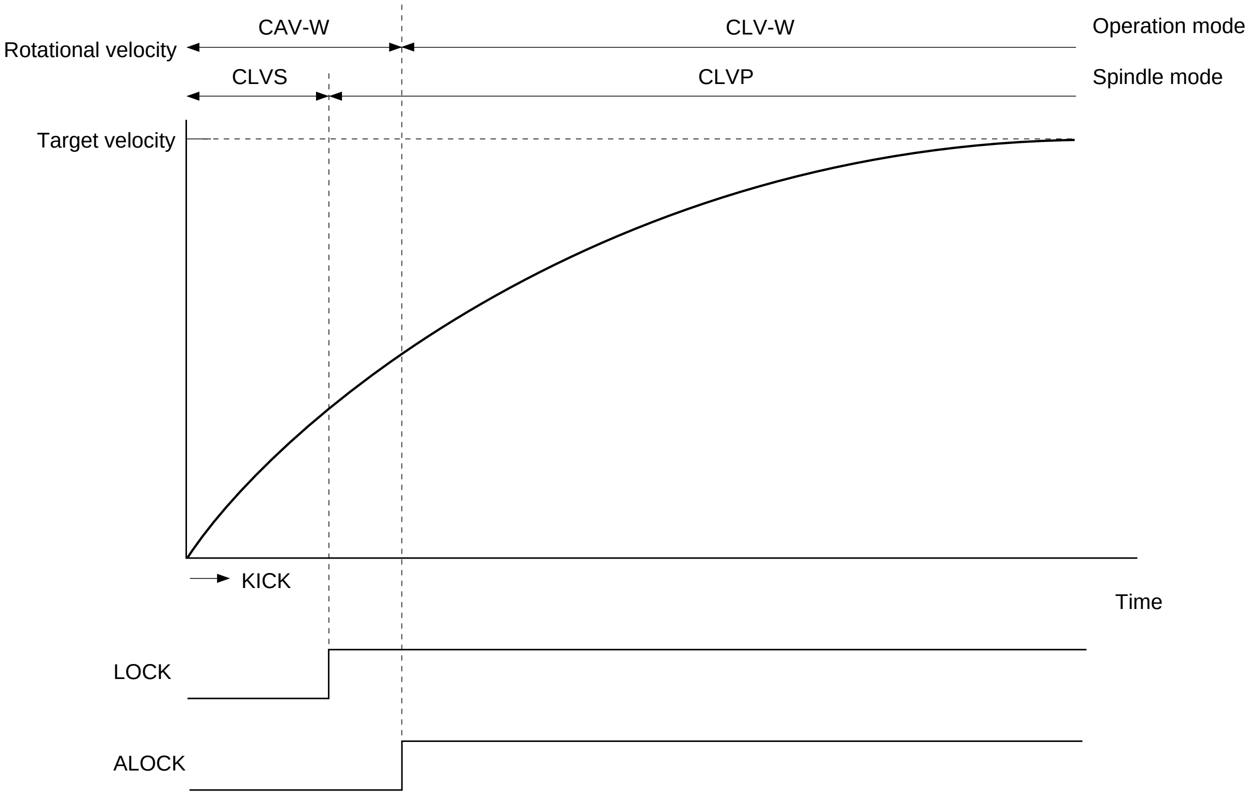


Fig. 3-1. Disc Stop to regular playback in CLV-W Mode

CLV-W Mode

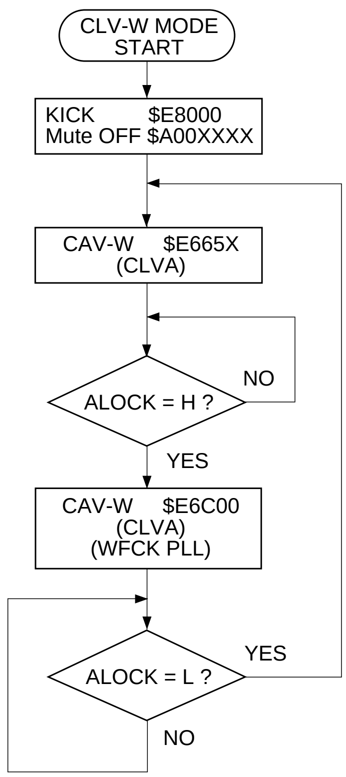


Fig. 3-2. CLV-W Mode Flow Chart

§4. Description of Other Functions

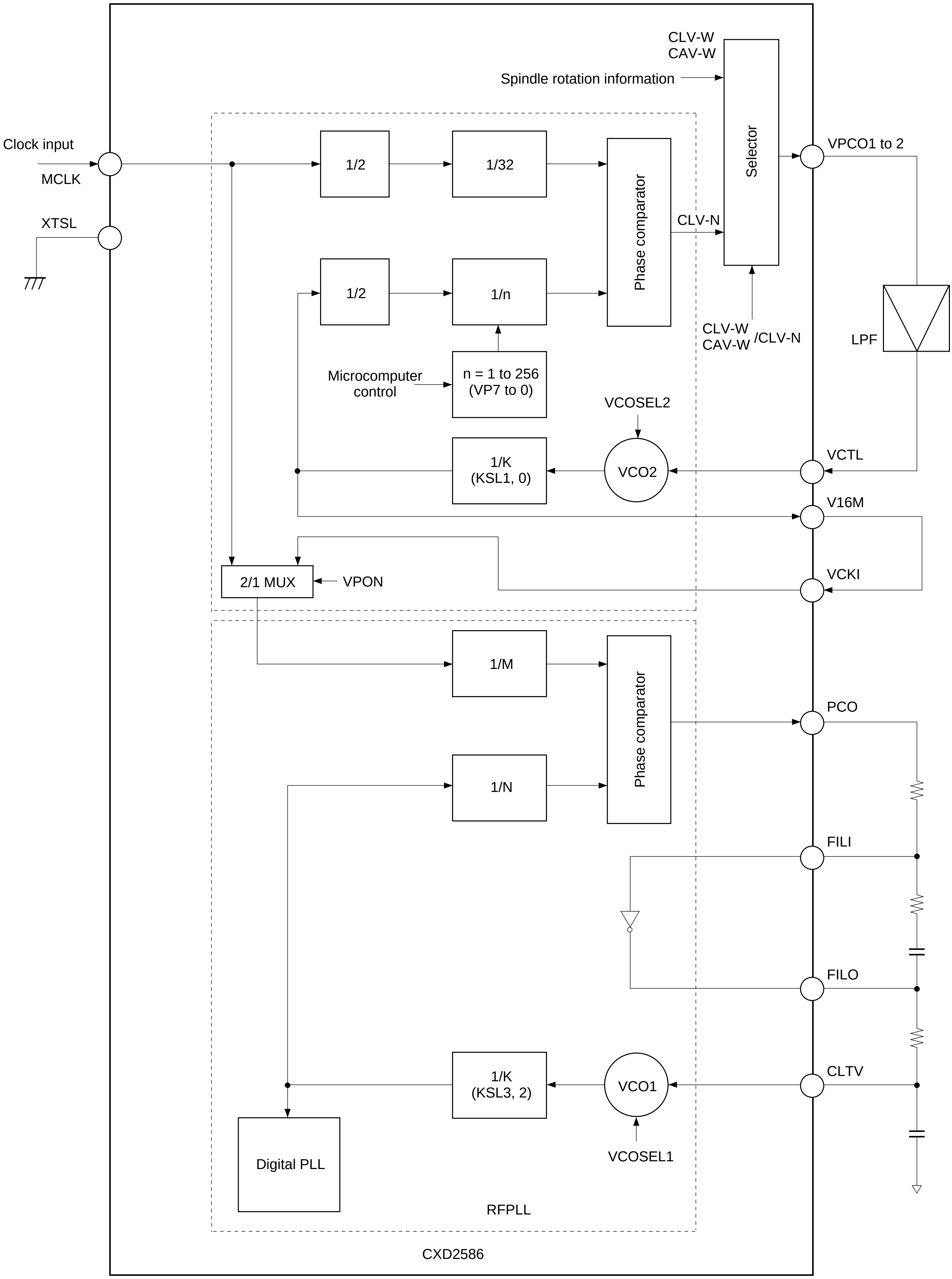
§4-1. Channel Clock Regeneration by the Digital PLL Circuit

- The channel clock is needed to demodulate the EFM signal regenerated by the optical system.
  Assuming T as the channel clock cycle, the EFM signal is modulated in an integer multiple of T from 3T to 11T. In order to read the information in the EFM signal, this integer value must be read correctly. As a result, T, that is the channel clock, is necessary.
  In an actual player, PLL is necessary to regenerate the channel clock because the fluctuation in the spindle rotation alters the width of the EFM signal pulses.
  Practically, PLL is necessary to regenerate the channel clock, because the EFM pulse width is altered by spindle rotation fluctuation.

The block diagram of this PLL is shown in Fig. 4-1.
The CXD2586R/-1 has a built-in three-stage PLL.

- The first-stage PLL is for the wide-band PLL. When the built-in VCO2 is used, LPF is required externally.
  When the built-in VCO2 is not used, LPF and VCO are required externally.
  The output of this first-stage PLL is used as a reference for all clocks within the LSI.
- The second-stage PLL generates a high-frequency clock needed by the third-stage digital PLL.
- The third-stage PLL is a digital PLL that regenerates the actual channel clock.
- The digital PLL in CLV-N mode has a secondary loop, which is the primary loop (phases) and the secondary loop (frequency). When FLFC = 1, the secondary loop can be turned off. High-frequency components such as 3T and 4T may contain deviations. In such a case, turning the secondary loop off yields better playability. However, in this case the capture range becomes ±50kHz.
- The new digital PLL in CLV-W mode follows the rotational velocity of the disc, in addition to the above-mentioned secondary loop.

Block Diagram 4-1



§4-2. Frame Sync Protection

- In normal speed playback, a frame sync is recorded approximately every 136µs (7.35kHz). This signal is used as a reference to recognize the data within a frame. Conversely, if the frame sync cannot be recognized, the data is processed as error data because the data cannot be recognized. As a result, recognizing the frame sync properly is extremely important for improving playability.

- In the CXD2586R/-1, window protection and forward protection/backward protection have been adopted for frame sync protection. These functions achieve very powerful frame sync protection. There are two window widths: one for cases where a rotational disturbance affects the player and the other for cases where there is no rotational disturbance (WSEL = 0/1). In addition, the forward protection counter is fixed to 13, and the backward protection counter to 3. Concretely, when the frame sync has been played back normally and then cannot be detected due to scratches, a maximum of 13 frames are inserted. If frame sync cannot be detected for 13 frames or more, the window is released and try to resyncronize the frame sync.
  In addition, immediately after the window is released and the resynchronization is executed, if a proper frame sync cannot be detected within 3 frames, the window is released immediately.

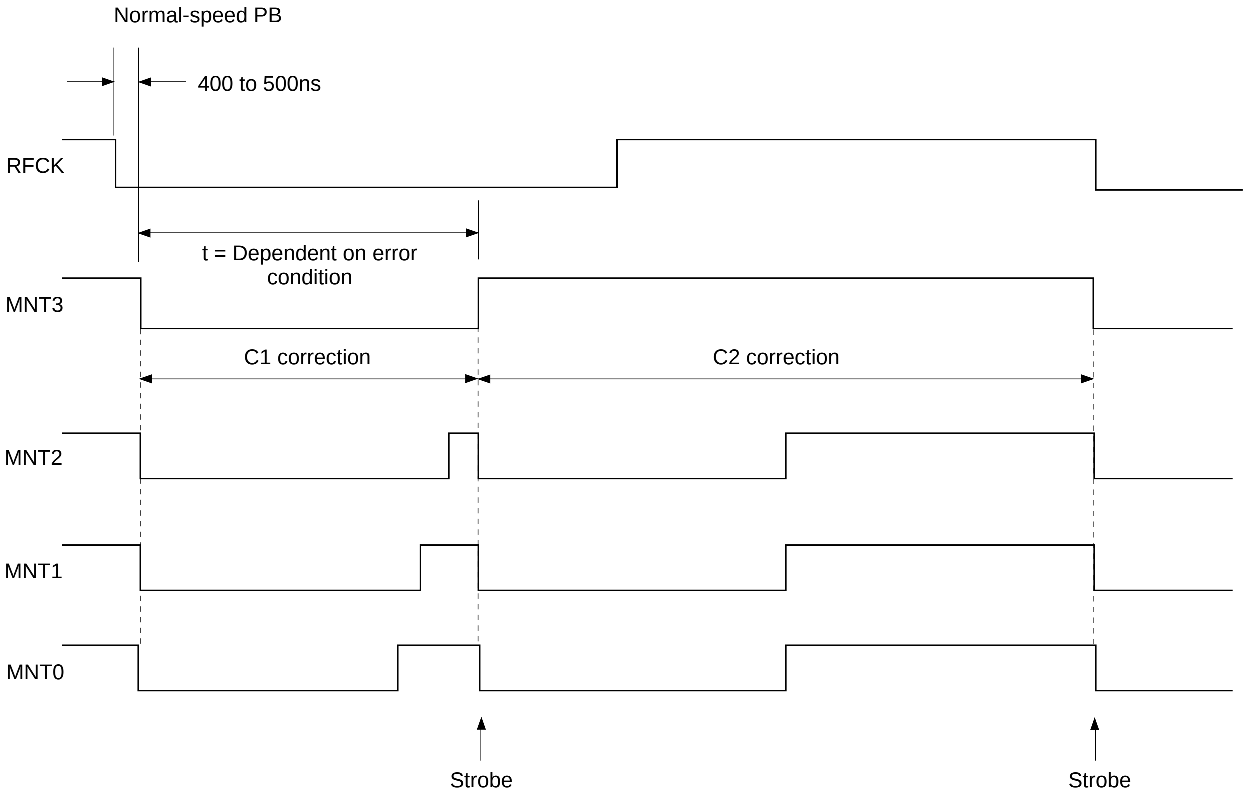
§4-3. Error Correction

- In the CD format, one 8-bit data contains two error correction codes, C1 and C2. For C1 correction, the code is created with 28-byte information and 4-byte C1 parity.
  For C2 correction, the code is created with 24-byte information and 4-byte parity.
  Both C1 and C2 are Reed Solomon codes with a minimum distance of 5.
- The CXD2586R/-1 uses refined super strategy to achieve double correction for C1 and quadruple correction for C2.
- In addition, to prevent C2 miscorrection, a C1 pointer is attached to data after C1 correction according to the C1 error status, the playback status of the EFM signal, and the operating status of the player.
- The correction status can be monitored externally.
  See the Table 4-2.
- When the C2 pointer is high, the data in question was uncorrectable. Either the pre-value was held or an average value interpolation was made for the data.

MNT3	MNT2	MNT1	MNT0	Description	
0	0	0	0	No C1 errors	; C1 pointer reset
0	0	0	1	One C1 error corrected	; C1 pointer reset
0	0	1	0	—	
0	0	1	1	—	
0	1	0	0	No C1 errors	; C1 pointer set
0	1	0	1	One C1 error corrected	; C1 pointer set
0	1	1	0	Two C1 errors corrected	; C1 pointer set
0	1	1	1	C1 correction impossible	; C1 pointer set
1	0	0	0	No C2 errors	; C2 pointer reset
1	0	0	1	One C2 error corrected	; C2 pointer reset
1	0	1	0	Two C2 errors corrected	; C2 pointer reset
1	0	1	1	Three C2 errors corrected	; C2 pointer reset
1	1	0	0	Four C2 errors corrected	; C2 pointer reset
1	1	0	1	—	
1	1	1	0	C2 correction impossible	; C1 pointer copy
1	1	1	1	C2 correction impossible	; C2 pointer set

Table 4-2.

Timing Chart 4-3



§4-4. DA Interface

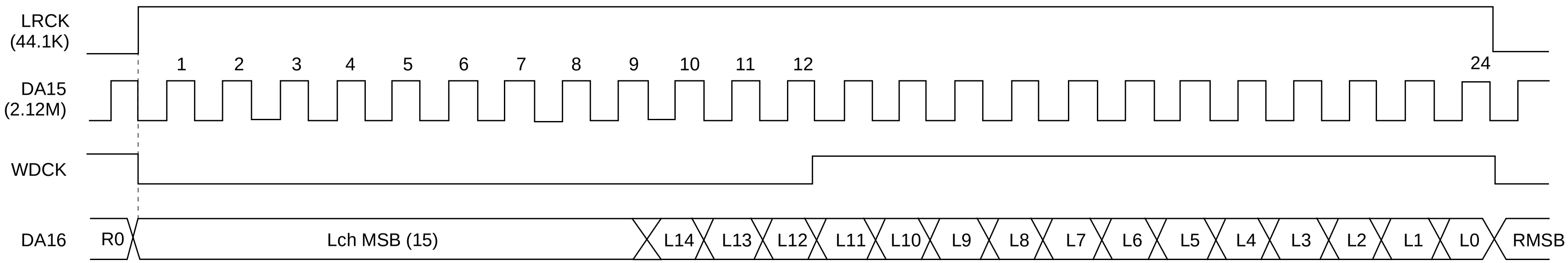
• The CXD2586R/-1 has two modes as DA interfaces.

a) 48-bit slot interface
This interface includes 48 cycles of the bit clock within one LRCK cycle, and is MSB first.
When LRCK is high, the data is for the left channel.

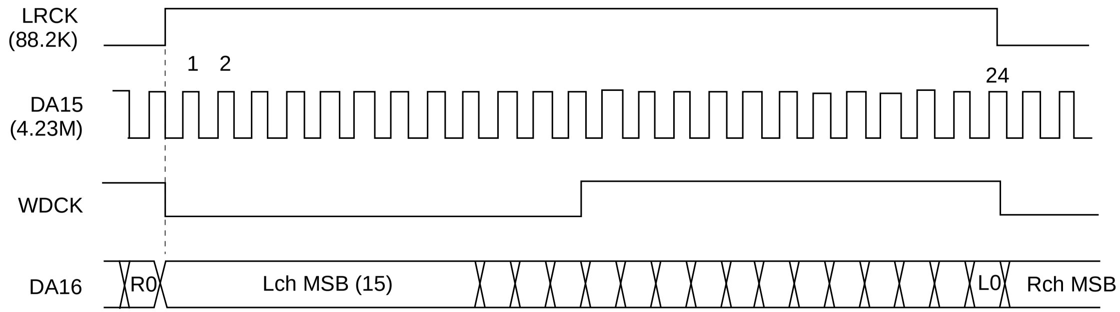
b) 64-bit slot interface
This interface includes 64 cycles of the bit clock within one LRCK cycle, and is LSB first.
When LRCK is low, the data is for the left channel.

Timing Chart 4-4

48bit slot Normal-Speed Playback PSSL = L

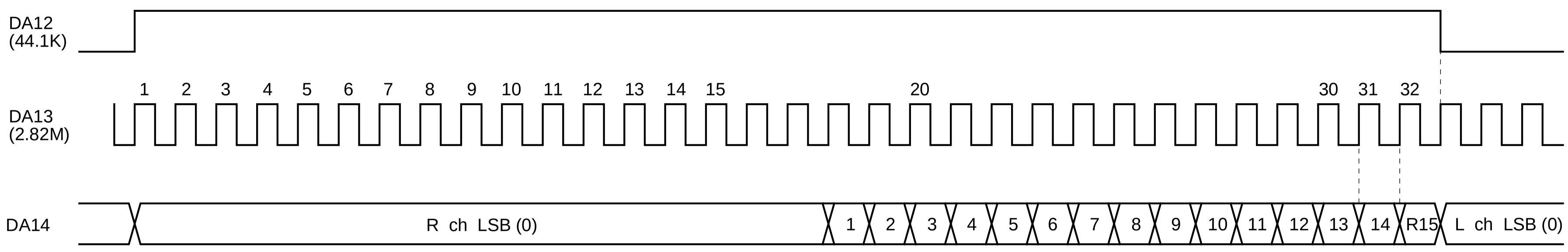


48bit slot Double-Speed Playback

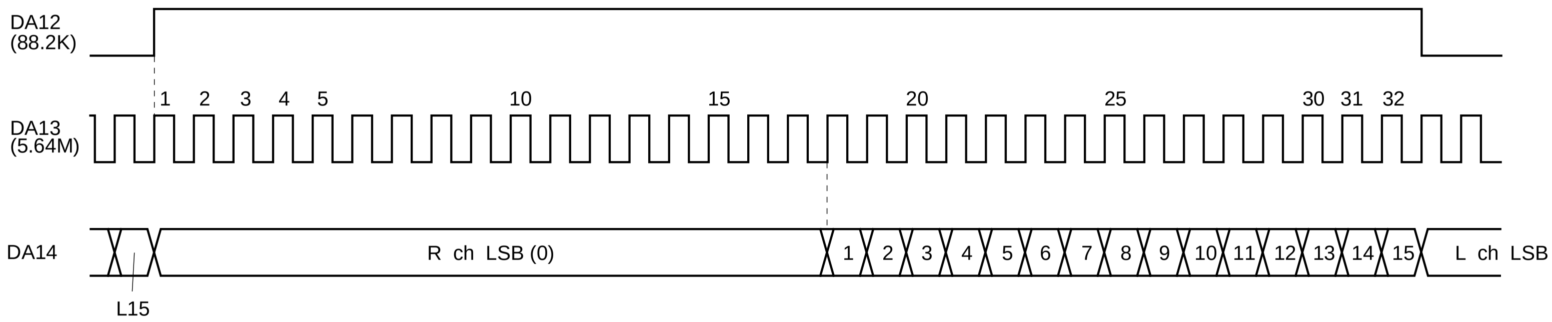


Timing Chart 4-5

64 Bit slot Normal Speed PB PSSL = L



64 Bit slot Double- Speed PB



§4-5. Digital Out

There are three digital output formats: the type 1 format for broadcasting stations, the type 2 form 1 format for home use, and the type 2 form 2 format for the manufacture of software.

The CDX2586R/-1 supports type 2 form 1.

In addition, regarding the clock accuracy of the channel status, level II is set for crystal clock use and level III for CAV-W mode. In addition, Sub Q data which are matched twice in succession after a CRC check are input to the first four bits (bits 0 to 3).

DOUT is output when the crystal is 34MHz and DSPB is set to 1 with XTSL high in CLV-N or CLV-W mode. Therefore, set MD2 to 0 and turn DOUT off.

Digital Out C bit

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	From sub Q: ID0	ID1	COPY	Emph	0	0	0	0	1	0	0	0	0	0	0	0
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0
32 – 176	0															

bit0 to 3 Sub Q control bits that matched twice with CRCOK

bit29 VPON: 1 Crystal: 0

Table 4-6.

§4-6. Servo Auto Sequence

This function performs a series of controls, including auto focus and track jumps. When the auto sequence command is received from the CPU, auto focus, 1 track jump, 2N track jumps, fine search, and M track move are executed automatically.
Servo is used in an exclusive manner during the auto sequence execution (when XBUSY = low), so that commands from the CPU are not transferred to the servo, but can be sent to the CXD2586R/-1.
In addition, when using the auto sequence, turn the A.SEQ of register 9 on.
When CLOK goes from low to high while XBUSY is low, XBUSY does not become high for a maximum of 100µs after that point. This is to prevent the transfer of erroneous data to the servo when XBUSY changes from low to high by the monostable multivibrator, which is reset by CLOK being low (when XBUSY is low).
In addition, a MAX timer is built in this LSI as a countermeasure against abnormal operation due to external disturbances, etc. When the auto sequence command is sent from the CPU, this command assumes a $4XY format, in which X specifies the command and Y sets the MAX timer value and timer range. If the executed auto sequence command does not terminate within the set timer value, the auto sequence is interrupted (like $40). See §1, $4X commands concerning the timer value and range. Also, the MAX timer is invalidated by inputting $4X0.
Although this command is explained in the format of $4X in the following command descriptions, the timer value and timer range are actually sent together from the CPU.

(a) Auto focus ($47)

Focus search-up is performed, FOK and FZC are checked, and the focus servo is turned on.
If $47 is received from the CPU, the focus servo is turned on according to Fig. 4-8. The auto focus starts with focus search-up, and note that the pickup should be lowered beforehand (focus search down). In addition, blind E of register 5 is used to eliminate FZC chattering. Concretely, the focus servo is turned on at the falling edge of FZC after FZC has been continuously high for a longer time than E.

(b) Track jump

1, 10, and 2N-track jumps are performed respectively. Always use this when focus, tracking and sled servo are on. Note that tracking gain-up and braking-on ($17) should be sent beforehand because they are not involved in this sequence.

• 1-track jump

When $48 ($49 for REV) is received from the CPU, a FWD (REV) 1-track jump is performed in accordance with Fig. 4-9. Set blind A and brake B with register 5.

• 10-track jump

When $4A ($4B for REV) is received from the CPU, a FWD (REV) 10-track jump is performed in accordance with Fig. 4-10. The principal difference from the 1-track jump is to kick the sled. In addition, after kicking the actuator, when 5 tracks have been counted through COUT, the brake is applied to the actuator. Then, when the actuator speed is found to have slowed up enough (determined by the COUT cycle becoming longer than the overflow C set in register 5), the tracking and sled servos are turned on.

• 2N-track jump

When $4C ($4D for REV) is received from the CPU, a FWD (REV) 2N-track jump is performed in accordance with Fig. 4-11. The track jump count "N" is set in register 7. Although N can be set to 2^{16} tracks, note that the setting is actually limited by the actuator. COUT is used for counting the number of jumps when N is less than 16, and MIRR is used when N is 16 or more.

Although the 2N-track jump basically follows the same sequence as the 10-track jump, the one difference is that after the tracking servo is turned on, the sled continues to move only for "D", set in register 6.

• Fine search

When $44 ($45 for REV) is received from the CPU, a FWD (REV) fine search (N-track jump) is performed in accordance with Fig. 4-12. The differences from a 2N-track jump are a higher precision jump achieved by controlling the traverse speed and a longer distance jump achieved by controlling the sled. The track jump count is set in register 7. N can be set to 2^{16} tracks. After kicking the actuator and sled, the traverse speed is controlled based on the overflow G. Set kick D and F in register 6 and overflow G in register 5. Also, sled speed control during traverse can be turned off by causing COMP to fall. Set the number of tracks during which COMP falls in register B. After N tracks have been counted through COUT, the brake is applied to the actuator and sled. (This is performed by turning on the tracking servo for the actuator, and by kicking the sled in the opposite direction during the time for kick D set in register 6.) Then, the tracking and sled servos are turned on. Set overflow G to the speed required to slow up just before the track jump terminates. (The speed should be such that it will come on-track when the tracking servo turns on at the termination of the track jump.) For example, set the target track count N-α for the traverse monitor counter which is set in register B, and COMP will be monitored. When the falling edge of this COMP is detected, overflow G can be reset.

• M track move

When $4E ($4F for REV) is received from the CPU, a FWD (REV) M track move is performed in accordance with Fig. 4-13. M can be set to 2^{16} tracks. COUT is used for counting the number of moves when M is less than 16, and MIRR is used when M is 16 or more. The M track move is executed only by moving the sled, and is therefore suited for moving across several thousand to several ten-thousand tracks. In addition, the track and sled servo are turned off after M tracks have been counted through COUT or MIRR unlike for the other jumps. Transfer $25 after the actuator is stabled.

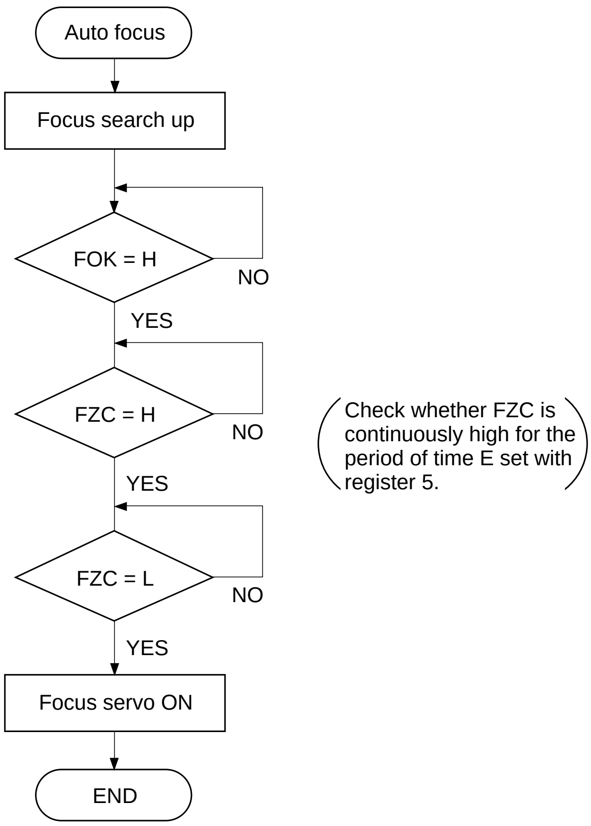


Fig. 4-8 (a). Auto Focus Flow Chart

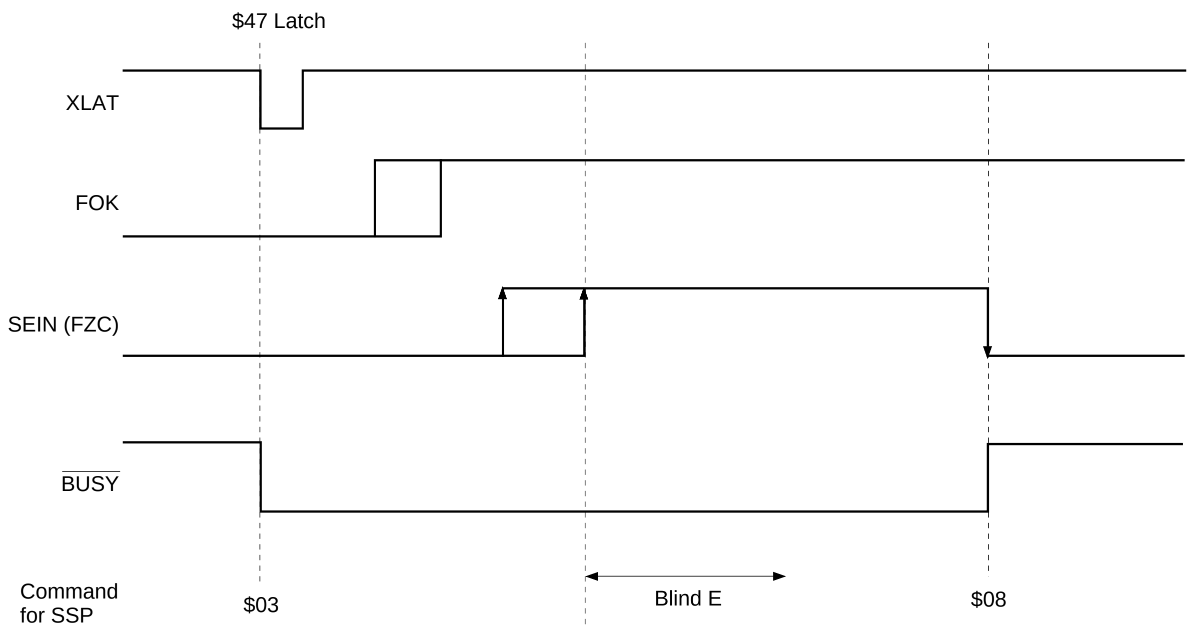


Fig. 4-8 (b). Auto Focus Timing Chart

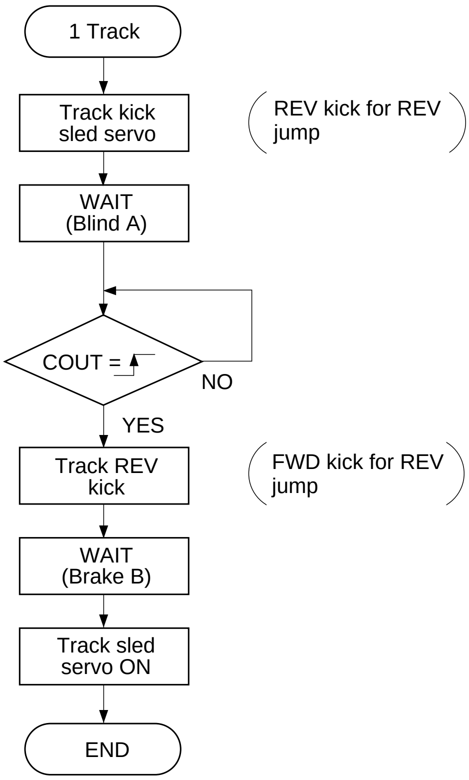


Fig. 4-9 (a). 1-Track Jump Flow Chart

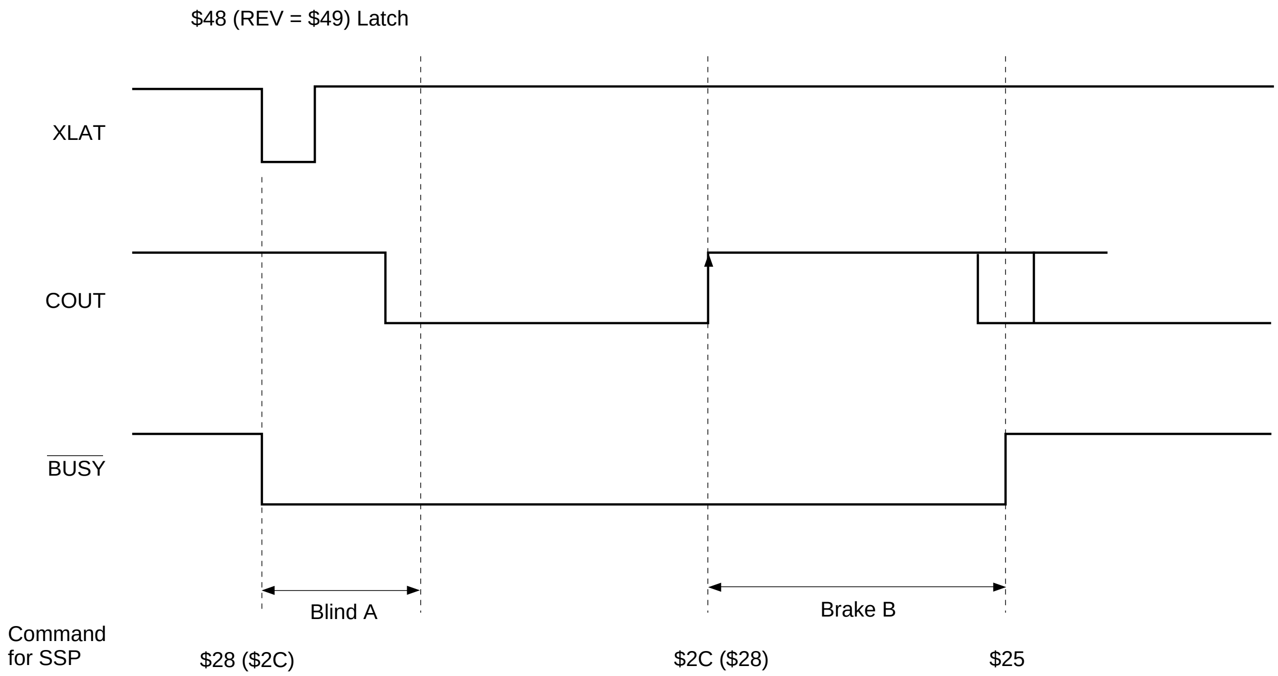


Fig. 4-9 (b). 1-Track Jump Timing Chart

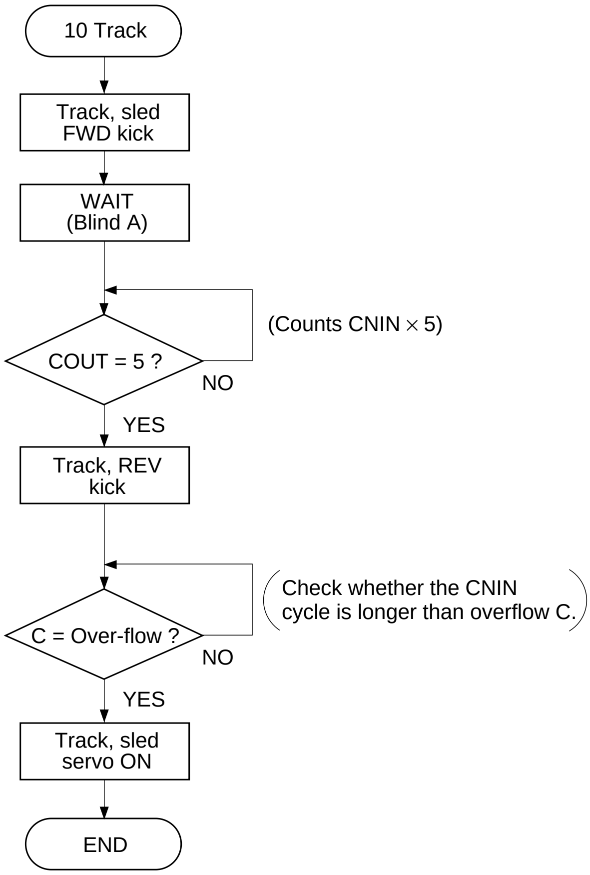


Fig. 4-10 (a). 10-Track Jump Flow Chart

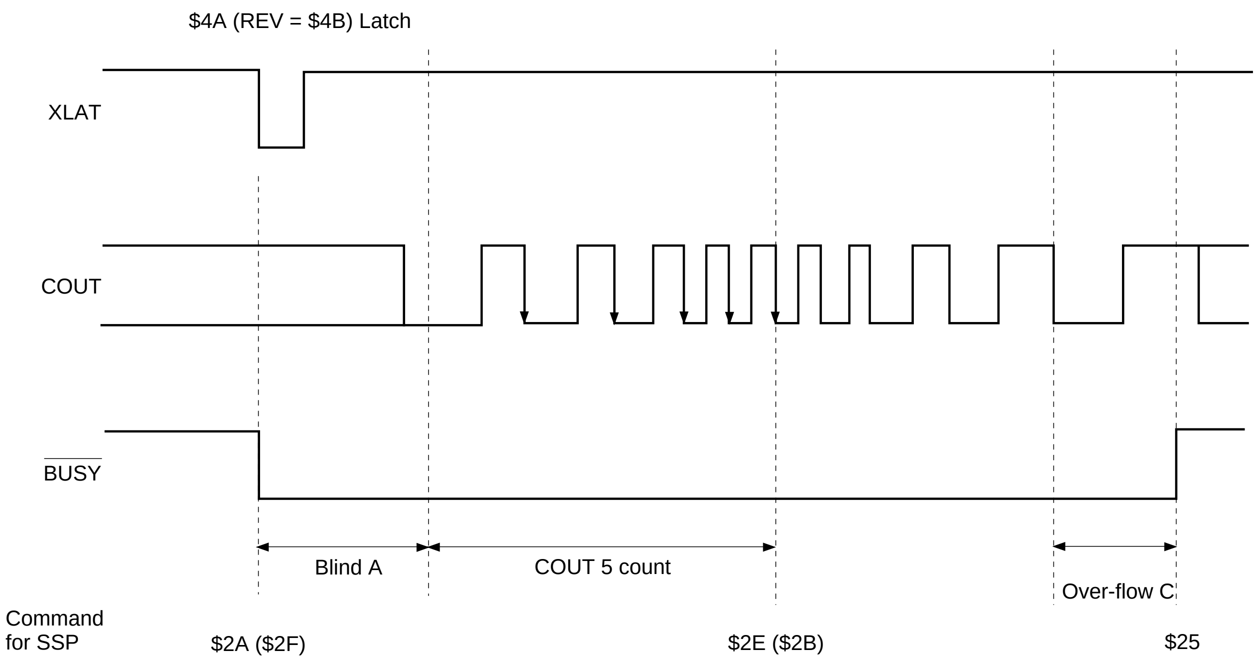


Fig. 4-10 (b). 10-Track Jump Timing Chart

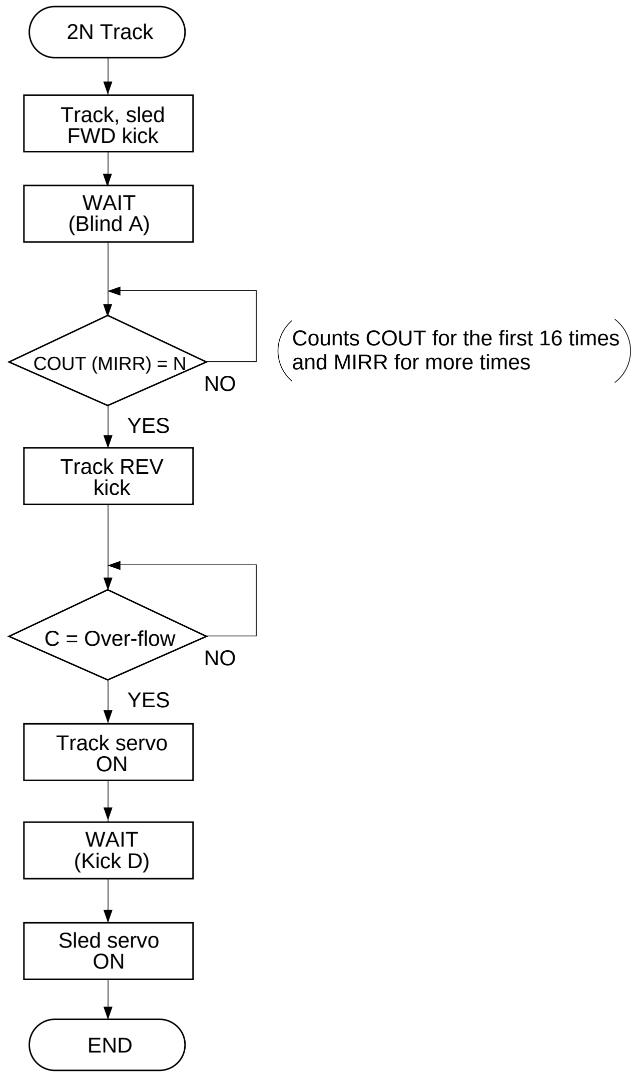


Fig. 4-11 (a). 2N-Track Jump Flow Chart

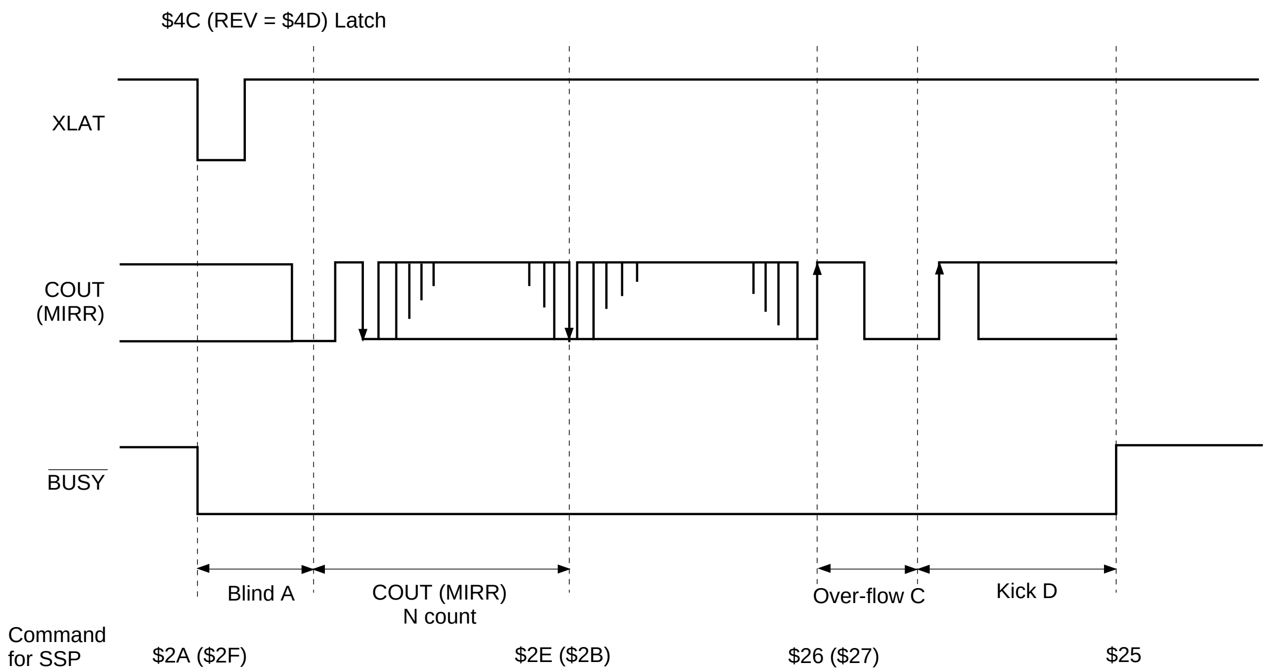


Fig. 4-11 (b). 2N Track Jump Timing Chart

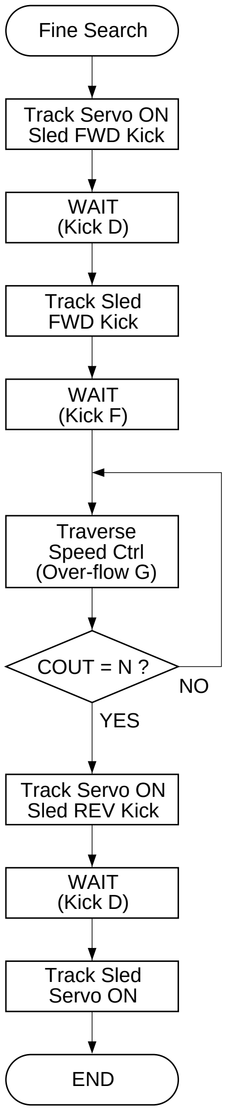


Fig. 4-12 (a). Fine Search Flow Chart

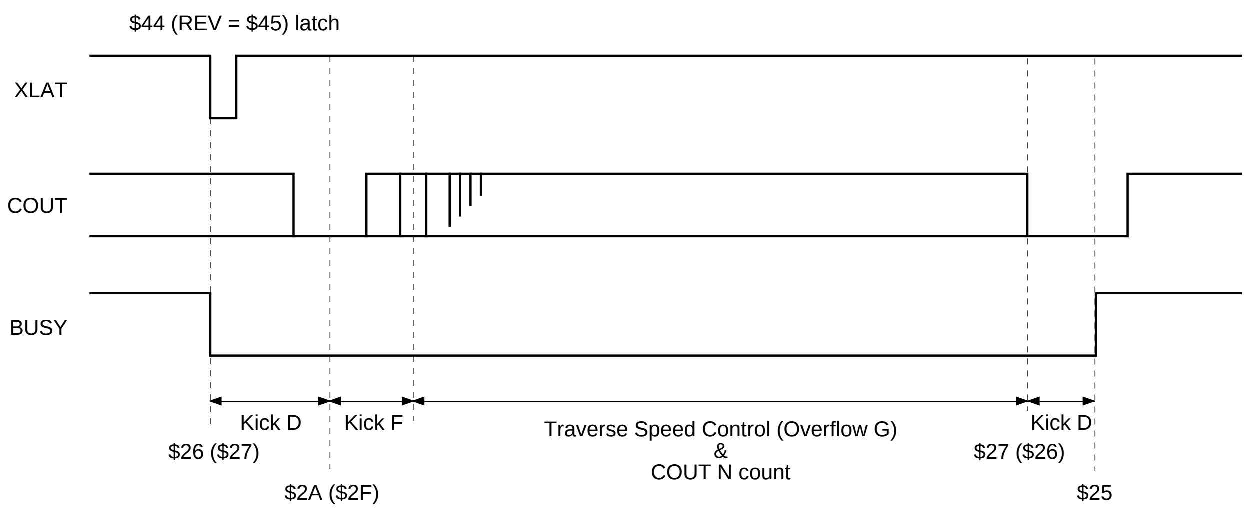


Fig. 4-12 (b). Fine Search Timing Chart

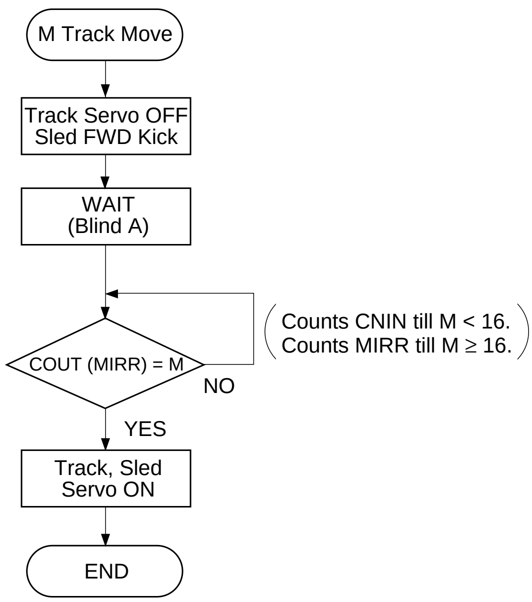


Fig. 4-13 (a). M-Track Move Flow Chart

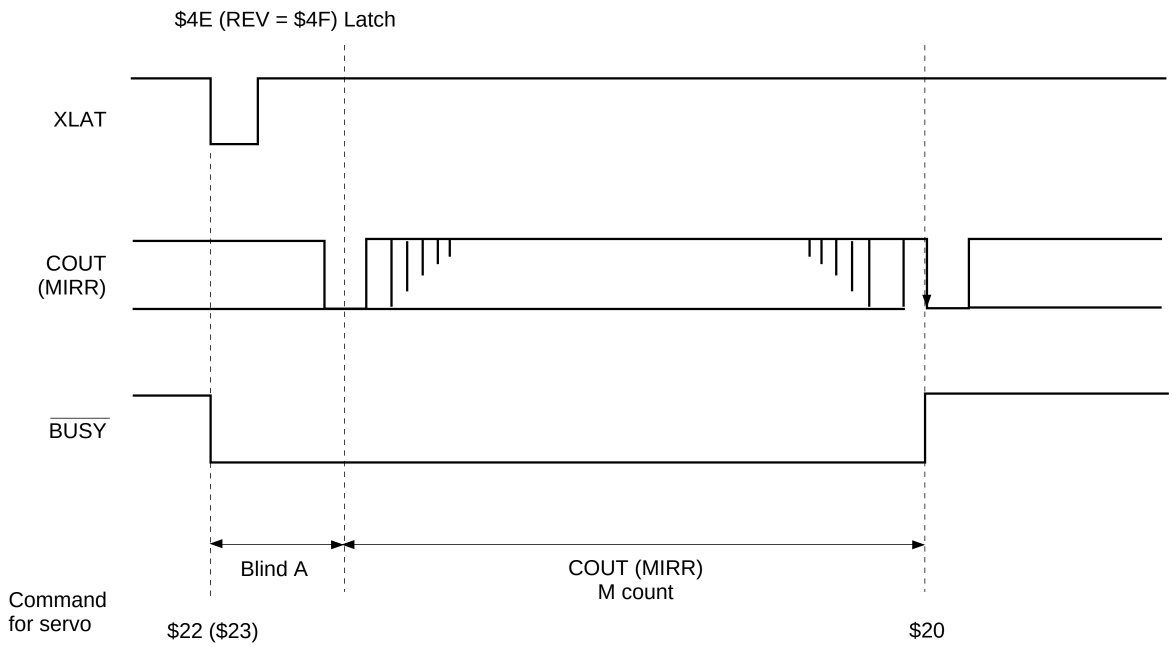
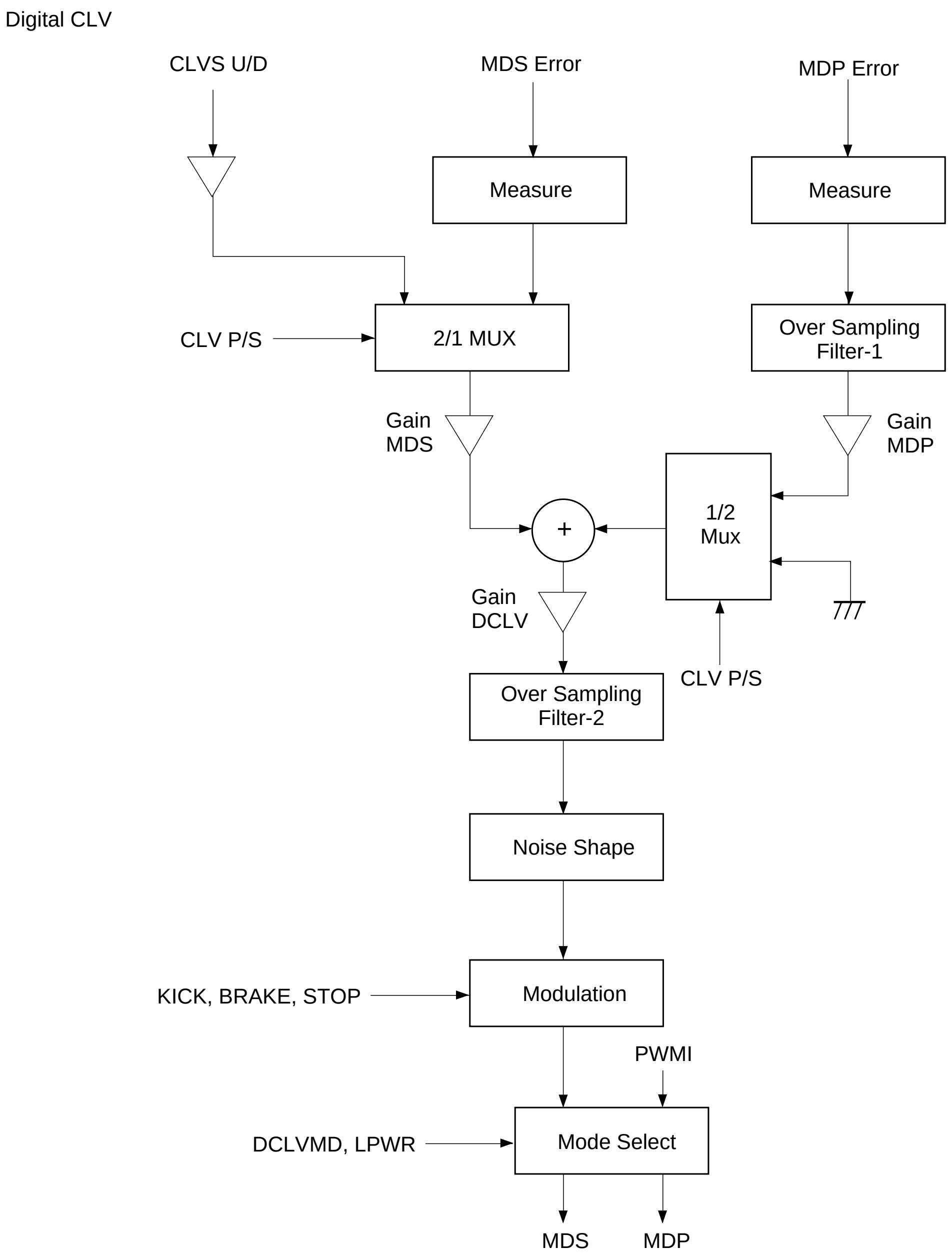


Fig. 4-13 (b). M-Track Move Timing Chart

§4-7. Digital CLV

Fig. 4-14 shows the block diagram. Digital CLV outputs MDS error and MDP error with PWM, sampling frequency is 130Hz at most during normal-speed playback in CLVS, CLVP and other modes.
In addition, the digital spindle servo gain is variable.



CLVS U/D: Up/down signal from CLVS servo
MDS error: Frequency error for CLVP servo
MDP error: Phase error for CLVP servo
PWMI: Spindle drive signal from the microcomputer

Fig. 4-14. Block Diagram

§4-8. Playback Speed

In the CXD2586R/-1, the following playback modes can be selected through different combinations of MCLK, XTSL pin, double-speed command (DSPB), VCO1 selection command (VCOSEL1), VCO1 frequency dividing command (KSL3, KSL2) and command transfer rate selector (ASHS) in CLV-N or CLV-W mode.

• **For the CXD2586R/-1**

Mode	MCLK	XTSL	DSPB	VCOSEL1*1	ASHS	Playback speed	Error correction
1	1152Fs	1	0	0/1	1	× 1.5	C1: double; C2: quadruple
2	1152Fs	1	1	1	1	× 3	C1: double; C2: double
3	1152Fs	0	0	1	*2	× 3	C1: double; C2: quadruple
4	1152Fs	0	1	1	*2	× 6	C1: double; C2: double
5	768Fs	1	0	0/1	0	× 1	C1: double; C2: quadruple
6	768Fs	1	1	0/1	0	× 2	C1: double; C2: double
7	768Fs	0	0	1	1	× 2	C1: double; C2: quadruple
8	768Fs	0	1	1	1	× 4	C1: double; C2: double
9	384Fs	0	0	0/1	0	× 1	C1: double; C2: quadruple
10	384Fs	0	1	0/1	0	× 2	C1: double; C2: double
11	384Fs	1	1	0/1	0	× 1	C1: double; C2: double

*1 Actually, use the optimal value by combining KSL3 with KSL2.
*2 The built-in auto sequencer can not be used.

The playback speed can be varied by setting VP0 to 7 in CAV-W mode. See "§3. Description of Modes" for details.

§4-9. DAC Block Playback Conditions

• The DAC block playback speed is controlled by sending the DADS command to the DSP block.

Mode	X'tal	DADS
1	768fs	0
2	384fs	1

§4-10. DAC Block Input Timing

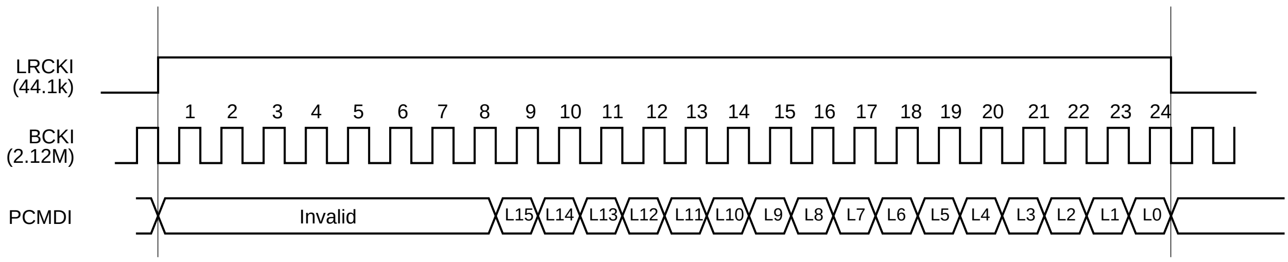
The timing charts for input to the DAC are shown below.

In the CXD2586R/-1, audio data is not sent from the CD signal processor block to the DAC block inside the LSI. The reason why is to allow data to be passed through an audio DSP, etc., on its way to the DAC block. To input data to the DAC block without passing it through an audio DSP, etc., the data connection must be made externally.

In this case, LRCK, BCK, and PCMD can be connected directly to LRCKI, BCKI, and PCMDI.

(See the Application Circuit.)

Normal-speed Playback



LPF Block

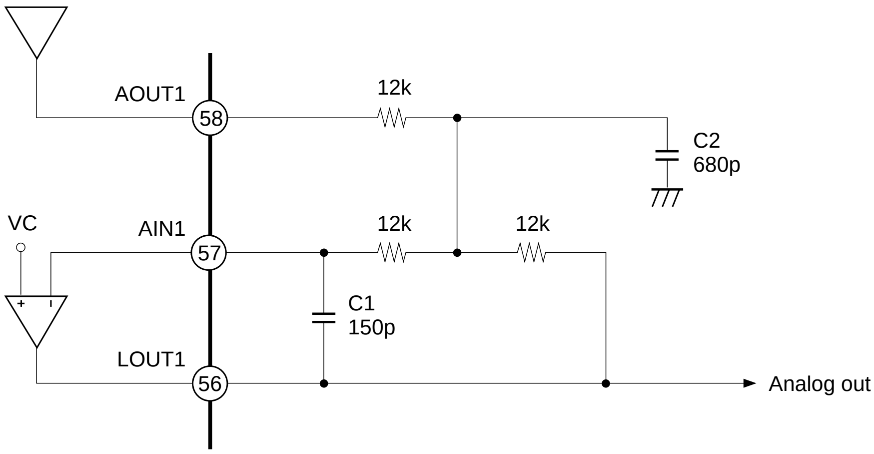
The CXD2586R/-1 contains an initial-stage secondary active LPF with numerous resistors and capacitors and an operational amplifier with reference voltage.
The resistors and capacitors are attached externally, allowing the cut-off frequency fc to be determined flexibly.
The reference voltage (VC) is $(AV_{DD} – AV_{SS})/2$.

The LPF block application circuit is shown below.
In this circuit, the cut-off frequency is fc ≈ 40kHz.

The capacitance of the external capacitors when fc = 30kHz and 50kHz are noted below as a reference.

- When fc ≈ 30kHz:
  C1 = 200pF, C2 = 910pF
- When fc ≈ 50kHz:
  C1 = 120pF, C2 = 560pF

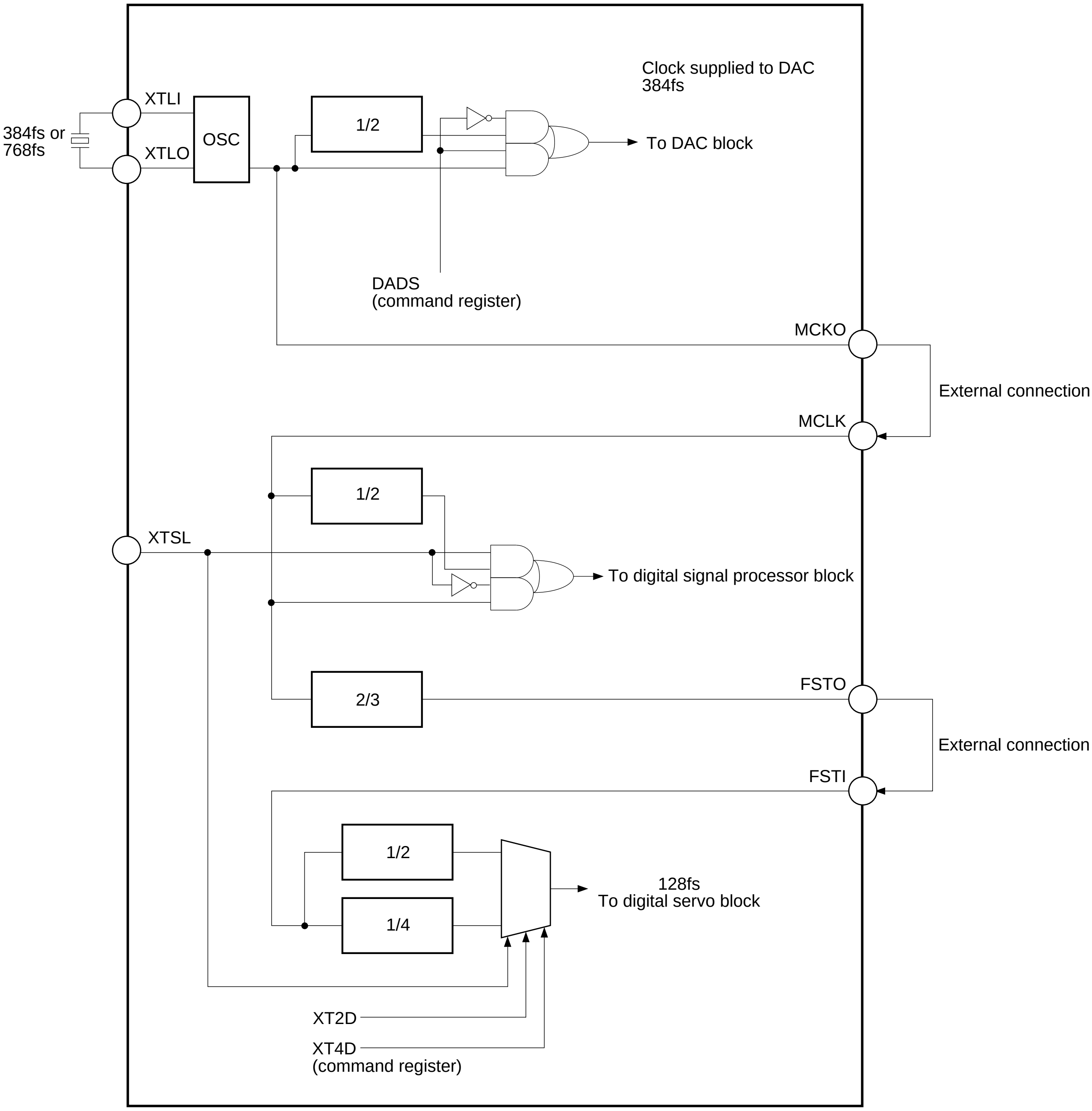
LPF Block Application Circuit



LPF external circuit

§4-11. CXD2586R/-1 Clock System

The DAC, digital signal processor and digital servo blocks can be switched to each playback mode according to how the crystal and clock circuit are connected. Each circuit is as shown in the diagram below; during normal use, MCKO and MCLK are directly connected to each other, and FSTO and FSTI are directly connected to each other.



[5] Description of Servo Signal Processing-System Functions and Commands

§5-1. General Description of the Servo Signal Processing System (Voltages are the values for a 5V power supply.)

Focus servo

Sampling rate:	88.2kHz
Input range:	2.5V center ±1.0V
Output format:	7-bit PWM
Others:	Offset cancel
	Focus bias adjustment
	Focus search
	Gain-down function
	Defect countermeasure
	Automatic gain control

Tracking servo

Sampling rate:	88.2kHz
Input range:	2.5V center ±1.0V
Output format:	7-bit PWM
Others:	Offset cancel
	E:F balance adjustment
	Track jump
	Gain-up function
	Defect countermeasure
	Drive cancel
	Automatic gain control
	Vibration countermeasure

Sled servo

Sampling rate:	345Hz
Input range:	2.5V center ±1.0V
Output format:	7-bit PWM
Others:	Sled move

FOK, MIRR, DFCT signals generation

RF signal sampling rate:	1.4MHz
Input range:	2.15V to 5.0V
Others:	RF zero level automatic measurement
	The signal input from the RFDC pin is multiplied by a factor of 0.7 and loaded into the A/D converter.

§5-2. Digital Servo Block Master Clock (MCK)

The FSTI pin is the reference clock input pin. The internal master clock (MCK) is generated by dividing the frequency of the signal input to FSTI. The frequency division ratio is 1/2 or 1/4.

Table 3-1 below shows the hypothetical case where the crystal clock generated from the digital signal processor block is 2/3 frequency-divided and input to the FSTI pin by externally connecting the FSTI pin and the FSTO pin.

The XT4D and XT2D command settings can be made with D13 and D12 of $3F. (Default = 0)

The digital servo block is designed with an MCK frequency of 5.6448MHz.

Mode	MCLK	FSTO	FSTI	XTSL	XT4D	XT2D	Frequency division ratio	MCK frequency
1	384Fs	256Fs	256Fs	∗	0	1	1/2	128Fs
2	384Fs	256Fs	256Fs	0	0	0	1/2	128Fs
3	768Fs	512Fs	512Fs	∗	1	0	1/4	128Fs
4	768Fs	512Fs	512Fs	1	0	0	1/4	128Fs

Fs = 44.1kHz, ∗: Don't care

Table 5-1.

§5-3. AVRG (Average) Measurement and Compensation

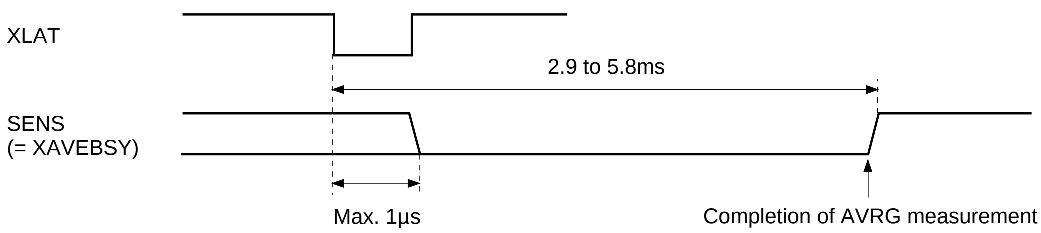
The CXD2586R/-1 has a circuit that measures AVRG of RFDC, VC, FE, and TE and a circuit that compensates them to control servo effectively.

AVRG measurement and compensation is necessary to initialize the CXD2586R/-1, and is able to cancel the offset by performing each AVRG measurement before playback operation and using these results for compensation. The level applied to the VC, FE RFDC and TE pins can be measured by setting D15 (VCLM), D13 (FLM), D11 (RFLM) and D4 (TCLM) of $38 respectively to 1.

AVRG measurement consists of digitally measuring the level applied to each analog input pin by taking the average of 256 samples, and then loading these values into the AVRG register.

AVRG measurement requires approximately 2.9ms to 5.8ms after the command is received.

During AVRG measurement, if the upper 8 bits of the serial command are 38 (Hex), the completion of AVRG measurement operation can be confirmed through the SENS pin. (See the Timing Chart 5-2.)



Timing Chart 5-2.

<Measurement>

- VC AVRG
  The offset can be canceled by measuring the VC level which is the center voltage for the system and using that value to apply compensation to each input error signal.

- FE AVRG
  CXD2586R/-1 measures the FE signal DC level, and can apply it to compensate the FZC comparator level output from the SENS pin during FCS SEARCH (focus search) using these measurement results.

- TE AVRG
  This measures the TE signal DC level.

- RE AVRG
  The CXD2586R/-1 generates the MIRR, DFCT and FOK signals from the RF signal. However, the FOK signal is generated by comparing the RF signal at a certain level, so that it is necessary to establish a zero level which becomes the comparator level reference. Therefore, the RF signal is measured before playback operation, and compensation is applied to bring this level to the zero level.

An example of sending AVRG measurement and compensation commands is shown below.
(Example) $380800 (RF Avrg. measurement on)
$382000 (FE Avrg. measurement on)
$380010 (TE Avrg. measurement on)
$388000 (VC Avrg. measurement on)
(Complete each AVRG measurement before starting the next.)
$38140A (RFLC, FLC0, FLC1 and TLC1 commands on)
(The required compensation should be turn on together; see Fig. 5-3.)
An interval of 5.8ms or more must be maintained between each command, or the SENS pin must be monitored to confirm that the previous command has been completed before the next AVRG command is sent.

<Compensation>

See Fig. 5-3 for the contents of each compensation below.

- RFLC
  The difference by which the RF signal exceeds the RF AVRG value is input to the RF In register.
  (00 is input when the RF signal is lower than the RF AVRG value.)
- TCL0
  The value obtained by subtracting the VC AVRG value from the TE signal is input to the TRK In register.
- TCL1
  The value obtained by subtracting the TE AVRG value from the TE signal is input to the TRK In register.
- VCLC
  The value obtained by subtracting the VC AVRG value from the FE signal is input to the FCS In register.
- FLC1
  The value obtained by subtracting the FE AVRG value from the FE signal is input to the FCS In register.
- FLC0
  The value obtained by subtracting the FE AVRG value from the FE signal is input to the FZC register.

§5-4. E:F Balance Adjustment Function

When the disc is rotated with the laser on, and with the FCS (focus) servo on via FCS Search (focus search), the traverse waveform appears in the TE signal due to disc eccentricity.

In this condition, the low-frequency component can be extracted from the TE signal using the built-in TRK hold filter by setting D5 (TBLM) of $38 to 1.

The extracted low-frequency component is loaded into the TRVSC register as a digital value, and the TRVSC register value is established when TBLM returns to 0.

Next, setting D2 (TLC2) of $38 to 1 applies only the amount of compensation (subtraction) equal to the TRVSC register value to the values obtained from the TE and SE input pins, enabling the E:F balance offset to be adjusted. (See Fig. 5-3.)

§5-5. FCS Bias (Focus Bias) Adjustment Function

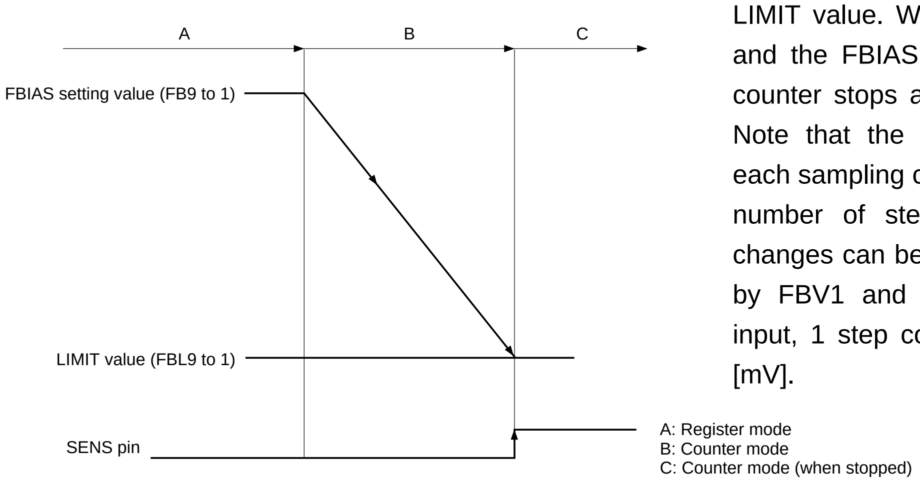
The FBIAS register value can be added to the FCS servo filter input by setting D14 (FBON) of $3A to 1. (See Fig. 3-3.)

When the FBIAS register value is set to D11 = 0 and D10 = 1 by $34F, data can be written using the 9-bit value of D9 to D1 (D9: MSB).

In addition, the RF jitter can be monitored by setting the SCOT command of $8 to 1. (See the DSP Block Timing Chart.)

The FBIAS register can be used as a counter by setting D13 (FBSS) of $3A to 1. It works as an up/down counter. The FBIAS register works as an up counter when D12 (FBUP) of $3A = 1, and as a down counter when D12 (FBUP) of $3A = 0. The number of up and down steps can be changed by setting D11 and 10 (FBV1 and FBV0) of $3A.

When using the FBIAS register as a counter, the counter stops when the value set beforehand in FBL9 to 1 of $34 matches the FCSBIAS value. Also, if the upper 8 bits of the serial command are $3A at this time, the counter stop can be monitored through SENS.



Here, the FBIAS setting values FB9 to 1 and the FBIAS LIMIT values FBL9 to 1 are assumed to be set in status A. For example, if command registers FBUP = 0, FBV1 = 0, FBV0 = 0 and FBSS = 1 are set from this status, down count starts from status A and approaches the set LIMIT value. When the LIMIT value is reached and the FBIAS value matches FBL9 to 1, the counter stops and the SENS pin goes to high. Note that the up/down counter changes with each sampling cycle of the focus servo filter. The number of steps by which the count value changes can be selected from 1, 2, 4 or 8 steps by FBV1 and FBV0. When converted to FE input, 1 step corresponds to approximately 3.9 [mV].

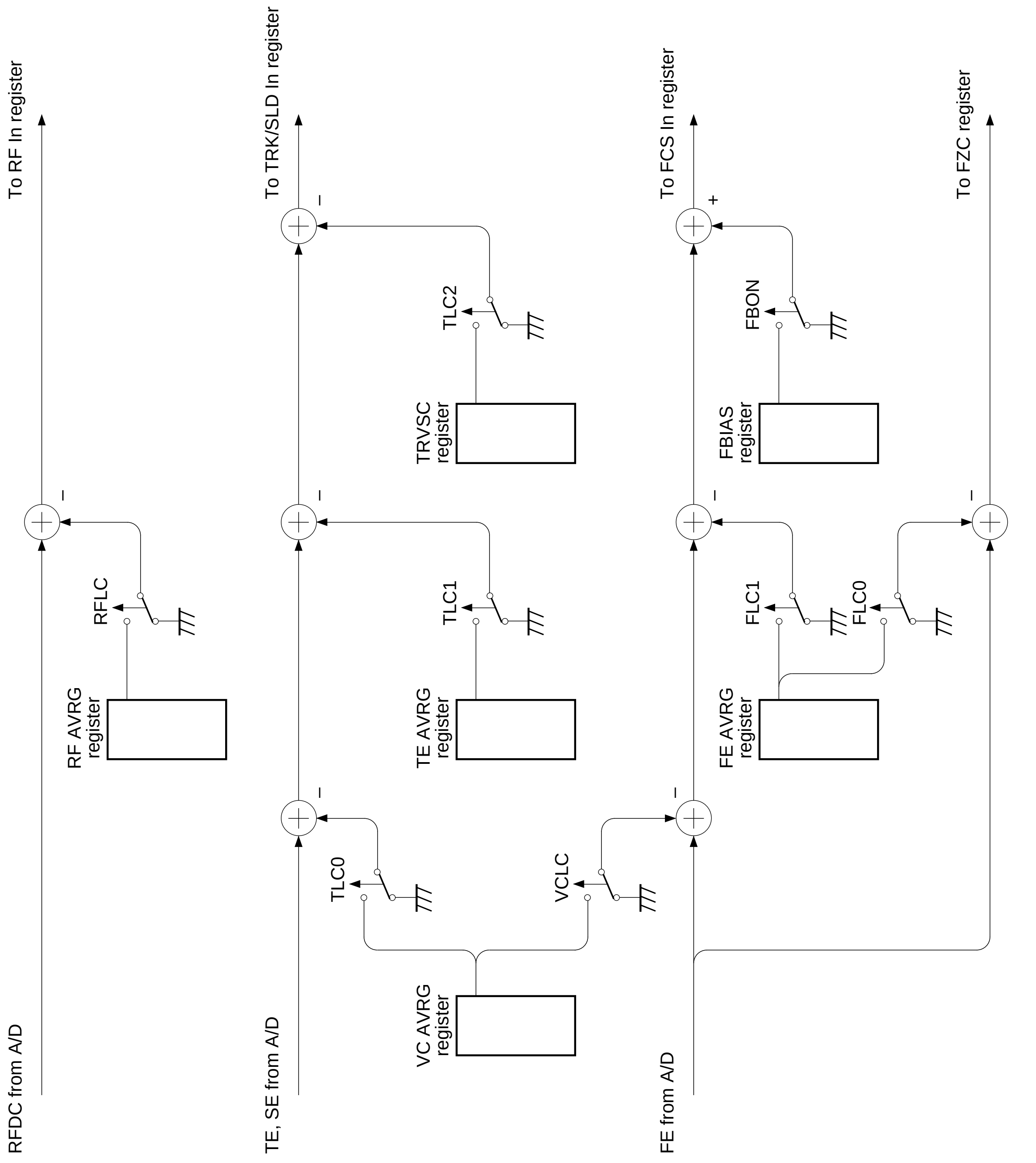
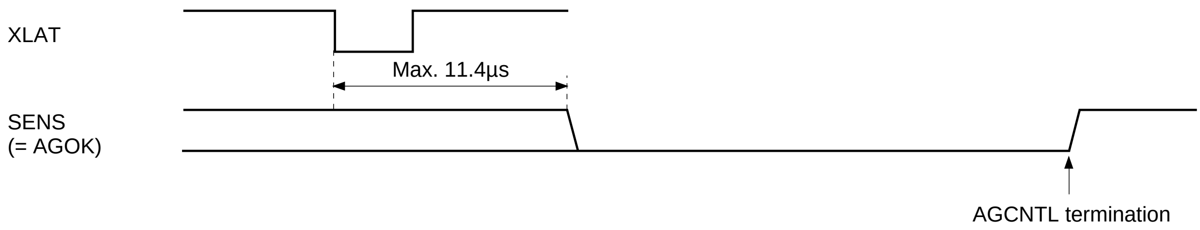

To RF In register
To TRK/SLD In register
To FCS In register
To FZC register
RFDC from A/D
TE, SE from A/D
FE from A/D
RF AVRG register
RFLC
TE AVRG register
TLC1
TRVSC register
TLC2
VC AVRG register
TLC0
VCLC
FE AVRG register
FLC1
FLC0
FBIAS register
FBON
–
+

Fig. 5-3.

§5-6. AGCNTL (Automatic Gain Control) Function

The AGCNTL function automatically adjusts the filter internal gain in order to obtain the appropriate gain with the servo loop. AGCNTL not only copes with the sensitivity variation of the actuator and photo diode, etc., but also obtains the optimal gain for each disc.
The AGCNTL command is sent when each servo is turned on. During AGCNTL operation, if the upper 8 bits of the serial command are 38 (Hex), the completion of AGCNTL operation can be confirmed through the SENS pin. (See the Timing Chart 5-4 and the Description of SENS Signals.)
Setting D9 and D8 of $38 to 1 set FCS (focus) and TRK (tracking) respectively to AGCNTL operation.

Note) During AGCNTL operation, each servo filter gain must be normal, and the anti-shock circuit (described hereafter) must be disabled.



Timing Chart 5-4.

Coefficient K13 changes for AGF (focus AGCNTL) and coefficients K23 and K07 changes for AGT (tracking AGCNTL) due to AGCNTL.
These coefficients change from 01 to 7F (Hex), and they must also be set within this range when written externally.
After AGCNTL operation has terminated, these coefficient values can be confirmed by reading them out from the SENS pin with the serial readout function (described hereafter).

AGCNTL related setting

The following settings can be changed with $35, $36 and $37.

FG6 to FG0;	AGF convergence gain setting, effective setting range: 00 to 57 (Hex)
TG6 to TG0;	AGT convergence gain setting, effective setting range: 00 to 57 (Hex)
AGS;	Self-stop on/off
AGJ;	Convergence completion judgment time
AGGF;	Internally generated sine wave amplitude (AGF)
AGGT;	Internally generated sine wave amplitude (AGT)
AGV1;	AGCNTL sensitivity 1 (during high sensitivity adjustment)
AGV2;	AGCNTL sensitivity 2 (during low sensitivity adjustment)
AGHS;	High sensitivity adjustment on/off
AGHT;	High sensitivity adjustment time

Note) Converging servo loop gain values can be changed with the FG6 to 0 and TG6 to 0 setting values. In addition, these setting values must be within the effective setting range. The default settings aim for 0dB at 1kHz. However, since convergence values vary according to the characteristics of each constituent element of the servo loop, FG and TG values should be set as necessary.

AGCNTL and default operation have two stages.
In the first stage, high sensitivity adjustment is performed for a certain period of time (select 256/128ms with AGHT), and the AGCNTL coefficient approaches the appropriate value roughly. The sensitivity at this time can be selected from two types with AGV1.
In the second stage, the AGCNTL coefficient approaches the appropriate value finely with relatively low sensitivity. The sensitivity for the second stage can be selected from two types with AGV2. In the second stage of default operation, when the AGCNTL coefficient reaches the appropriate value and stops changing, the CXD2586R/-1 confirms that the AGCNTL coefficient has not changed for a certain period of time (select 63/31ms with AGHJ), and then terminates AGCNTL operation. (Self-stop mode)
This self-stop mode can be canceled by setting AGS to 0.
In addition, the first stage is omitted for AGCNTL operation when AGHS is set to 0.
An example of AGCNTL coefficient transitions during AGCNTL operation and the relationship between the various settings are shown in Fig. 5-5.

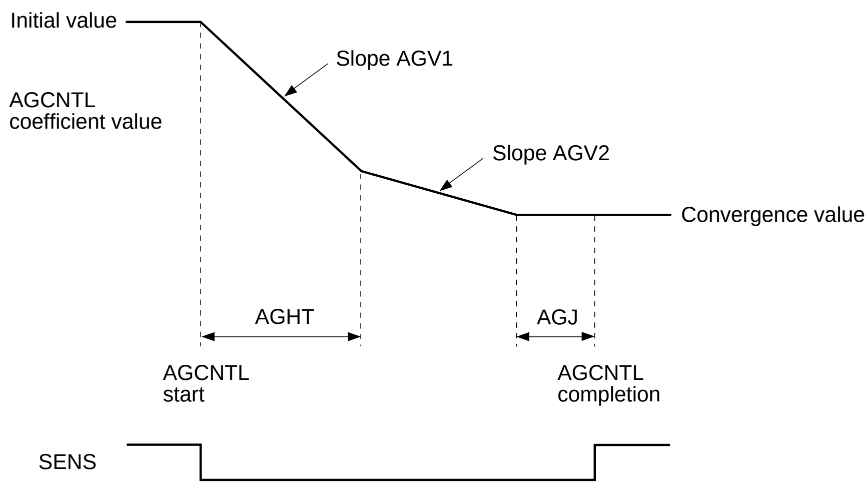


Fig. 5-5.

§5-7. FCS Servo and FCS Search (Focus Search)

The FCS servo is controlled by the 8-bit serial command $0X. (See Table 5-6.)

Register name	Command	D23 to D20	D19 to D16	
0	FOCUS CONTROL	0 0 0 0	1 0 ∗ ∗	FOCUS SERVO ON (FOCUS GAIN NORMAL)
			1 1 ∗ ∗	FOCUS SERVO ON (FOCUS GAIN DOWN)
			0 ∗ 0 ∗	FOCUS SERVO OFF, 0V OUT
			0 ∗ 1 ∗	FOCUS SERVO OFF, FOCUS SEARCH VOLTAGE OUT
			0 ∗ 1 0	FOCUS SEARCH VOLTAGE DOWN
			0 ∗ 1 1	FOCUS SEARCH VOLTAGE UP

∗: Don't care

Table 5-6.

FCS Search

FCS search is required in the course of turning on the FCS servo.

Fig. 5-7 shows the signals for sending commands $00 → $02 → $03 and performing only FCS search.
Fig. 5-8 shows the signals for sending $08 (FCS on) after that.

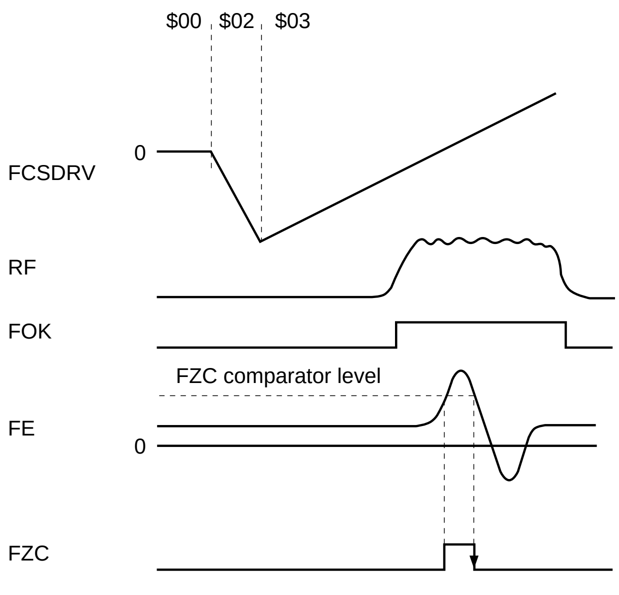


Fig. 5-7.

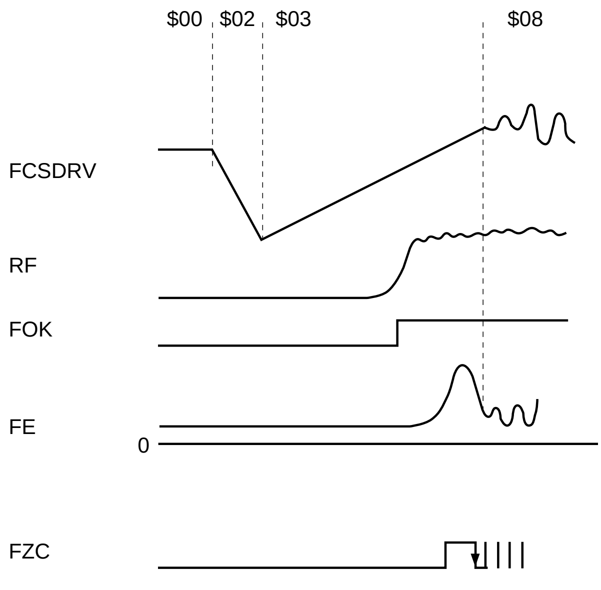


Fig. 5-8.

§5-8. TRK (Tracking) and SLD (Sled) Servo Control

TRK and SLD servo is controlled by the 8-bit command $2X. (See Table 5-9.)
When the upper 4 bits of the serial command are 2 (Hex), TZC is output from the SENS pin.

Register name	Command	D23 to D20	D19 to D16	
2	TRACKING MODE	0 0 1 0	0 0 * *	TRACKING SERVO OFF
			0 1 * *	TRACKING SERVO ON
			1 0 * *	FORWARD TRACK JUMP
			1 1 * *	REVERSE TRACK JUMP
			* * 0 0	SLED SERVO OFF
			* * 0 1	SLED SERVO ON
			* * 1 0	FORWARD SLED MOVE
			* * 1 1	REVERSE SLED MOVE

*: Don’t care

Table 5-9.

TRK Servo

The TRK JUMP (track jump) height can be set with the 6 bits D13 to D8 of $36.
In addition, when the TRK servo is on and D17 of $1 is set to 1, the TRK servo filter assumes gain-up status.
The TRK servo filter also assumes gain-up status when vibration detection is performed with the LOCK signal low and the anti-shock circuit (described hereafter) enabled.
The gain-up filter used when TRK has assumed gain-up status has two types of structures which can be selected by setting D16 of $1. (See Table 5-17.)

SLD Servo

The SLD MOV (sled move) output, composed of a basic value from the 6 bits D13 to D8 of $37, is determined by multiplying this value by × 1, × 2, × 3, or × 4 magnification set using D17 and D16 when D19 = D18 = 0 is set with $3. (See Table 5-10.)
SLD MOV must be performed continuously for 50 µs or more. In addition, if the LOCK input signal goes low when the SLD servo is on, the SLD servo turns off.

Note) When the LOCK signal is low, the TRK servo is set gain-up status and the SLD servo is turned off, by the default. This is disabled by setting D6 (LKSW) of $38 to 1.

Register name	Command	D23 to D20	D19 to D16	
3	SELECT	0 0 1 1	0 0 0 0	SLED KICK LEVEL (basic value × ±1)
			0 0 0 1	SLED KICK LEVEL (basic value × ±2)
			0 0 1 0	SLED KICK LEVEL (basic value × ±3)
			0 0 1 1	SLED KICK LEVEL (basic value × ±4)

Table 5-10.

§5-9. MIRR and DFCT Signal Generation

The RF signal obtained from the RFDC pin is sampled at approximately 1.4MHz and loaded. The MIRR and DFCT signals are generated from this RF signal.

MIRR Signal Generation

The loaded RF signal is applied to peak hold and bottom hold circuits.
An envelope is generated from the waveforms generated in these circuits, and the MIRR comparator level is generated from the average of these envelope waveforms.
The MIRR signal is generated by comparing this MIRR comparator level with the waveform generated by subtracting the bottom hold value from the peak hold value. (See Fig. 5-11.)

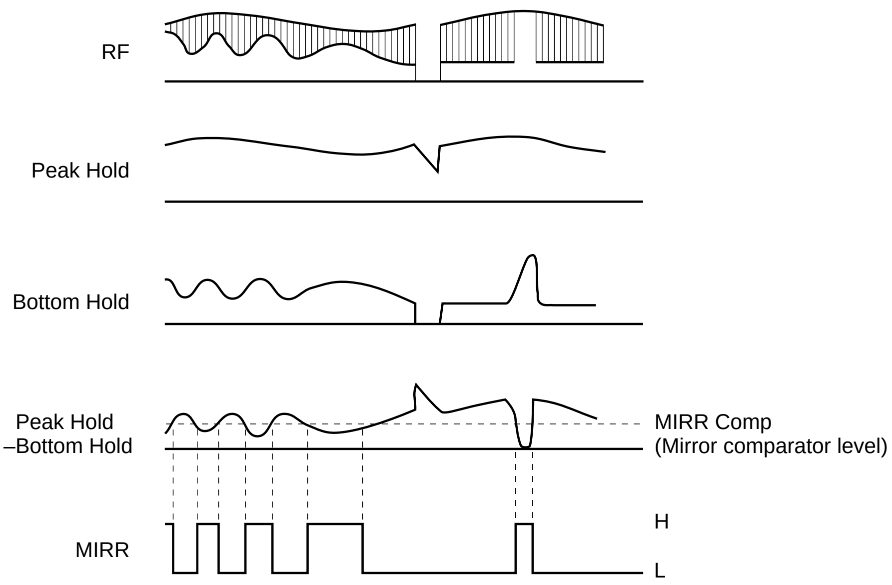


Fig. 5-11.

DFCT Signal Generation

The loaded RF signal is input to two peak hold circuits with different time constants, and the DFCT signal is generated by comparing the difference between these two peak hold waveforms with the DFCT comparator level. (See Fig. 5-12.)
The DFCT comparator level can be selected from four values using D13 and D12 of $3B.

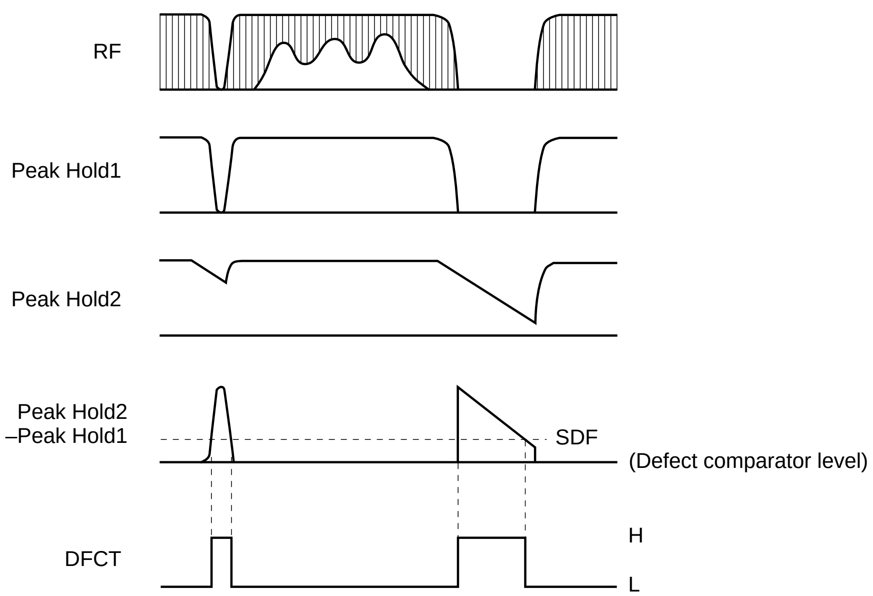


Fig. 5-12.

§5-10. DFCT Countermeasure Circuit

The DFCT countermeasure circuit performs operations to maintain the directionality of the servo so that the servo does not become easily dislocated due to scratches or defects on discs.
Specifically, these operations are achieved by performing scratch and defect detection with the DFCT signal generation circuit, and when DFCT goes high, applying the low frequency component of the error signal before DFCT went high to the FCS and TRK servo filter inputs. (See Fig. 5-13.)
In addition, these operations are activated by the default. They can be disabled by setting D7 (DFSW) of $38 to 1 or by inputting high level to the DFSW pin.

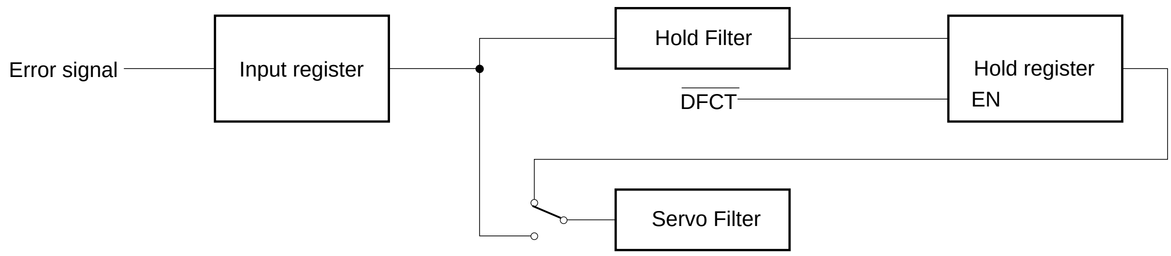


Fig. 5-13.

§5-11. Anti-Shock Circuit

When vibrations are produced in the CD player, this circuit forces the TRK filter to assume gain-up status so that the servo does not become easily dislocated. This circuit is for systems which require vibration countermeasures.
Concretely, vibrations are detected using an internal anti-shock filter and comparator circuit, and the gain is increased. (See Fig. 5-14.) The comparator level is fixed to 1/16 of the maximum comparator input amplitude. However, the comparator level is practically variable by the anti-shock filter output coefficient K35.
This function can be turned on and off by D19 of $1 when the brake circuit (described hereafter) is off. (See Table 5-17.)
This circuit can also support an external vibration detection circuit, and can also set the TRK servo filter to gain-up status by inputting high level to the ATSK pin.
When the serial command is $1, vibration detection can be monitored from the SENS pin.

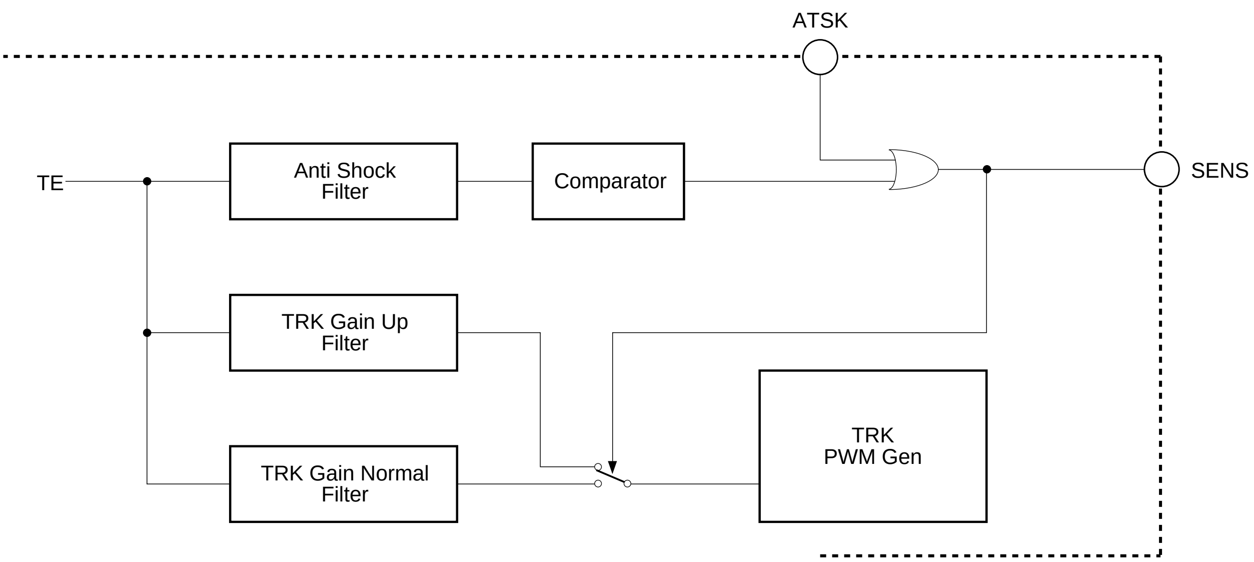


Fig. 5-14.

§5-12. Brake Circuit

Immediately after a long distance track jump it tends to be hard for the actuator to settle and for the servo to turn on.

The brake circuit prevents these phenomenon.

In principle, this circuit cuts unnecessary portions of the tracking drive and works it as the brake by utilizing the 180° offset in the RF envelope and tracking error phase relationship which occurs when the actuator traverses the track in the radial direction from the inner track to the outer track and vice versa. (See Figs. 5-15 and 5-16.)

Concretely, this operation is achieved by masking the tracking drive using the TRKCNCL signal generated by loading the MIRR signal at the edge of the TZC (Tracking Zero Cross) signal.

The brake circuit can be turned on and off by D18 of $1. (See Fig. 5-17.)

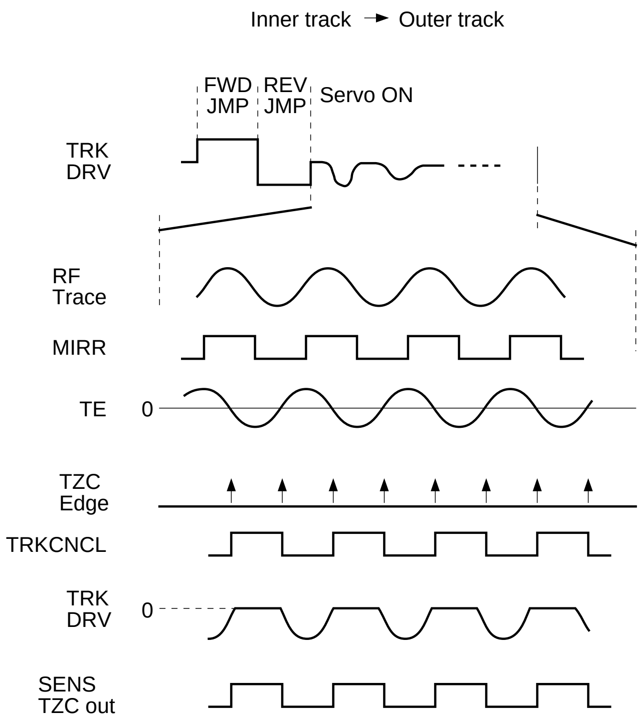


Fig. 5-15.

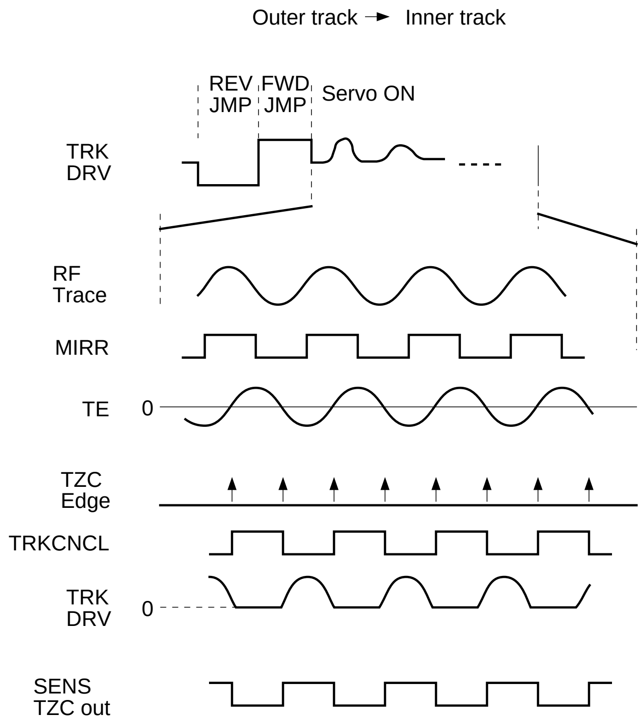


Fig. 5-16.

Register name	Command	D23 to D20	D19 to D16	
1	TRACKING CONTROL	0 0 0 1	1 0 ∗ ∗	ANTI SHOCK ON
			0 ∗ ∗ ∗	ANTI SHOCK OFF
			∗ 1 ∗ ∗	BRAKE ON
			∗ 0 ∗ ∗	BRAKE OFF
			∗ ∗ 0 ∗	TRACKING GAIN NORMAL
			∗ ∗ 1 ∗	TRACKING GAIN UP
			∗ ∗ ∗ 1	TRACKING GAIN UP FILTER SELECT 1
			∗ ∗ ∗ 0	TRACKING GAIN UP FILTER SELECT 2

∗: Don't care

Fig. 5-17.

§5-13. COUT Signal

The COUT signal is output to count the number of tracks during traverse, etc. It is basically generated by loading the MIRR signal at both edges of the TZC signal. However, the used TZC signal can be selected and there are two types of output methods according to the COUT signal application.

for 1-track jumps, etc.
  Fast phase COUT signal with a fast phase TZC signal.

for High-speed traverse
  Reliable COUT signal with a delayed phase TZC signal.

This is because some time is required to generate the MIRR signal, and it is necessary to delay the TZC signal in accordance with the MIRR signal delay during high-speed traverse.
The COUT signal output method is switched with D16 when D19 = D18 = 1 and D17 = 0 are set with $3. (When D16 = 1, for delayed phase and high-speed traverse.) In addition, the TZC signal delay can be selected from two values with D14 of $36.

§5-14. Serial Readout Circuit

The following measurement and adjustment results can be read out from the SENS pin by inputting the readout clock to the SCLK pin by $39. (See Fig. 5-18, Table 5-19 and the Description of SENS Signals.)

Specified commands

$390C	VC AVRG measurement result
$3908	FE AVRG measurement result
$3904	TE AVRG measurement result
$391F	RF AVRG measurement result
$3953	FCS AGCNTL coefficient result
$3963	TRK AGCNTL coefficient result
$391C	TRVSC adjustment result
$391D	FBIAS register value

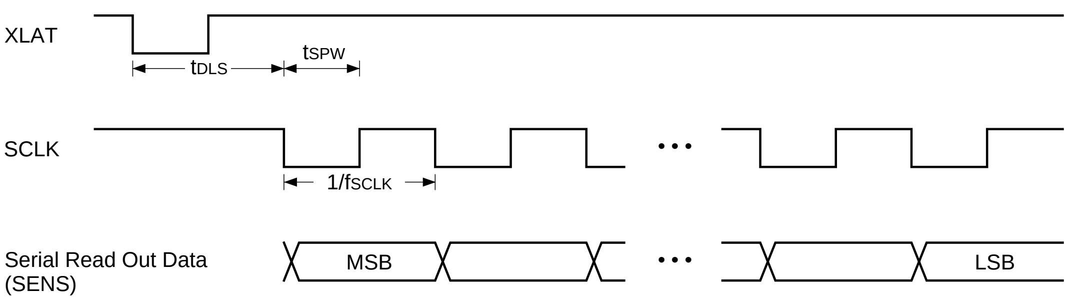


Fig. 5-18.

Item	Symbol	Min.	Typ.	Max.	Unit
SCLK frequency	f_{SCLK}			1	MHz
SCLK pulse width	t_{SPW}	500			ns
Delay time	t_{DLS}	15			µs

Table 5-19.

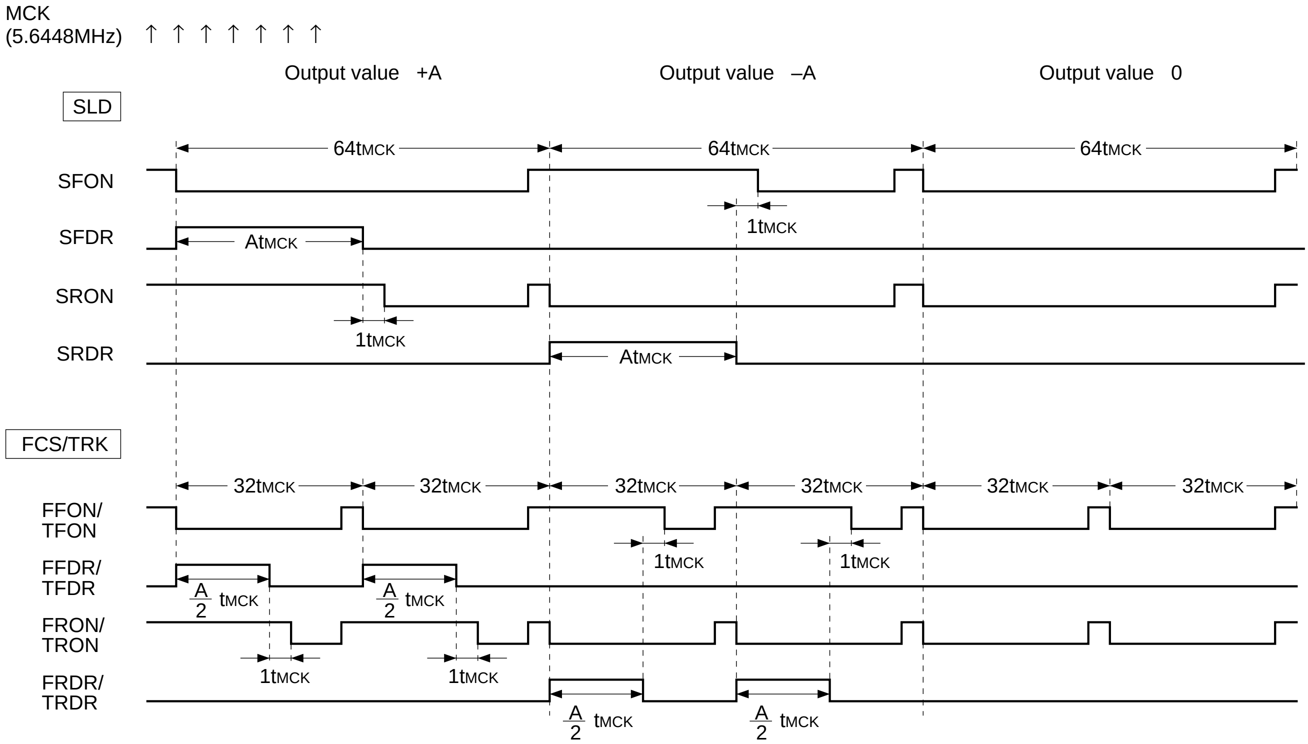
During readout, the upper 8 bits of the serial data must be 39 (Hex).

§5-15. Writing the Coefficient RAM

The coefficient RAM can be rewritten by $34. All coefficients have default values in the built-in ROM, and transfer from the ROM to the RAM is completed approximately 40µs after the XRST pin rises. (The coefficient RAM cannot be rewritten during this period.)
After that, the characteristics of each built-in filter can be finely adjusted by rewriting the data for each address of the coefficient RAM.
The coefficient rewrite command is comprised of 24 bits, with D14 to D8 of $34 as the address (D15 = 0) and D7 to D0 as data.

§5-16. PWM Output

FCS, TRK and SLD outputs are output as PWM waveforms.
In particular, FCS and TRK permit accurate drive by using a double oversampling noise shaper.
Timing Chart 5-20 and Figs. 5-21 and 5-22 show examples of output waveforms and drive circuits.



The ON signal (FON and RON) is active low.

$$t_{MCK} = \frac{1}{5.6448\text{MHz}} \approx 180\text{ns}$$

Timing Chart 5-20.

Example of Driver Circuits

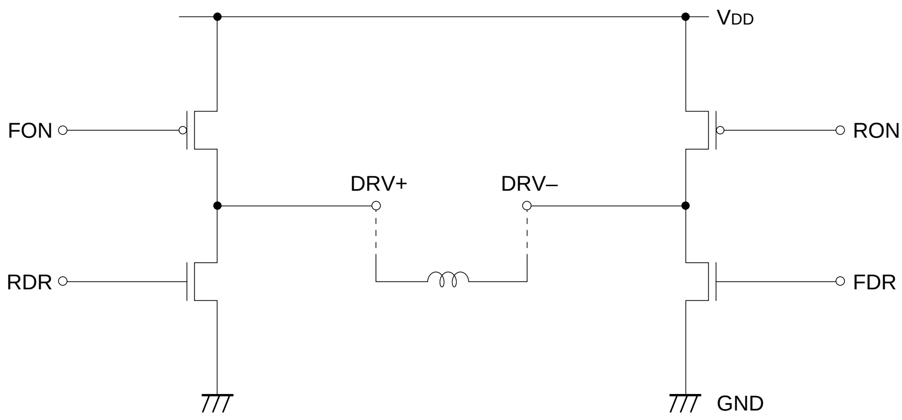


Fig. 5-21. PWM Bridge Drive Circuit

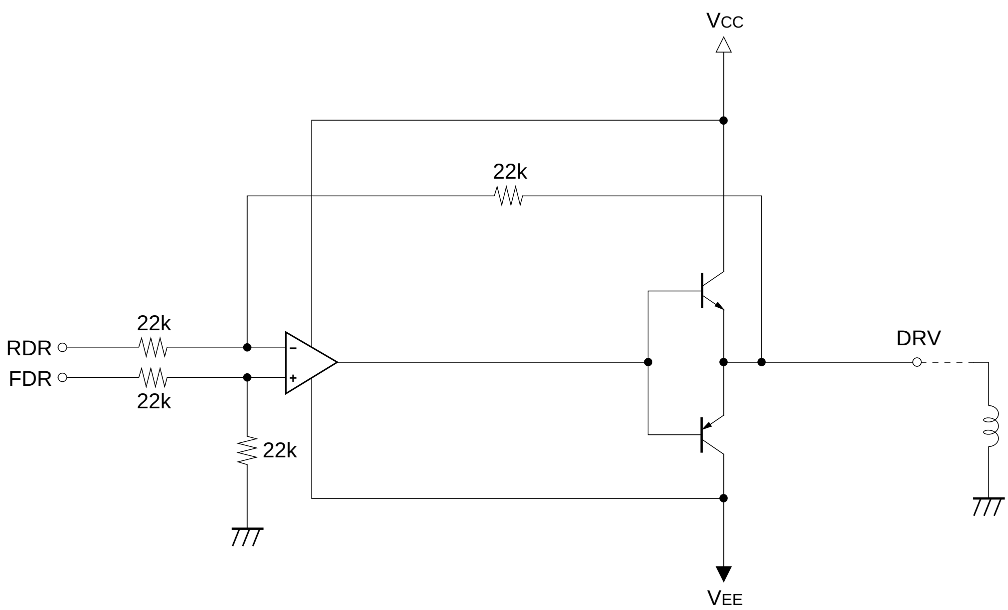


Fig. 5-22. Operational Amplifier Drive Circuit

§5-17. DIRC Input Pin

The $2 command register can be changed by operating the DIRC input pin.
Using the DIRC pin allows serial data transfer to be simplified during TRKJMP.
Fig. 5-23 shows $2 command register changes produced by DIRC pin changes.
In addition, Timing Chart 5-24 shows DIRC-based operations during TRKJMP.
High level must be input to the DIRC pin when the XRST pin rises from low to high.

TRK

Q3	Q2	Servo status
0	0	OFF
0	1	ON
1	0	FWD JMP
1	1	REV JMP

⇒

Q3	Q2	Servo status
1	1	REV JMP
1	0	FWD JMP
1	1	REV JMP
1	0	FWD JMP

⇒

Q3	Q2	Servo status
0	1	ON
0	1	ON
0	1	ON
0	1	ON

SLD

Q1	Q0	Servo status
0	0	OFF
0	1	ON
1	0	FWD MOV
1	1	REV MOV

⇒

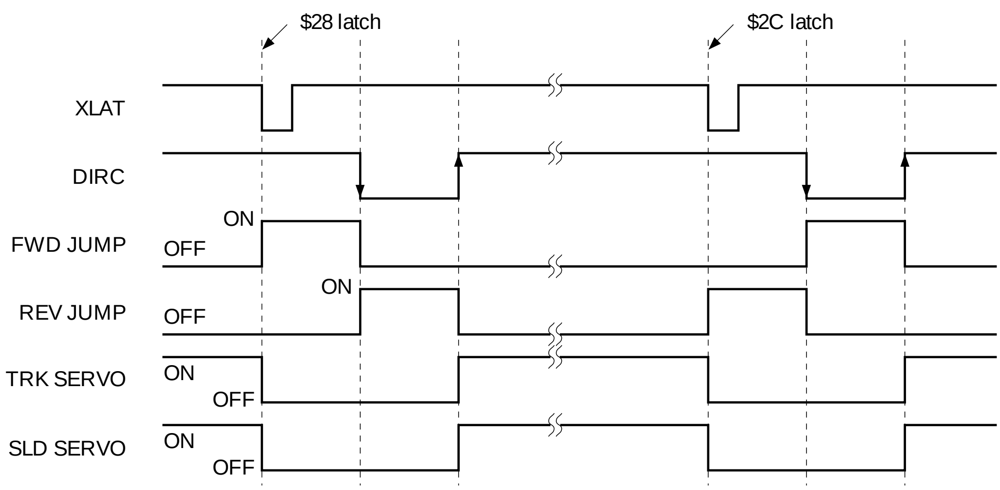
Q1	Q0	Servo status
0	0	OFF
0	1	ON
1	0	FWD MOV
1	1	REV MOV

⇒

Q1	Q0	Servo status
0	1	ON
0	1	ON
1	0	FWD MOV
1	1	REV MOV

Q3, Q2, Q1 and Q0 correspond to D19, D18, D17 and D16 of $2.

Fig. 5-23.



Timing Chart 5-24.

§5-18. Servo Status Changes Produced by the LOCK Signal

When the LOCK signal becomes low, the TRK servo assumes the gain-up status and the SLD servo turns off in order to prevent SLD free-running.
Setting D6 (LKSW) of $38 to 1 deactivates this function.
In other words, neither the TRK servo nor the SLD servo change even when the LOCK signal becomes low.
This enables microcomputer control.

§5-19. Description of Commands and Data Sets

The following description contains portions which convert internal voltages into the values when they are output externally and describe them as input conversion or output conversion.
Input conversion converts these voltages into the voltages entering input pins before A/D conversion.
Output conversion converts PWM output values into analog voltage values.
Both types of conversion are calculated at V_{DD} = 5.0V. If this voltage changes, the conversion values also change proportionally. (Voltage conversion = V_{DDX}/5; V_{DDX}: used supply voltage)

$34

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	KA6	KA5	KA4	KA3	KA2	KA1	KA0	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0

When D15 = 0
KA6 to KA0: Coefficient address
KD7 to KD0: Coefficient data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	0	FBL9	FBL8	FBL7	FBL6	FBL5	FBL4	FBL3	FBL2	FBL1	—

When D15 = D14 = D13 = D12 = D11 = 1 ($34F)
D10 = 0
FBIAS LIMIT register write
FBL9 to FBL1: Data; data compared with FB9 to 1, FBL9 = MSB.
When using the FBIAS register in counter mode, counter operation stops when the value of FB9 to 1 matches FBL9 to 1.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	1	FB9	FB8	FB7	FB6	FB5	FB4	FB3	FB2	FB1	—

When D15 = D14 = D13 = D12 = 1. ($34F)
D11 = 0, D10 = 1
FBIAS register write
FB9 to FB1: Data; FB9 is MSB two's complement data.
For FE input conversion, FB9 to FB1 = 011111111 corresponds to approximately +1V and FB9 to FB1 = 100000000 to –1V respectively. (when the supply voltage = 5V)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	0	TV9	TV8	TV7	TV6	TV5	TV4	TV3	TV2	TV1	TV0

When D15 = D14 = D13 = D12 = 1. ($34F)
D11 = 0, D10 = 1
TRVSC register write
TV9 to TV0: Data; TV9 is MSB two's complement data.
For TE input conversion, TV9 to TV0 = 0011111111 corresponds to approximately +1V and TV9 to TV0 = 1100000000 to –1V respectively. (when the supply voltage = 5V)

Note) • When the TRVSC register is read out, the data length is 9 bits. At this time, data corresponding to each bit of TV8 to TV0 during external write are read out.
• When reading out internally measured values and then writing these values externally, set TV9 the same as TV8.

$35

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FT1	FT0	FS5	FS4	FS3	FS2	FS1	FS0	FTZ	FG6	FG5	FG4	FG3	FG2	FG1	FG0

FT1, FT0, FTZ: Focus search-up speed
Default value: 010 (3.36V/s)
Focus drive output conversion

FT1	FT0	FTZ	Focus search speed
0	0	0	6.73 V/s
0	1	0	3.36
1	0	0	2.24
1	1	0	1.68
0	0	1	8.97
0	1	1	5.38
1	0	1	4.49
1	1	1	3.85

FS5 to FS0: Focus search limit voltage
Default value: 011000 (±1.875V)
Focus drive output conversion

FG6 to FG0: AGF convergence gain setting value
Default value: 0101101

$36

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	DTZC	TJ5	TJ4	TJ3	TJ2	TJ1	TJ0	SFJP	TG6	TG5	TG4	TG3	TG2	TG1	TG0

DTZC: DTZC delay (8.5/4.25µs)
Default value: 0 (4.25µs)

TJ5 to TJ0: Track jump voltage
Default value: 001110 (≈ ±1.09V)
Tracking drive output conversion

SFJP: Surf jump mode on/off
TRK PWM output is made by adding the tracking filter output and TJReg (TJ5 to 0), by setting D7 to 1 (on).

TG6 to TG0: AGT convergence gain setting value
Default value: 0101110

$37

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FZSH	FZSL	SM5	SM4	SM3	SM2	SM1	SM0	AGS	AGJ	AGGF	AGGT	AGV1	AGV2	AGHS	AGHT

FZSH, FZSL: FZC (Focus Zero Cross) slice level
Default value:01 (±250mV); FE input conversion

FZSH	FZSL	Slice level
0	0	+500mV
0	1	+250
1	0	+125
1	1	+62.5

SM5 to SM0: Sled move voltage
Default value: 010000 (≈ ±1.25V)
Sled drive output conversion

AGS: AGCNTL self-stop on/off
Default value: 1 (on)

AGJ: AGCNTL convergence completion judgment time during low sensitivity adjustment (31/63ms)
Default value: 0 (63ms)

AGGF: Focus AGCNTL internally generated sine wave amplitude (small/large)
Default value: 1 (large)

AGGT: Tracking AGCNTL internally generated sine wave amplitude (small/large)
Default value: 1 (large)

		FE/TE input conversion
AGGF	0 (small)	63mV
	1 (large)	125
AGGT	0 (small)	125mV
	1 (large)	250

AGV1: AGCNTL convergence sensitivity during high sensitivity adjustment; high/low
Default value: 1 (high)

AGV2: AGCNTL convergence sensitivity during low sensitivity adjustment; high/low
Default value: 0 (low)

AGHS: AGCNTL high sensitivity adjustment on/off
Default value: 1 (on)

AGHT: AGCNTL high sensitivity adjustment time (128/256ms)
Default value: 0 (256ms)

$38

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VCLM	VCLC	FLM	FLC0	RFLM	RFLC	AGF	AGT	DFSW	LKSW	TBLM	TCLM	FLC1	TLC2	TLC1	TLC0

◎ VCLM: VC level measurement (on/off)
VCLC: VC level compensation for FCS In register (on/off)
◎ FLM: Focus zero level measurement (on/off)
FLC0: Focus zero level compensation for FZC register (on/off)
◎ RFLM: RF zero level measurement (on/off)
RFLC: RF zero level compensation (on/off)
AGF: Focus automatic gain adjustment (on/off)
AGT: Tracking automatic gain adjustment (on/off)
DFSW: Defect disable switch (on/off)
Setting this switch to 1 (on) disables the defect countermeasure circuit.
LKSW: Lock switch (on/off)
Setting this switch to 1 disables the sled free-running prevention circuit.
TBLM: Traverse center measurement (on/off)
◎ TCLM: Tracking zero level measurement (on/off)
FLC1: Focus zero level compensation for FCS In register (on/off)
TLC2: Traverse center compensation (on/off)
TLC1: Tracking zero level compensation (on/off)
TLC0: VC level compensation for TRK/SLD In register (on/off)

Note) Commands marked with ◎ are accepted every 2.9ms.
All commands are on when set to 1.

$39

D15	D14	D13	D12	D11	D10	D9	D8
DAC	SD6	SD5	SD4	SD3	SD2	SD1	SD0

DAC: Serial data readout DAC mode (on/off)
SD6 to SD0: Serial readout data select

<table>
<tr><th>SD6</th><th>SD5</th><th colspan="3">Readout data</th><th>Readout data length</th></tr>
<tr><td>1</td><td colspan="4">Address = coefficient RAM data for (SD5 to SD0)</td><td>8 bits</td></tr>
<tr><td>0</td><td>1</td><td colspan="3">Address = Data RAM data for (SD4 to SD0)</td><td>16 bits</td></tr>
<tr><td rowspan="15">0</td><td rowspan="15">0</td><td>SD4</td><td>SD3 to SD0</td><td></td><td></td></tr>
<tr><td rowspan="6">1</td><td>1 1 1 1</td><td>RF AVRG register</td><td>8 bits</td></tr>
<tr><td>1 1 1 0</td><td>RFDC input signal</td><td>8 bits</td></tr>
<tr><td>1 1 0 1</td><td>FBIAS register</td><td>9 bits</td></tr>
<tr><td>1 1 0 0</td><td>TRVSC register</td><td>9 bits</td></tr>
<tr><td>0 0 1 1</td><td>RFDC envelope (bottom)</td><td>8 bits</td></tr>
<tr><td>0 0 1 0</td><td>RFDC envelope (peak)</td><td>8 bits</td></tr>
<tr><td rowspan="7">0</td><td>1 1 * *</td><td>VC AVRG register</td><td>9 bits</td></tr>
<tr><td>1 0 * *</td><td>FE AVRG register</td><td>9 bits</td></tr>
<tr><td>0 1 * *</td><td>TE AVRG register</td><td>9 bits</td></tr>
<tr><td>0 0 1 1</td><td>FE input signal</td><td>8 bits</td></tr>
<tr><td>0 0 1 0</td><td>TE input signal</td><td>8 bits</td></tr>
<tr><td>0 0 0 1</td><td>SE input signal</td><td>8 bits</td></tr>
<tr><td>0 0 0 0</td><td>VC input signal</td><td>8 bits</td></tr>
</table>

Note) Coefficients K40 to K4F cannot be read out. *: Don’t care
See the description for SRO1 and SRO0 of $3F concerning readout methods for the above data.

$3A

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	FBON	FBSS	FBUP	FBV1	FBV0	0	TJD0	FPS1	FPS0	TPS1	TPS0	CEIT	SJHD	INBK	MTI0

FBON: FBIAS (focus bias) register addition (on/off)
The FBIAS register value is added to the signal loaded into the FCS In register by setting D14 to 1 (on).

FBSS: FBIAS (focus bias) register/counter switching
The FCS BIAS register can be used as a counter by setting D13 to 1 (on).

FBUP: FBIAS (focus bias) counter up/down operation switching
This performs counter up/down control when FBSS = 1. The FBIAS register functions as a down counter when D12 is set to 0, and as an up counter when set to 1.

FBV1, FBV0: FBIAS (focus bias) counter voltage switching
FCS BIAS count up steps is decided by these bits.

FBV1	FBV0	Number of steps
0	0	1
0	1	2
1	0	4
1	1	8

The counter changes once for each sampling cycle of the focus servo filter. When MCK is 128Fs, the sampling frequency is 88.2kHz. When converted to FE input, 1 step is approximately 3.9 [mV].

TJD0: This sets the tracking servo filter data RAM to 0 when switched from track jump to servo on only when SFJP = 1 (during surf jump operation).

FPS1, FPS0: Gain setting when transferring data from the focus filter to the PWM block.

TPS1, TPS0: Gain setting when transferring data from the tracking filter to the PWM block.
This is effective for increasing the overall gain in order to widen the servo band.
Operation when FPS1, FPS0 (TPS1, TPS0) = 00 is the same as usual (7-bit shift). However, 6dB, 12dB and 18dB can be selected independently for focus (tracking) by setting the relative gain to 0dB when FPS1, FPS0 (TPS1, TPS0) = 00.

FPS1	FPS0	Relative gain
0	0	0dB
0	1	+6dB
1	0	+12dB
1	1	+18dB

TPS1	TPS0	Relative gain
0	0	0dB
0	1	+6dB
1	0	+12dB
1	1	+18dB

CEIT: The CE pin input takes over the TE pin input by setting D3 to 1 (on). This means that the registers and filters for TE input are used for CE input.

SJHD: This holds the tracking filter output at the value when surf jump starts during surf jump.

INBK: When D1 is 0 (off), the brake circuit masks the tracking filter output signal with the TRKCNCL which is generated by taking the MIRR signal at the TZC edge. When D1 is set to 1 (on), the tracking filter input is masked instead of the output.

MTI0: The tracking filter input is masked when the MIRR signal is high by setting D0 to 1 (on).

$3B

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFO2	SFO1	SDF2	SDF1	MAX2	MAX1	SFOX	BTF	D2V2	D2V1	D1V2	D1V1	RINT	0	0	0

SFOX, SFO2, SFO1: FOK slice level
Default value: 011 (313mV)
RFDC input conversion

SFOX	SFO2	SFO1	Slice level
0	0	0	179mV
0	0	1	223
0	1	0	268
0	1	1	313
1	0	0	357
1	0	1	446
1	1	0	536
1	1	1	625

SDF2,SDF1: DFCT slice level
Default value: 10 (179mV)
RFDC input conversion

SDF2	SDF1	Slice level
0	0	89mV
0	1	134
1	0	179
1	1	224

MAX2, MAX1: DFCT maximum time
Default value: 00 (no timer limit)

MAX2	MAX1	DFCT maximum time
0	0	No timer limit
0	1	2.00ms
1	0	2.36
1	1	2.72

BTF: Bottom hold double-speed count-up mode for MIRR signal generation
On/off (default: off)
On when set to 1.

D2V2, D2V1: Peak hold 2 for DFCT signal generation
Count-down speed setting
Default value: 01 (0.492V/ms, 44.1kHz)
[V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

D2V2	D2V1	Count-down speed	
		[V/ms]	[kHz]
0	0	0.246	22.05
0	1	0.492	44.1
1	0	0.984	88.2
1	1	1.969	176.4

D1V2, D1V1: Peak hold 1 for DFCT signal generation
Count down speed setting
Default value: 01 (3.938V/ms, 352.8kHz)
[V/ms] unit items indicate RFDC input conversion; [kHz] unit items indicate the operating frequency of the internal counter.

D1V2	D1V1	Count-down speed	
		[V/ms]	[kHz]
0	0	1.969	176.4
0	1	3.938	352.8
1	0	7.875	705.6
1	1	15.75	1411.2

RINT: This initializes the initial-stage registers of the circuits which generate MIRR, DFCT and FOK.

$3E

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
F1NM	F1DM	F3NM	F3DM	T1NM	T1UM	T3NM	T3UM	DFIS	TLCD	RFLP	0	0	0	MIRI	XT1D

F1NM, F1DM: Quasi double accuracy setting for FCS servo filter first-stage
On when set to 1; default = 0.
F1NM: Gain normal
F1DM: Gain down

T1NM, T1UM: Quasi double accuracy setting for TRK servo filter first-stage
On when set to 1; default = 0.
T1NM: Gain normal
T1UM: Gain up

F3NM, F3DM: Quasi double accuracy setting for FCS servo filter third-stage
On when set to 1; default = 0.
Generally, the advance amount of the phase becomes large by partially setting the FCS servo third-stage filter which is used as the phase compensation filter to double accuracy.
F3NM: Gain normal
F3DM: Gain down

T3NM, T3UM: Quasi double accuracy setting for TRK servo filter third-stage
On when set to 1; default = 0.
Generally, the advance amount of the phase becomes large by partially setting the TRK servo third-stage filter which is used as the phase compensation filter to double accuracy.
T3NM: Gain normal
T3UM: Gain up

Note) Filter first- and third-stage quasi double accuracy settings can be set individually.
See FILTER Composition at the end of this specification concerning quasi double-accuracy.

DFIS: FCS hold filter input extraction node selection
0: M05 (Data RAM address 05); default
1: M04 (Data RAM address 04)

TLCD: This command masks the TLC2 command set by D2 of $38 only when FOK is low.
On when set to 1; default = 0

RFLP: This command passes the signal obtained from the RFDC pin through the LPF (low pass filter) before the built-in A/D converter.
0: LPF off; default
1: LPF on

MIRI: MIRR input switching.
The MIRR signal can be input from an external source. When D1 is 0, the MIRR signal is used internally as usual. When D1 = 1, the MIRR signal can be input from an external source through the MIRR pin.

XT1D: The clock input from FSTI can be used as the master clock for the servo block regardless of the XTSL pin, XT2D and XT4D by setting D0 to 1.

$3F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	AGG4	XT4D	XT2D	0	DRR2	DRR1	DRR0	0	ASFG	0	LPAS	SRO1	SRO0	AGHF	COT2

AGG4: This varies the amplitude of the internally generated sine wave using the AGGF and AGGT commands during AGC.
When AGG4 = 0, the default is used. When AGG4 = 1, the setting is as shown in the table below.

AGGF (MSB)	AGGT (LSB)	TE/FE input conversion
0	0	31 [mV]
0	1	63 [mV]
1	0	125 [mV]
1	1	250 [mV]

These settings are the same as for both focus auto gain control and tracking auto gain control.

XT4D, XT2D: MCK (digital servo master clock) frequency division setting
This command forcibly sets the frequency division ratio to 1/2 or 1/4 when MCK is generated from the signal input to the FSTI pin.

XT4D	XT2D	Frequency division ratio
0	0	According to XTSL (default)
0	1	1/2
1	0	1/4

DRR2 to DRR0: Partially clears the Data RAM values (0 write).
The following values are cleared when set to 1 (on) respectively; default = 0
DRR2: M08, M09, M0A
DRR1: M00, M01, M02
DRR0: M00, M01, M02 only when LOCK = low
Note) Set DRR1 and DRR0 for 50µs or more.

ASFG: When vibration detection is performed during anti-shock circuit operation, FCS servo filter is set to gain normal status.
On when set to 1; default = 0

LPAS: Built-in analog buffer low-current consumption mode
This mode reduces the total analog buffer current consumption for the VC, TE, SE and FE input by using a single operational amplifier.
On when set to 1; default = 0
Note) When using this mode, firstly check whether each error signal is properly A/D converted using the SRO1 and SRO0 commands of $3F.

SRO1, SRO0: These commands are to output various data externally continuously which have been specified with the $39 command. (However, D15 (DAC) of $39 must be set to 1.)
Digital output can be obtained from three specified pins (SOCK, XOLT and SOUT) by setting these commands to 1 respectively. The default is 0, 0.

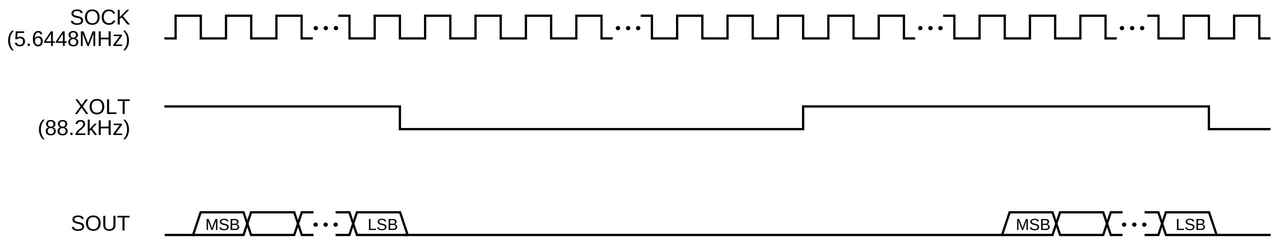
The output pins for each case are shown below.

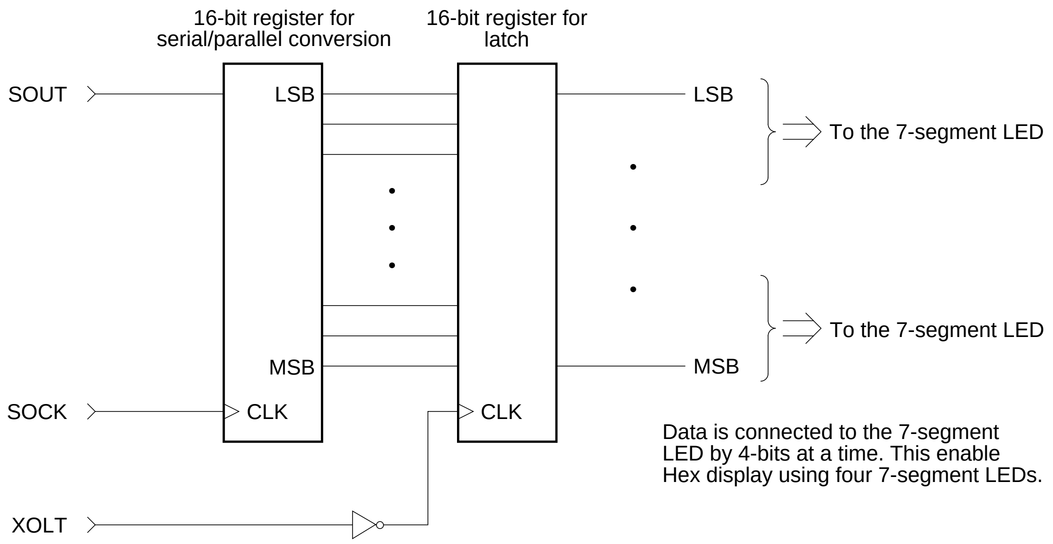
	SRO1 = 1	SRO0 = 1
SOCK	DA13	DA10
XOLT	DA12	DA09
SOUT	DA14	DA11

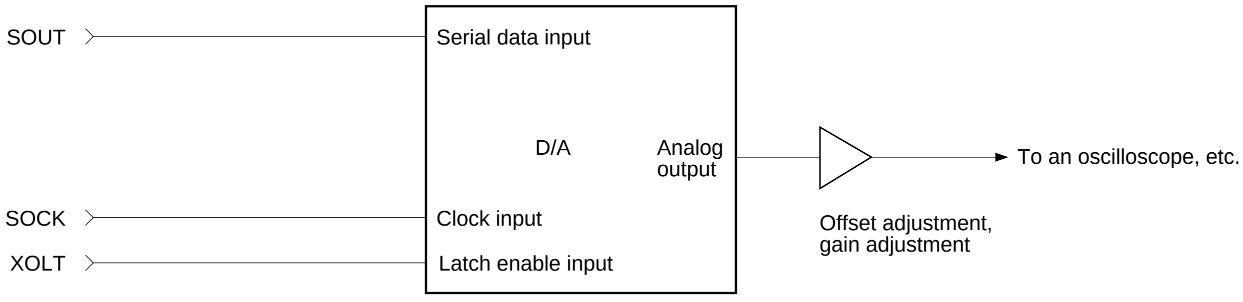
(See the Description of Data Readout on the following page.)

AGHF: This halves the frequency of the internally generated sine wave during AGC.
COT2: The STZC signal is output from COUT by setting D0 to 1.
(STZC: TZC signal generated by sampling the TE signal at 700kHz)

Description of Data Readout







Waveforms can be monitored with an oscilloscope using a serial input-type D/A converter as shown above.

§5-20. List of Servo Filter Coefficients

<Coefficient Preset Value Table (1)>

ADDRESS	DATA	CONTENTS
K00	E0	SLED INPUT GAIN
K01	81	SLED LOW BOOST FILTER A-H
K02	23	SLED LOW BOOST FILTER A-L
K03	7F	SLED LOW BOOST FILTER B-H
K04	6A	SLED LOW BOOST FILTER B-L
K05	10	SLED OUTPUT GAIN
K06	14	FOCUS INPUT GAIN
K07	30	SLED AUTO GAIN
K08	7F	FOCUS HIGH CUT FILTER A
K09	46	FOCUS HIGH CUT FILTER B
K0A	81	FOCUS LOW BOOST FILTER A-H
K0B	1C	FOCUS LOW BOOST FILTER A-L
K0C	7F	FOCUS LOW BOOST FILTER B-H
K0D	58	FOCUS LOW BOOST FILTER B-L
K0E	82	FOCUS PHASE COMPENSATE FILTER A
K0F	7F	FOCUS DEFECT HOLD GAIN
K10	4E	FOCUS PHASE COMPENSATE FILTER B
K11	32	FOCUS OUTPUT GAIN
K12	20	ANTI SHOCK INPUT GAIN
K13	30	FOCUS AUTO GAIN
K14	80	HPTZC / Auto Gain HIGH PASS FILTER A
K15	77	HPTZC / Auto Gain HIGH PASS FILTER B
K16	80	ANTI SHOCK HIGH PASS FILTER A
K17	77	HPTZC / Auto Gain LOW PASS FILTER B
K18	00	Fix*
K19	F1	TRACKING INPUT GAIN
K1A	7F	TRACKING HIGH CUT FILTER A
K1B	3B	TRACKING HIGH CUT FILTER B
K1C	81	TRACKING LOW BOOST FILTER A-H
K1D	44	TRACKING LOW BOOST FILTER A-L
K1E	7F	TRACKING LOW BOOST FILTER B-H
K1F	5E	TRACKING LOW BOOST FILTER B-L
K20	82	TRACKING PHASE COMPENSATE FILTER A
K21	44	TRACKING PHASE COMPENSATE FILTER B
K22	18	TRACKING OUTPUT GAIN
K23	30	TRACKING AUTO GAIN
K24	7F	FOCUS GAIN DOWN HIGH CUT FILTER A
K25	46	FOCUS GAIN DOWN HIGH CUT FILTER B
K26	81	FOCUS GAIN DOWN LOW BOOST FILTER A-H
K27	3A	FOCUS GAIN DOWN LOW BOOST FILTER A-L
K28	7F	FOCUS GAIN DOWN LOW BOOST FILTER B-H
K29	66	FOCUS GAIN DOWN LOW BOOST FILTER B-L
K2A	82	FOCUS GAIN DOWN PHASE COMPENSATE FILTER A
K2B	44	FOCUS GAIN DOWN DEFECT HOLD GAIN
K2C	4E	FOCUS GAIN DOWN PHASE COMPENSATE FILTER B
K2D	1B	FOCUS GAIN DOWN OUTPUT GAIN
K2E	00	NOT USED
K2F	00	NOT USED

<Coefficient ROM Preset Value Table (2)>

ADDRESS	DATA	CONTENTS
K30	80	Fix*
K31	66	ANTI SHOCK LOW PASS FILTER B
K32	00	NOT USED
K33	7F	ANTI SHOCK HIGH PASS FILTER B-H
K34	6E	ANTI SHOCK HIGH PASS FILTER B-L
K35	20	ANTI SHOCK FILTER COMPARATE GAIN
K36	7F	TRACKING GAIN UP2 HIGH CUT FILTER A
K37	3B	TRACKING GAIN UP2 HIGH CUT FILTER B
K38	80	TRACKING GAIN UP2 LOW BOOST FILTER A-H
K39	44	TRACKING GAIN UP2 LOW BOOST FILTER A-L
K3A	7F	TRACKING GAIN UP2 LOW BOOST FILTER B-H
K3B	77	TRACKING GAIN UP2 LOW BOOST FILTER B-L
K3C	86	TRACKING GAIN UP PHASE COMPENSATE FILTER A
K3D	0D	TRACKING GAIN UP PHASE COMPENSATE FILTER B
K3E	57	TRACKING GAIN UP OUTPUT GAIN
K3F	00	NOT USED
K40	04	TRACKING HOLD FILTER INPUT GAIN
K41	7F	TRACKING HOLD FILTER A-H
K42	7F	TRACKING HOLD FILTER A-L
K43	79	TRACKING HOLD FILTER B-H
K44	17	TRACKING HOLD FILTER B-L
K45	6D	TRACKING HOLD FILTER OUTPUT GAIN
K46	00	NOT USED
K47	00	NOT USED
K48	02	FOCUS HOLD FILTER INPUT GAIN
K49	7F	FOCUS HOLD FILTER A-H
K4A	7F	FOCUS HOLD FILTER A-L
K4B	79	FOCUS HOLD FILTER B-H
K4C	17	FOCUS HOLD FILTER B-L
K4D	54	FOCUS HOLD FILTER OUTPUT GAIN
K4E	00	NOT USED
K4F	00	NOT USED

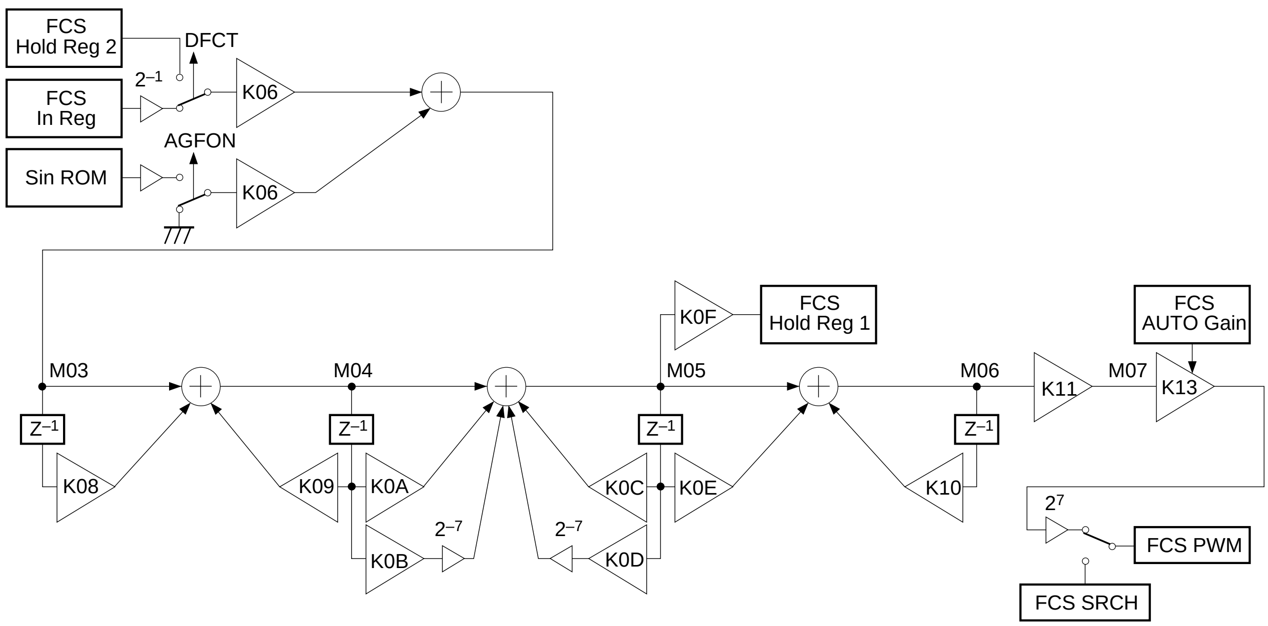
* Fix indicates that normal preset values should be used.

§5-21. FILTER Composition

The internal filter composition is shown below.

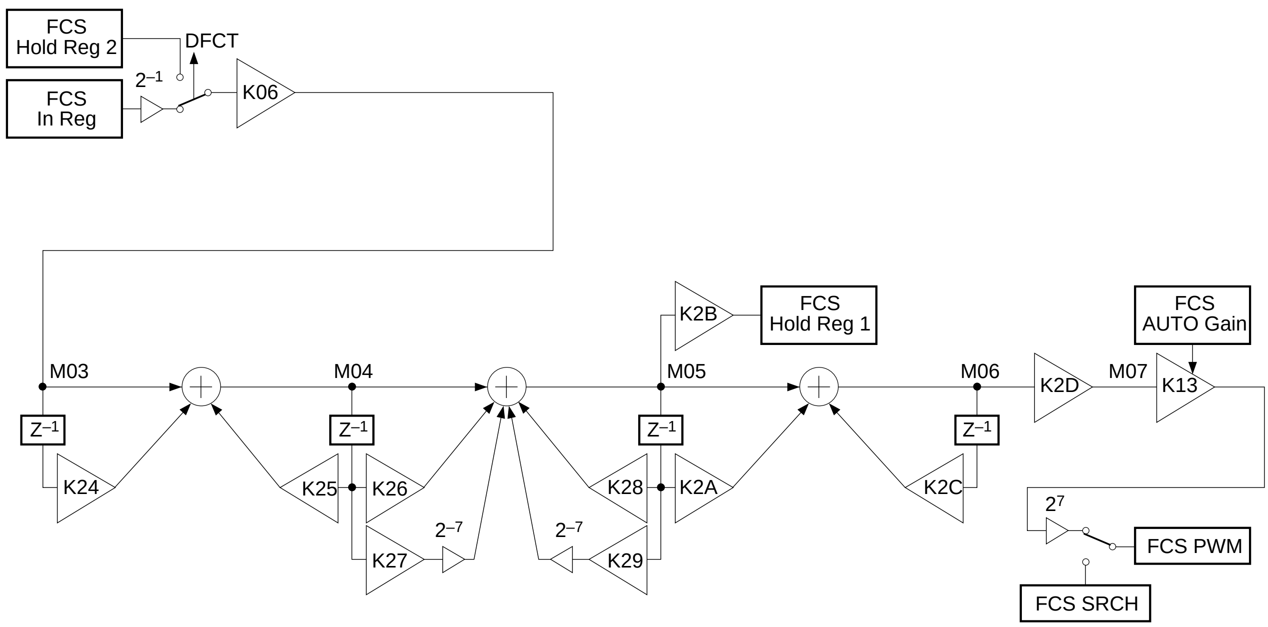
K ∗ ∗ and M ∗ ∗ indicate coefficient RAM and Data RAM address values respectively.

FCS Servo Gain Normal; fs = 88.2kHz



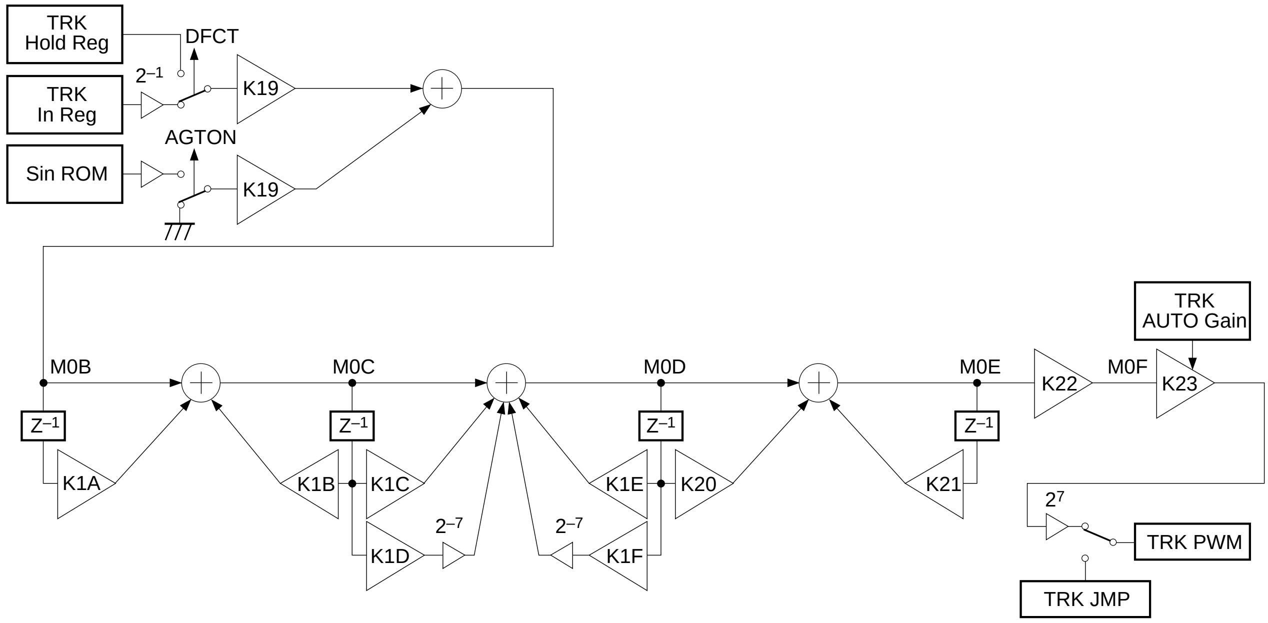
Note) Set the MSB bit of the K0B and K0D coefficients to 0.

FCS Servo Gain Down; fs = 88.2kHz



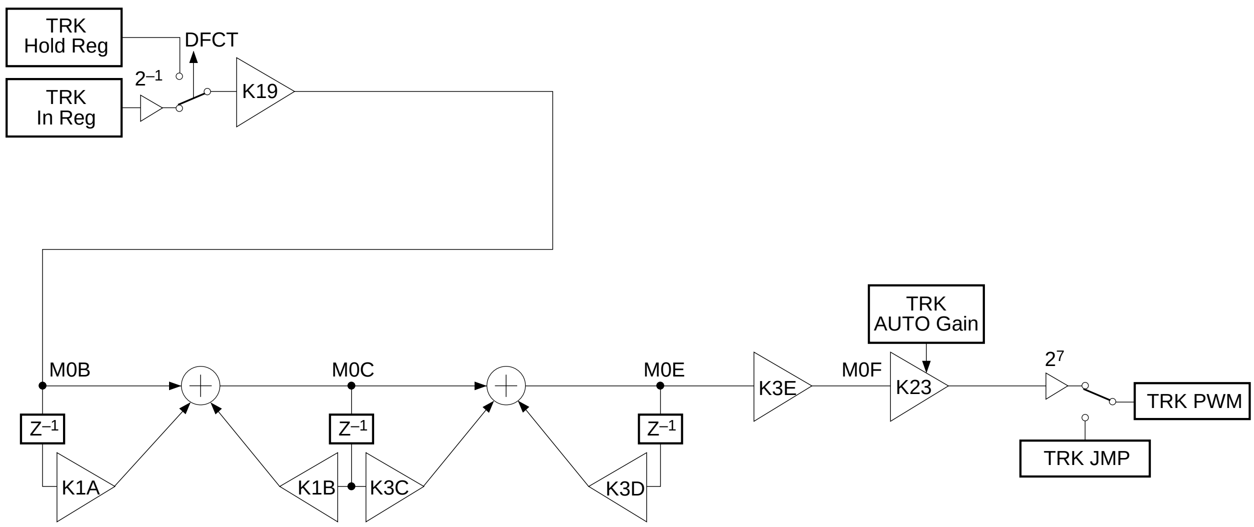
Note) Set the MSB bit of the K27 and K29 coefficients to 0.

TRK Servo Gain Normal; fs = 88.2kHz

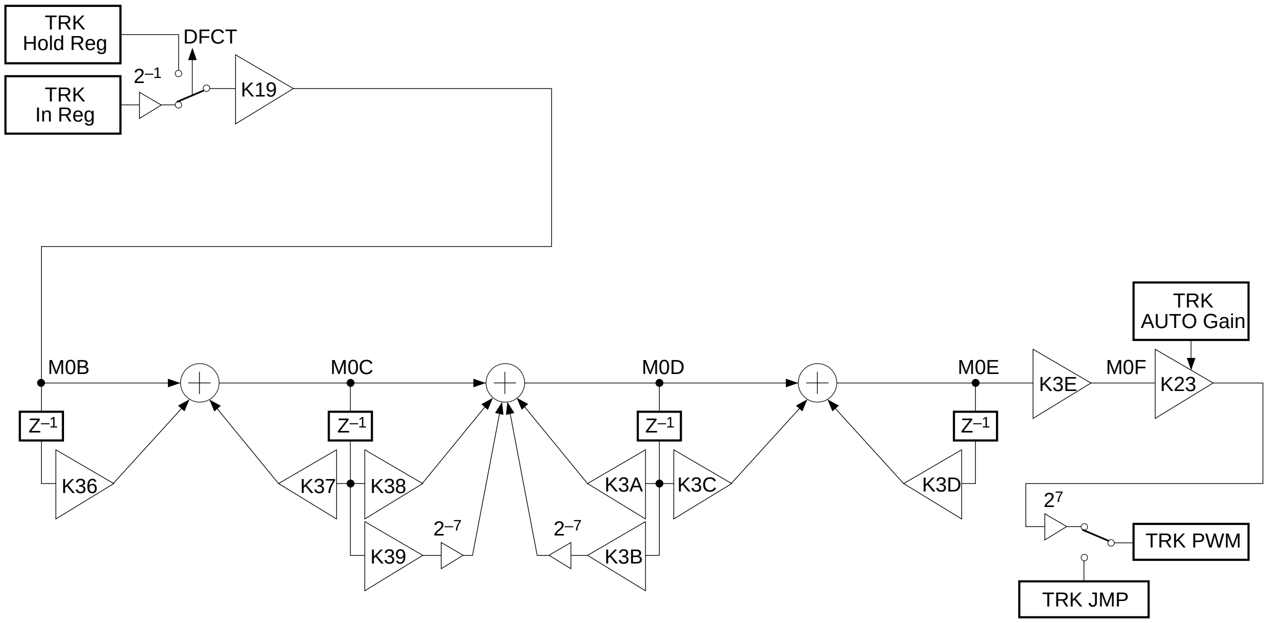


Note) Set the MSB bit of the K1D and K1F coefficients to 0.

TRK Servo Gain Up 1; fs = 88.2kHz

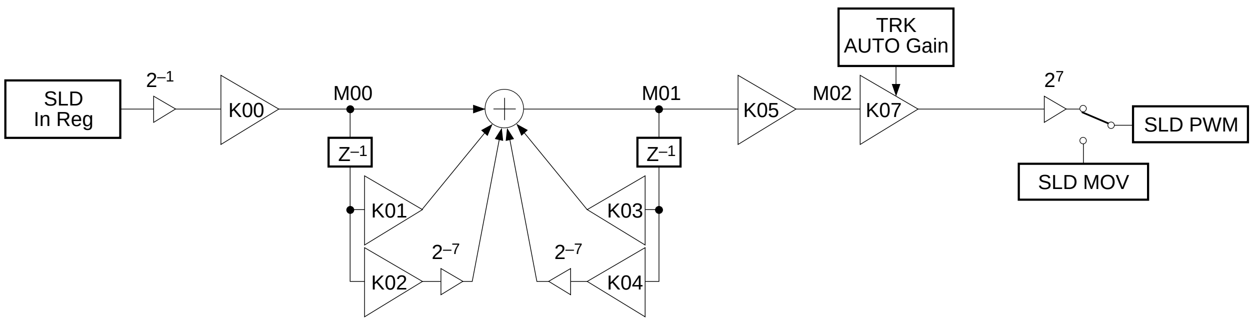


TRK Servo Gain Up 2; fs = 88.2kHz



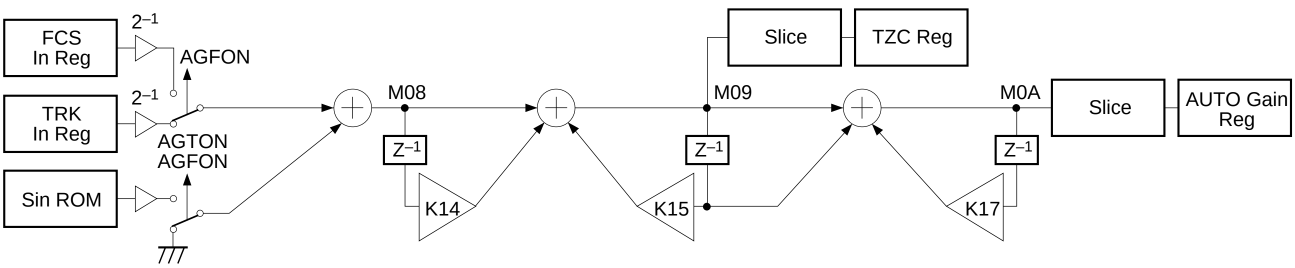
Note) Set the MSB bit of the K39 and K3B coefficients to 0.

SLD Servo; fs = 345Hz

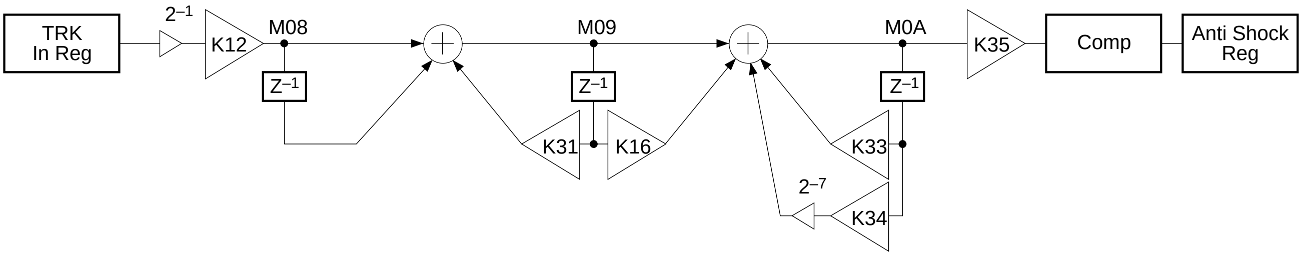


Note) Set the MSB bit of the K02 and K04 coefficients to 0.

HPTZC/Auto Gain; fs = 88.2kHz

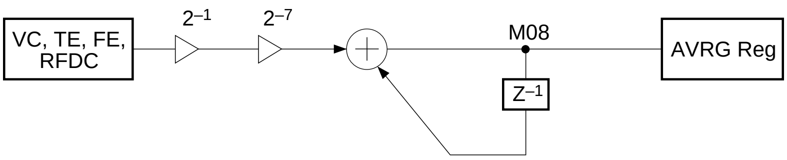


Anti Shock; fs = 88.2kHz

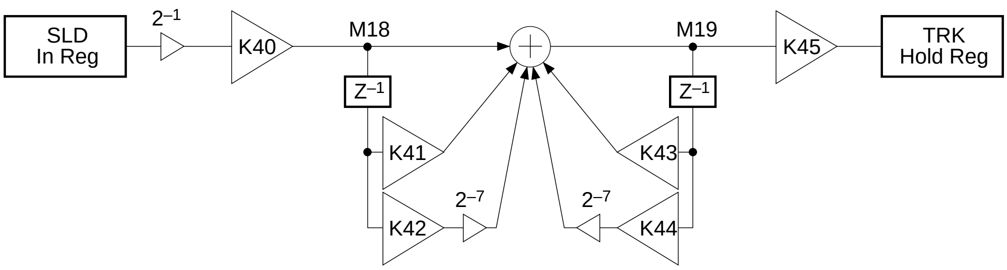


Note) Set the MSB bit of the K34 coefficient to 0.
The comparator level is 1/16 the maximum amplitude of the comparator input.

AVRG; fs = 88.2kHz

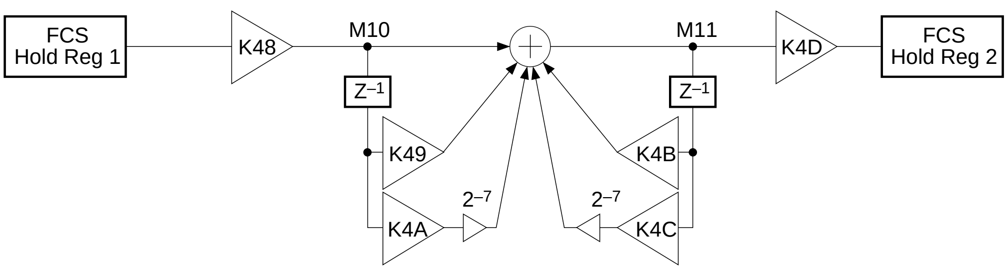


TRK Hold; fs = 345Hz



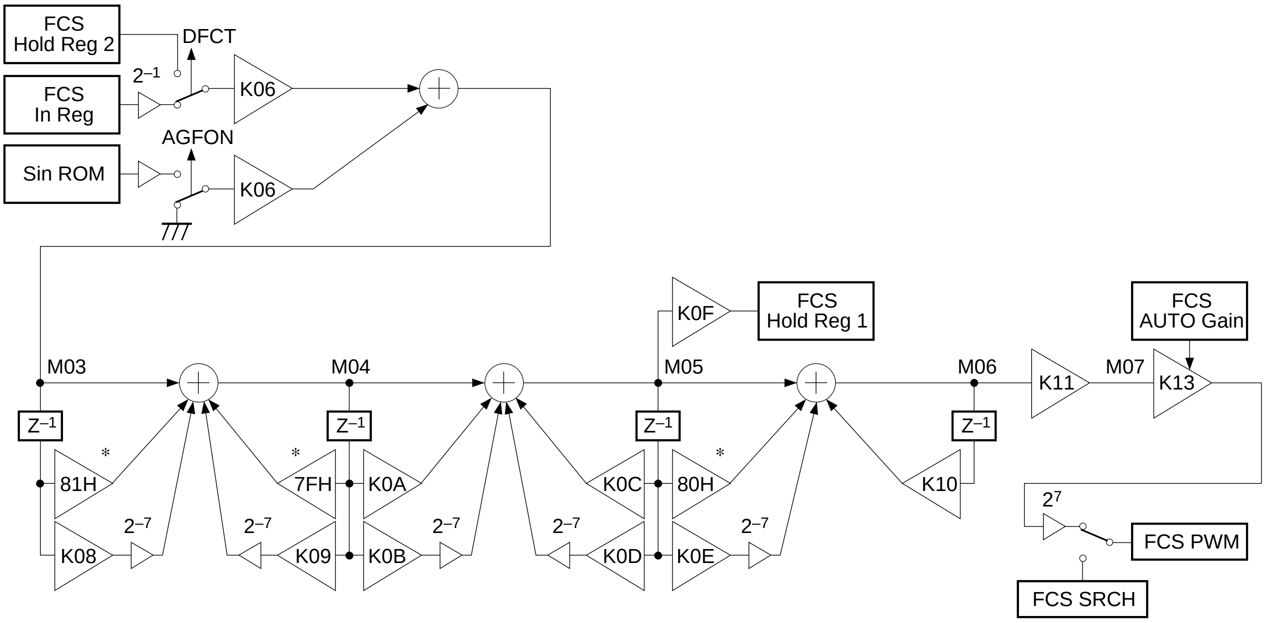
Note) Set the MSB bit of the K42 and K44 coefficients to 0.

FCS Hold; fs = 345Hz



Note) Set the MSB bit of the K4A and K4C coefficients to 0.

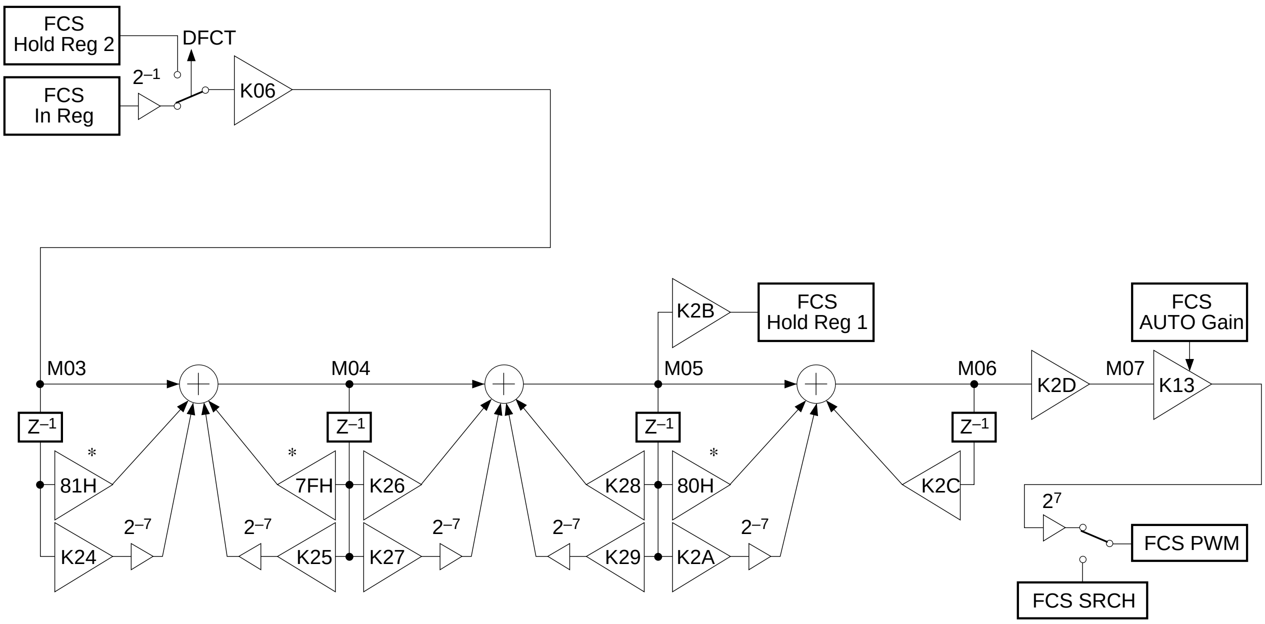
FCS Servo Gain Normal; fs = 88.2kHz, during quasi double accuracy (Ex.: $3EAXX0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K0B and K0D coefficients during normal operation, and of the K08, K09 and K0E coefficients during quasi double accuracy to 0.

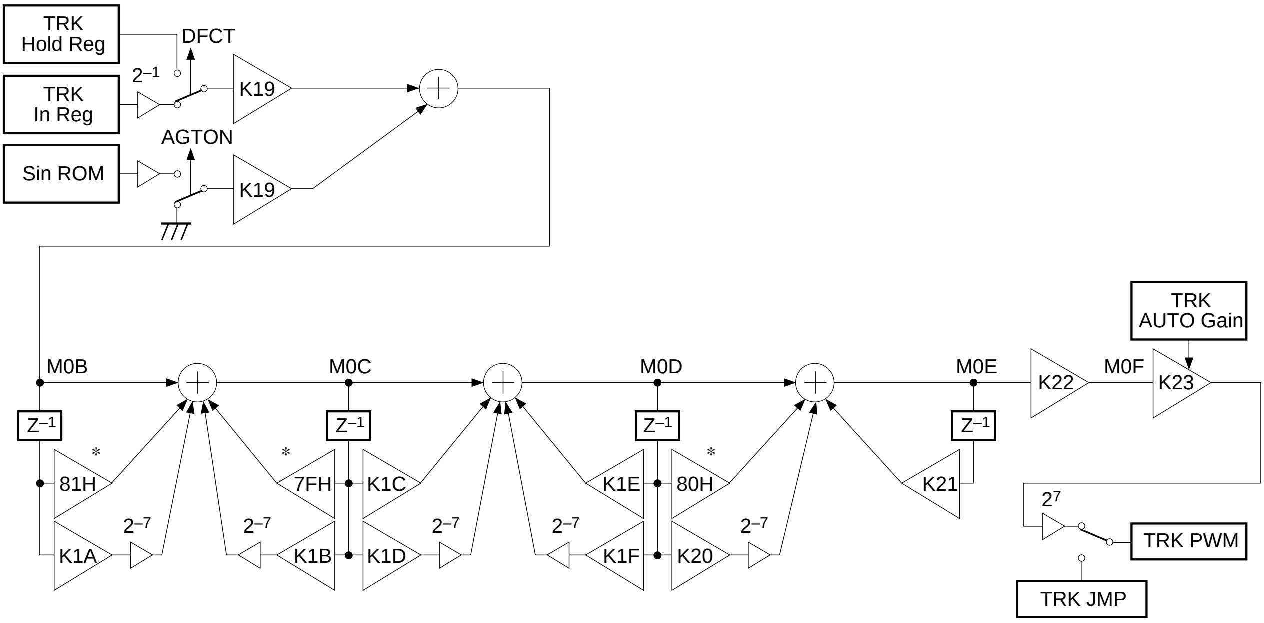
FCS Servo Gain Down; fs = 88.2kHz, during quasi double accuracy (Ex.: $3E5XX0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K27 and K29 coefficients during normal operation, and of the K24, K25 and K2A coefficients during quasi double accuracy to 0.

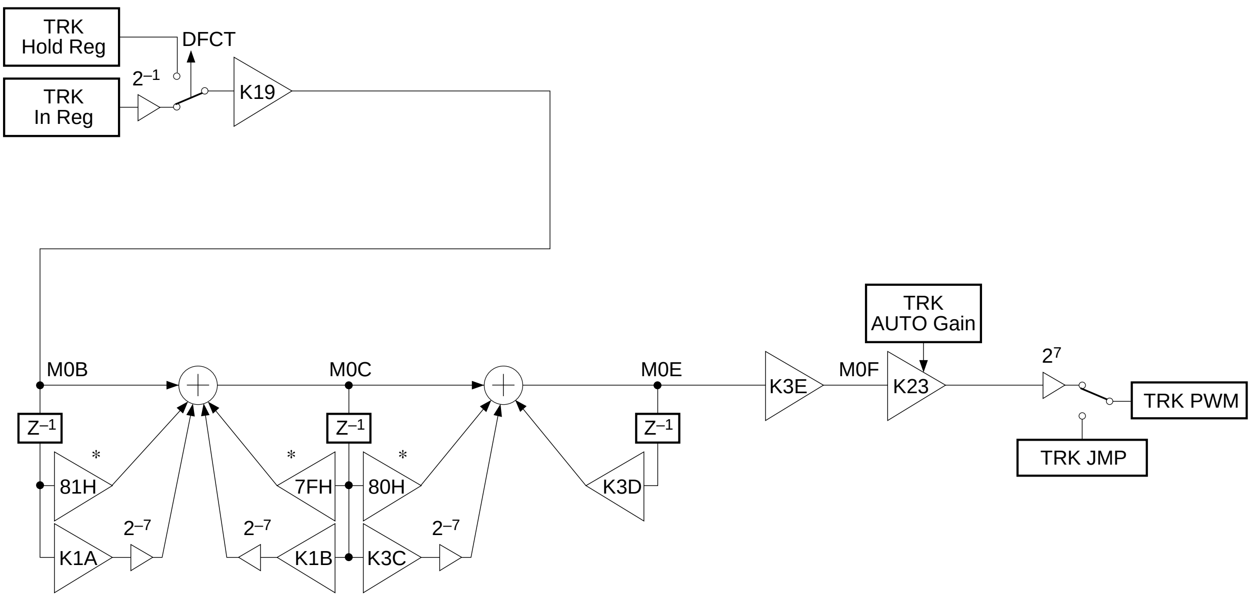
TRK Servo Gain Normal; fs = 88.2kHz, during quasi double accuracy (Ex.: $3EXAX0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K1D and K1F coefficients during normal operation, and of the K1A, K1B and K20 coefficients during quasi double accuracy to 0.

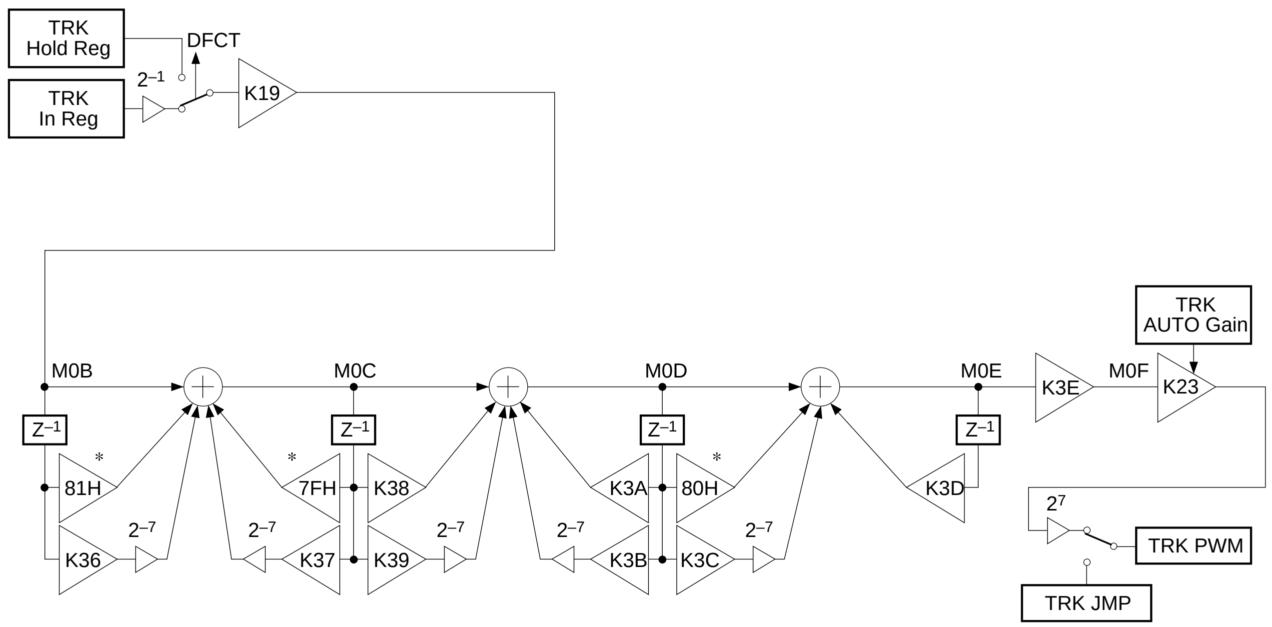
TRK Servo Gain up 1; fs = 88.2kHz, during quasi double accuracy (Ex.: $3EX5X0)



* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

Note) Set the MSB bit of the K1A, K1B and K3C coefficients during quasi double accuracy to 0.

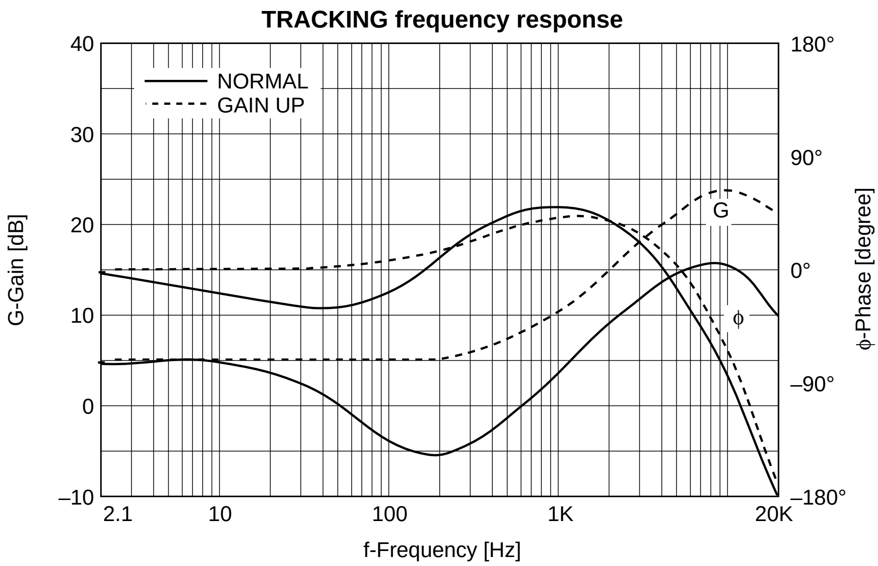
TRK Servo Gain up 2; fs = 88.2kHz, during quasi double accuracy (Ex.: $3EX5X0)

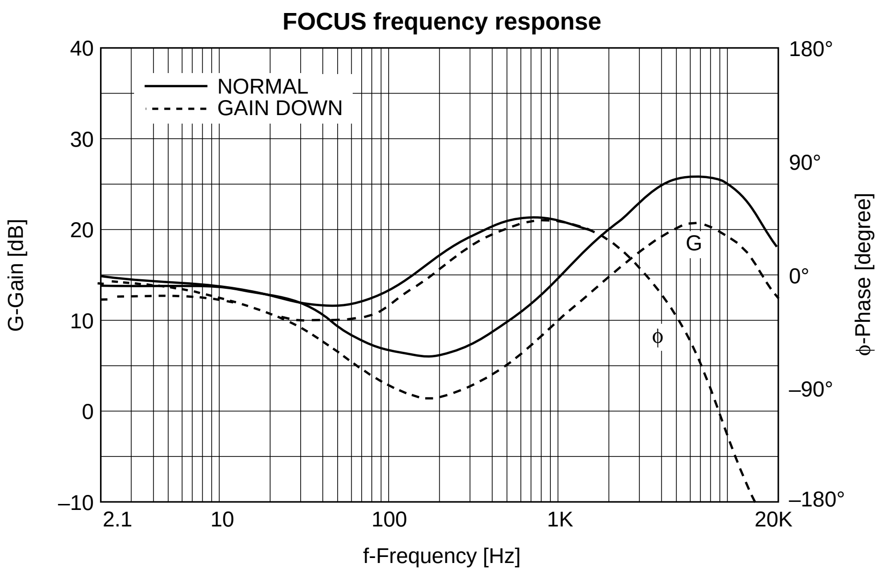


* 81H, 7FH and 80H are each Hex display 8-bit fixed values when set to quasi double accuracy.

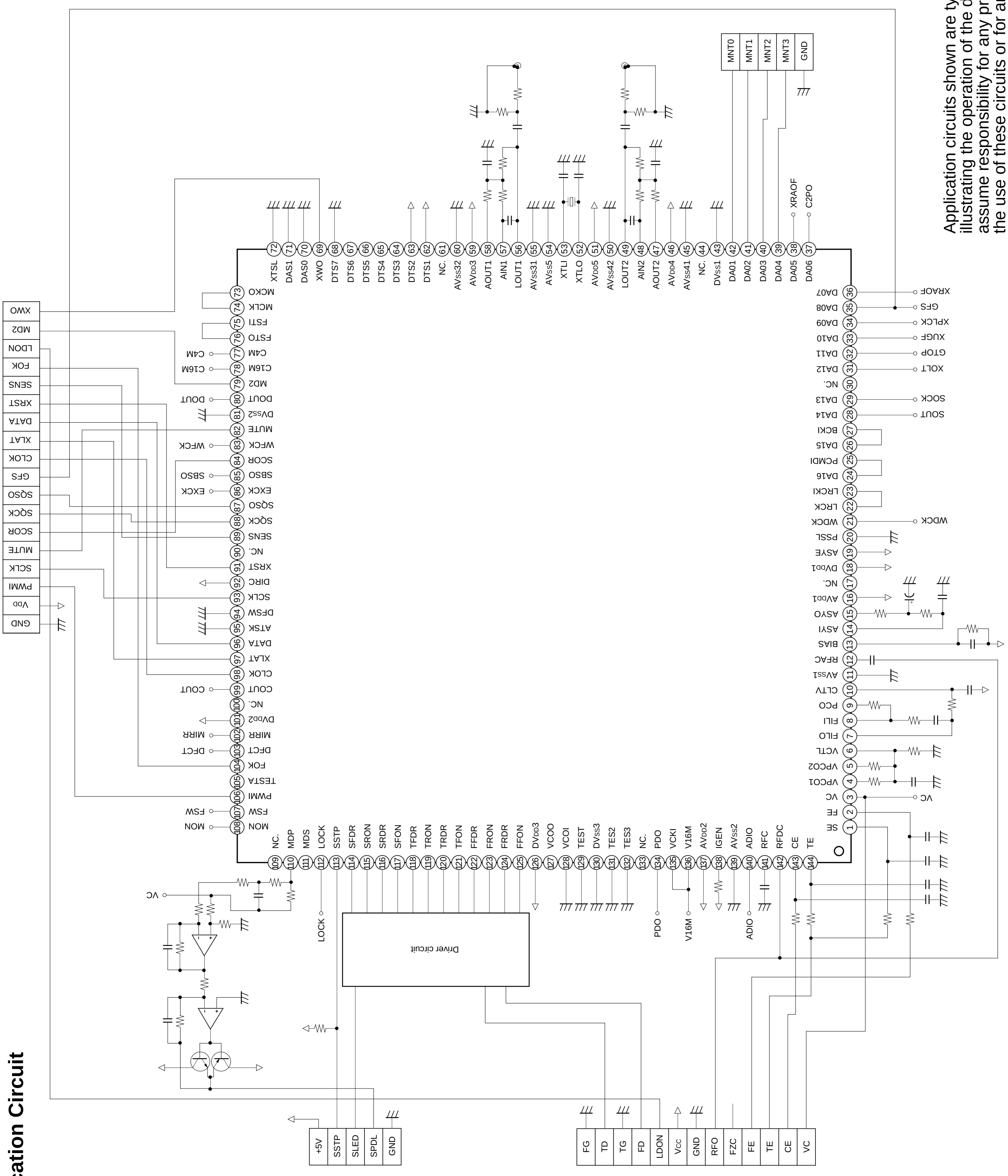
Note) Set the MSB bit of the K39 and K3B coefficients during normal operation, and of the K36, K37 and K3C coefficients during quasi double accuracy to 0.

§5-22. TRACKING and FOCUS Frequency Response





§6-1. Application Circuit

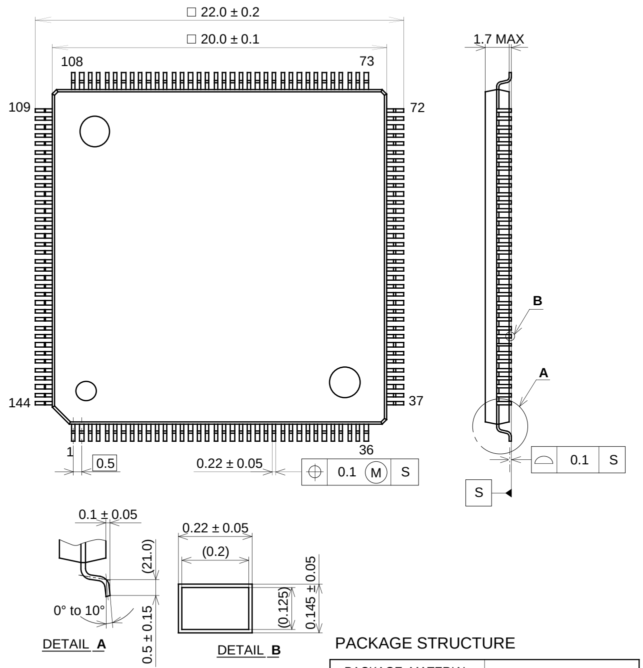


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline Unit: mm

LQFP-144P-L01

144PIN LQFP (PLASTIC)



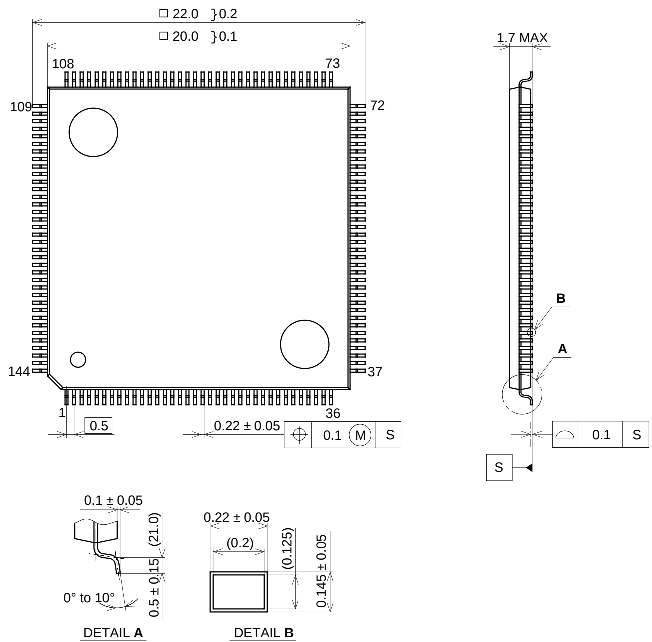
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE WEIGHT	1.3 g

SONY CODE	LQFP-144P-L01
EIAJ CODE	LQFP144-P-2020-A
JEDEC CODE	――――――

LQFP-144P-L021

144PIN LQFP(PLASTIC)



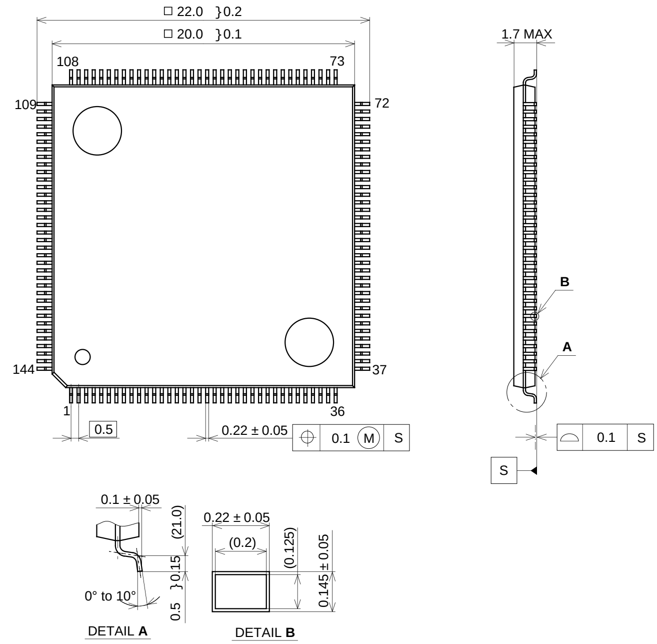
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	1.3g

SONY CODE	LQFP-144P-L021
EIAJ CODE	LQFP144-P-2020
JEDEC CODE	――――――

LQFP-144P-L022

144PIN LQFP(PLASTIC)



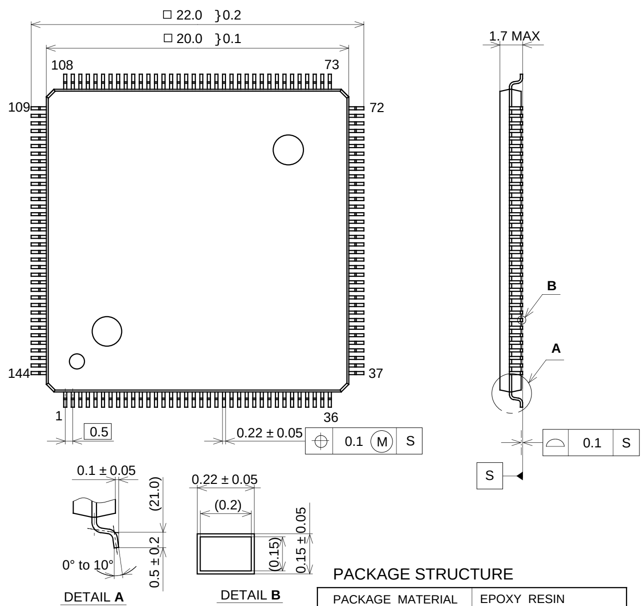
PACKAGE STRUCTURE

SONY CODE	LQFP-144P-L022
EIAJ CODE	LQFP144-P-2020
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE WEIGHT	1.3g

LQFP-144P-L081

144PIN LQFP(PLASTIC)



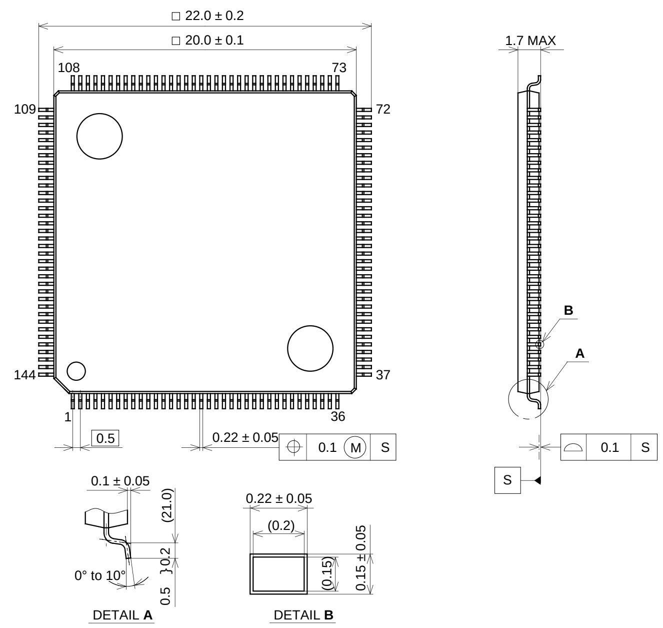
PACKAGE STRUCTURE

SONY CODE	LQFP-144P-L081
EIAJ CODE	LQFP144-P-2020
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	1.3g

LQFP-144P-L141

144PIN LQFP(PLASTIC)



PACKAGE STRUCTURE

SONY CODE	LQFP-144P-L141
EIAJ CODE	LQFP144-P-2020
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	1.3g