



Quad +15V 256-Position Digital Potentiometer with Pin Selectable SPI/I²C Digital Interface

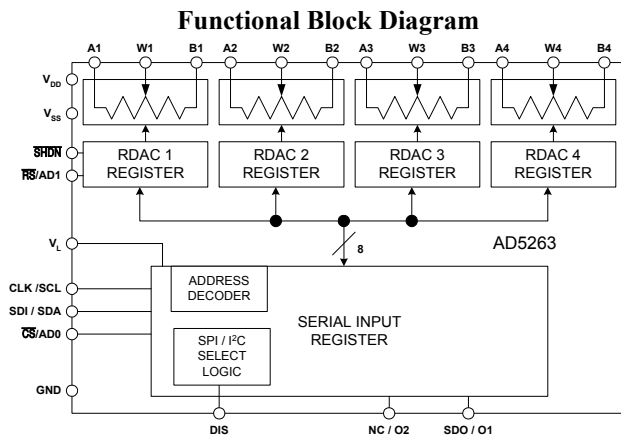
Preliminary Technical Data AD5263

FEATURES

- 4-Channel 256-Position
- End-to-End Resistance 20k, 50k, 200kΩ
- Pin Selectable SPI or I²C Compatible Interface
- Two Package Address Decode Pins AD0 and AD1
- Low Temperature Coefficient 30ppm/°C
- Wide Operating Temperature Range -40 to 125°C
- +5 to +15V Single-Supply; ±7.5V Dual-Supply Operation

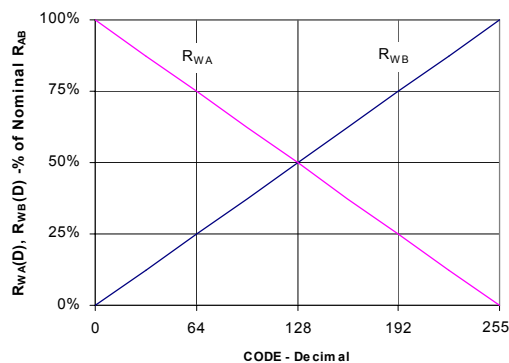
APPLICATIONS

- Mechanical Potentiometer Replacement
- Optical Network Adjustment
- Instrumentation: Gain, Offset Adjustment
- Stereo Channel Audio Level Control
- Automotive Electronics Adjustment
- Programmable Voltage to Current Conversion
- Programmable Filters, Delays, Time Constants
- Line Impedance Matching
- Low Resolution DAC Replacement
- Motor Control



GENERAL DESCRIPTION

The AD5263 is the industries first quad channel, 256 position, digital potentiometer¹ with a selectable digital interface. These devices perform the same electronic adjustment function as mechanical potentiometers or variable resistors with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance. Each channel of the AD5263 contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by a digital code loaded into the 3-wire SPI or 2-wire I²C compatible serial-input register. The resistance between the wiper and either end point of the fixed resistor varies linearly with respect to the digital code transferred into the RDAC latch. The variable resistor offers a completely programmable value of resistance, between the A terminal and the wiper or the B terminal and the wiper. The fixed A to B terminal resistance of 20k, 50k or 200kΩ has a nominal temperature coefficient of 30 ppm/°C. Unlike the majority of the digital potentiometers in the market, these devices can operate up to +15V or ±7.5V.



R_{WA} and R_{WB} vs. Code

The AD5263 is available in narrow body TSSOP-24. All parts are guaranteed to operate over the automotive temperature range of -40°C to +125°C.

NOTE

1. The terms digital potentiometer, VR, and RDAC are used interchangeably.

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Preliminary Technical Data

AD5263

ELECTRICAL CHARACTERISTICS 20k, 50k, 200kΩ VERSION ($V_{DD} = +5V$, $V_{SS} = -5V$, $V_L = +5V$, $V_A = +V_{DD}$, $V_B = 0V$, $-40^\circ C < T_A < +125^\circ C$ unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE Specifications apply to all VRs						
Resistor Differential NL ²	R-DNL	R_{WB} , $V_A=NC$	-1	$\pm 1/4$	+1	LSB
Resistor Nonlinearity ²	R-INL	R_{WB} , $V_A=NC$	-2	$\pm 1/2$	+2	LSB
Nominal resistor tolerance ³	ΔR_{AB}	$T_A = 25^\circ C$	-30		30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	Wiper = No Connect		30		ppm/ $^\circ C$
Wiper Resistance	R_W	$I_W = 1 V/R_{AB}$, $V_{DD} = +5V$		50	100	Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE Specifications apply to all VRs						
Resolution	N				8	Bits
Differential Nonlinearity ⁴	DNL		-1	$\pm 1/4$	+1	LSB
Integral Nonlinearity ⁴	INL		-2	$\pm 1/2$	+2	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 80H		5		ppm/ $^\circ C$
Full-Scale Error	V_{WFSSE}	Code = FFH	-2	-1	+0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00H	0	+1	+2	LSB
RESISTOR TERMINALS						
Voltage Range ⁵	$V_{A,B,W}$		V_{SS}		V_{DD}	V
Capacitance ⁶ Ax, Bx	$C_{A,B}$	$f = 1 \text{ MHz}$, measured to GND, Code = 80H		TBD		pF
Capacitance ⁶ Wx	C_W	$f = 1 \text{ MHz}$, measured to GND, Code = 80H		TBD		pF
Common-Mode Leakage	I_{CM}	$V_A = V_B = V_{DD} / 2$		1		nA
DIGITAL INPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	$V_L = +3V$, $V_{SS} = 0V$	2.1			V
Input Logic Low	V_{IL}	$V_L = +3V$, $V_{SS} = 0V$			0.6	V
Input Current	I_{IL}	$V_{IN} = 0V$ or $+5V$			± 1	μA
Input Capacitance ⁶	C_{IL}			5		pF
DIGITAL Output						
O1, O2	V_{OH}	$I_{OH} = 0.4mA$, I ² C Mode	2.4		5.5	V
O1, O2	V_{OL}	$I_{OL} = -1.6mA$, I ² C Mode	0		0.4	V
SDO	V_{OL}	$I_{OL} = -6mA$			0.6	V
SDO	V_{OL}	$I_{OL} = -3mA$			0.4	V
Three-State Leakage Current	I_{OZ}	$V_{IN} = 0V$ or $+5V$			± 1	μA
Output Capacitance ⁶	C_{OZ}			3	8	pF
POWER SUPPLIES						
Logic Supply	V_L		2.7		5.5	V
Power Single-Supply Range	$V_{DD \text{ RANGE}}$	$V_{SS} = 0V$	4.5		16.5	V
Power Dual-Supply Range	$V_{DD/SS \text{ RANGE}}$		± 4.5		± 7.5	V
Logic Supply Current	I_L	$V_L = +5V$			60	μA
Positive Supply Current	I_{DD}	$V_{IH} = +5V$ or $V_{IL} = 0V$			1	μA
Negative Supply Current	I_{SS}	$V_{SS} = -5V$			1	μA
Power Dissipation ⁹	P_{DISS}	$V_{IH} = +5V$ or $V_{IL} = 0V$, $V_{DD} = +5V$, $V_{SS} = -5V$			0.6	mW
Power Supply Sensitivity	PSS	$\Delta V_{DD} = +5V \pm 10\%$		0.002	0.01	%/%
DYNAMIC CHARACTERISTICS ^{6, 10}						
Bandwidth -3dB	BW	$R_{AB} = 20k/50k/200k\Omega$		400/TBD/TBD		KHz
Total Harmonic Distortion	THD _W	$V_A = 1V_{rms}$, $V_B = 0V$, $f = 1KHz$, $R_{AB} = 20K\Omega$		0.05		%
V_W Settling Time	t_S	$V_A = 10V$, $V_B = 0V$, ± 1 LSB error band		2		μs
Resistor Noise Voltage	e_{N_WB}	$R_{WB} = 10K\Omega$, $f = 1KHz$, $R_S = 0$		9		nV \sqrt{Hz}

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ELECTRICAL CHARACTERISTICS 20k, 50k, 200kΩ VERSION ($V_{DD} = +5V, V_{SS} = -5V, V_L = +5V,$

$V_A = +V_{DD}, V_B = 0V, -40^{\circ}C < T_A < +125^{\circ}C$ unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ ¹	Max	Units
SPI INTERFACE TIMING CHARACTERISTICS applies to all parts (Notes 6,10)						
Clock Frequency	f_{CLK}				25	MHz
Input Clock Pulse Width	t_{CH}, t_{CL}	Clock level high or low	20			ns
Data Setup Time	t_{DS}		10			ns
Data Hold Time	t_{DH}		10			ns
\overline{CS} Setup Time	t_{CSS}		15			ns
\overline{CS} High Pulse Width	t_{CSW}		20			ns
CLK Fall to \overline{CS} Fall Hold Time	t_{CSH0}		0			ns
CLK Fall to \overline{CS} Rise Hold Time	t_{CSH1}		0			ns
\overline{CS} Rise to Clock Rise Setup	t_{CS1}		10			ns
Reset Pulsewidth	t_{RS}		5			ns
I ² C INTERFACE TIMING CHARACTERISTICS applies to all parts(Notes 6,12)						
SCL Clock Frequency	f_{SCL}				400	KHz
t_{BUF} Bus free time between STOP & START	t1		1.3			μs
$t_{HD,STA}$ Hold Time (repeated START)	t2	After this period the first clock pulse is generated	0.6			μs
t_{LOW} Low Period of SCL Clock	t3		1.3			μs
t_{HIGH} High Period of SCL Clock	t4		0.6		50	μs
$t_{SU,STA}$ Setup Time For START Condition	t5		0.6			μs
$t_{HD,DAT}$ Data Hold Time	t6				0.9	μs
$t_{SU,DAT}$ Data Setup Time	t7		100			ns
t_F Fall Time of both SDA & SCL signals	t8				300	ns
t_R Rise Time of both SDA & SCL signals	t9				300	ns
$t_{SU,STO}$ Setup time for STOP Condition	t10		0.6			μs

NOTES:

- Typicals represent average readings at +25°C and $V_{DD} = +5V, V_{SS} = -5V$.
- Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. $I_W = V_{DD}/R$ for both $V_{DD}=+5V, V_{SS}=-5V$.
- $V_{AB} = V_{DD}, Wiper (V_W) =$ No connect
- INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and $V_B = 0V$. DNL specification limits of $\pm 1LSB$ maximum are Guaranteed Monotonic operating conditions.
- Resistor terminals A, B, W have no limitations on polarity with respect to each other.
- Guaranteed by design and not subject to production test.
- Measured at the Ax terminals. All Ax terminals are open circuited in shutdown mode.
- Worst case supply current consumed when input all logic-input levels set at 2.4V, standard characteristic of CMOS logic.
- P_{DJSS} is calculated from $(I_{DD} \times V_{DD})$. CMOS logic level inputs result in minimum power dissipation.
- All dynamic characteristics use $V_{DD} = +5V, V_{SS} = -5V, V_L = +5V$.
- Measured at a V_{WW} pin where an adjacent V_{WW} pin is making a full-scale voltage change.
- See timing diagram for location of measured values. All input control voltages are specified with $t_R=t_F=2ns$ (10% to 90% of +3V) and timed from a voltage level of 1.5V. Switching characteristics are measured using $V_L = +5V$.
- Propagation delay depends on value of $V_{DD}, R_L,$ and C_L .
- The AD5263 contains 5,184 transistors. Die Size: 108mil x 198mil, 21,384sq. mil.

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AD5263

ABSOLUTE MAXIMUM RATINGS¹ ($T_A = +25^\circ\text{C}$, unless otherwise noted)

V_{DD} to GND	-0.3, +16.5V
V_{SS} to GND	0V, -7.5V
V_{DD} to V_{SS}	+16.5V
V_L to GND	-0.3, +6.5V
V_A, V_B, V_W to GND	V_{SS}, V_{DD}
$A_X - B_X, A_X - W_X, B_X - W_X$	
Intermittent ²	$\pm 20\text{mA}$
Continuous	$\pm 5\text{mA}$
Digital Inputs & Output Voltage to GND	0V, +7V
Operating Temperature Range	-40°C to $+85^\circ\text{C}$
Maximum Junction Temperature ($T_{J\text{MAX}}$)	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$+300^\circ\text{C}$
Vapor Phase (60 sec)	$+215^\circ\text{C}$
Infrared (15 sec)	$+220^\circ\text{C}$
Thermal Resistance ³ θ_{JA}	
TSSOP-24	143°C/W

NOTES

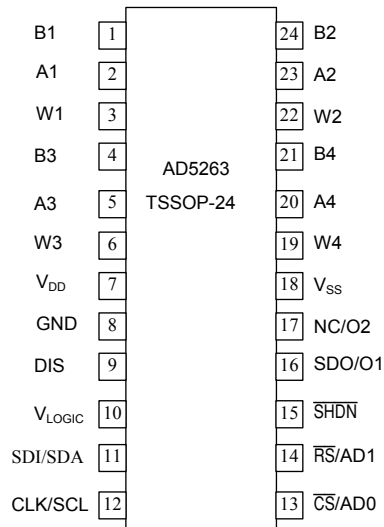
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance
3. Package Power Dissipation $(T_{J\text{MAX}} - T_A) / \theta_{JA}$

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5263 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD5263 PIN CONFIGURATION



8	GND	Ground
9	DIS	Digital Interface Select (SPI/I ² C Select); SPI when DIS='0', I ² C when DIS='1'
10	V _{LOGIC}	Logic Supply Voltage, needs to be same voltage as the digital logic controlling the AD5263.
11	SDI/SDA	SDI = 3-wire Serial Data Input/ SDA = 2-wire Serial Data Input/Output
12	CLK/SCL	Serial Clock Input
13	$\overline{CS}/AD0$	Chip Select / I ² C Compatible Device Address Bit 0
14	$\overline{RS}/AD1$	RESETB/I ² C Compatible Device Address Bit 1
15	\overline{SHDN}	Shutdown -- Ties wiper to terminal A, opens terminal B
16	SDO/O1	Serial Data Output, Open Drain transistor requires pull-up resistor/Digital Output O1, can be used to drive external logic
17	NC/O2	No Connection/Digital Output O2, can be used to drive external logic
18	V _{SS}	Negative power supply, specified for operation from 0 to -5V.
19	W4	Wiper terminal W4 (ADDR=11)
20	A4	Resistor terminal A4
21	B4	Resistor terminal B4
22	W2	Wiper terminal W2 (ADDR=01)
23	A2	Resistor terminal A2
24	B2	Resistor terminal B2

TABLE VII: AD5263 PIN Descriptions

Pin	Name	Description
1	B1	Resistor terminal B1
2	A1	Resistor terminal A1 (ADDR=00)
3	W1	Wiper terminal W1
4	B3	Resistor terminal B3
5	A3	Resistor terminal A3
6	W3	Wiper terminal W3 (ADDR=10)
7	V _{DD}	Positive power supply, specified for +5V to +15V operation

Model	R _{AB} (k Ω)	Temp	Package Description	Package Option	# Parts per Container	Top Mark*
AD5263BRU20	20	-40/+125°C	TSSOP-24	RU-24	62	AD5263B20
AD5263BRU20-REEL7	20	-40/+125°C	TSSOP-24	RU-24	1,000	AD5263B20
AD5263BRU50	50	-40/+125°C	TSSOP-24	RU-24	62	AD5263B50
AD5263BRU50-REEL7	50	-40/+125°C	TSSOP-24	RU-24	1,000	AD5263B50
AD5263BRU200	200	-40/+125°C	TSSOP-24	RU-24	62	AD5263B200
AD5263BRU200-REEL7	200	-40/+125°C	TSSOP-24	RU-24	1,000	AD5263B200

*Line 1 contains part number, line 2 contains ADI logo followed by the end-to-end resistance, line 3 contains date code YYYY.

SPI Compatible Digital Interface (DIS='0')

Table I. AD5263 Serial-Data Word Format

ADDR		DATA							
B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
		MSB							LSB
2^9		2^7							2^0

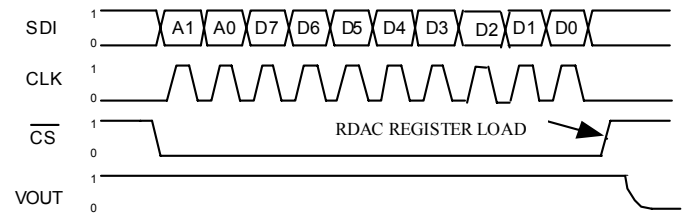


Figure 1a. AD5263 Timing Diagram ($V_A = 5V$, $V_B = 0V$, $V_W = V_{OUT}$)

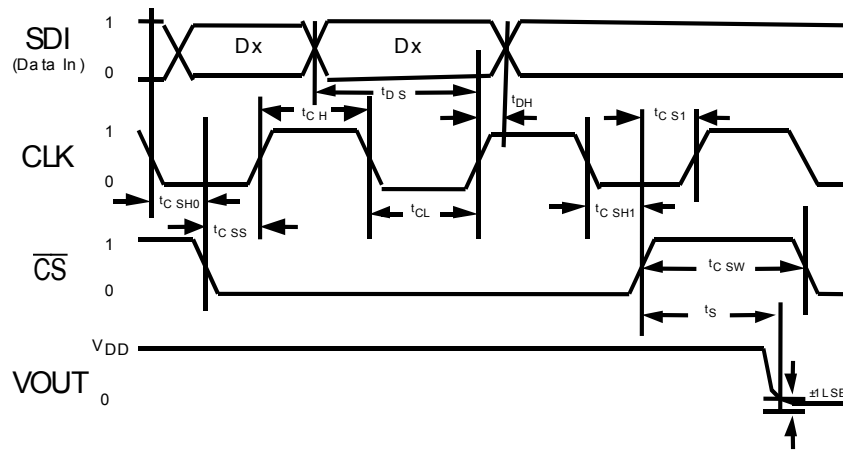


Figure 1b. Detailed Timing Diagram ($V_A = 5V$, $V_B = 0V$, $V_W = V_{OUT}$)

I²C Compatible Digital Interface (DIS='1')

Table IIA. Write Mode

S	0	1	0	1	1	A	A	W	A	X	A	A	R	S	O	O	X	A	D	D	D	D	D	D	D	A	P
Slave Address Byte						Instruction Byte									Data Byte												

Table IIB. I²C Read Mode Data Word Format

S	0	1	0	1	1	0	A	R	A	D	D	D	D	D	D	D	D	A	P
Slave Address Byte							Data Byte												

S = Start Condition

P = Stop Condition

A = Acknowledge

AD1, AD0 = Package pin programmable address bits, Must match with the logic states at pins AD1, AD0

A1, A0 = RDAC sub address select

RS = Software Reset wiper (A1, A0) to mid scale position

SD = Shutdown active high, ties wiper (A1, A0) to terminal A, opens terminal B, RDAC register contents are not disturbed. To exit shutdown a command SD = '0' must be executed for each RDAC (A1, A0).

W = Write = '0'

R = Read = '1'

D7, D6, D5, D4, D3, D2, D1, D0 = Data Bits

X = Don't Care

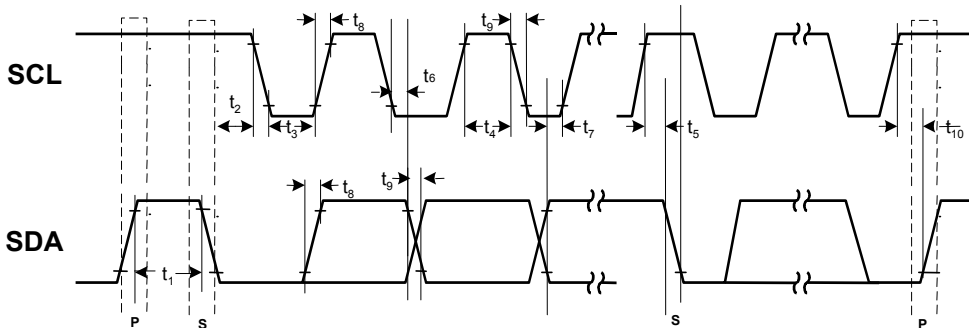


Figure 2. Detailed Timing Diagram

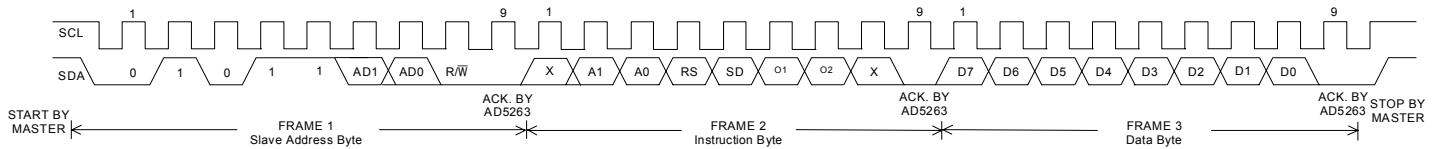


Figure 3a. Writing to the RDAC Register

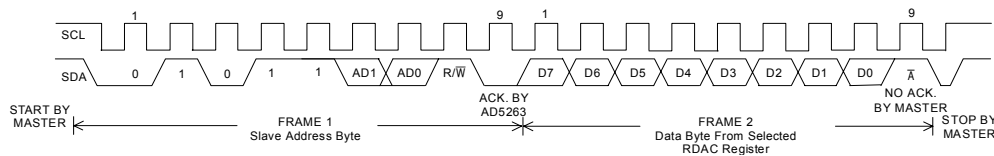


Figure 3b. Reading Data from a Previously Selected RDAC Register in Write Mode

OPERATION

The AD5263 is a quad channel, 256-position digitally-controlled variable resistor (VR) device.

To program the VR settings, refer to the Digital Interface section. Both parts have an internal power ON preset that places the wiper at mid-scale during power on, which simplifies the fault condition recovery at power up. In addition, the shutdown $\overline{\text{SHDN}}$ pin of AD5263 places the RDAC in an almost zero power consumption state where terminal A is open circuited and the wiper W is connected to terminal B, resulting in only leakage current consumption in the VR structure. During shutdown, the VR latch settings are maintained or new settings can be programmed. When the part is returned from shutdown, the corresponding VR setting will be applied to the RDAC.

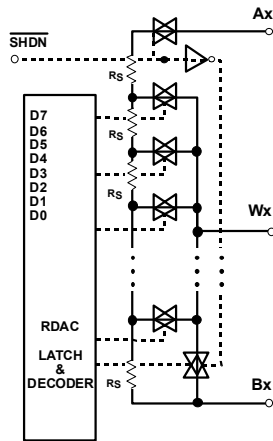


Figure 4. AD5263 Equivalent RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR Rheostat Operation

The nominal resistance of the RDAC between terminals A and B is available in 20k, 50k, and 200k Ω . The final two or three digits of the part number determine the nominal resistance value, e.g. 20k Ω = 20; 50k Ω = 50; 200k Ω = 200. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings.

Assume a 20k Ω part is used, the wiper's first connection starts at the B terminal for data 00 $_H$. Since there is a 60 Ω wiper contact resistance, such connection yields a minimum of 60 Ω resistance between terminals W and B. The second connection is the first tap point corresponds to 138 Ω ($R_{WB} = R_{AB}/256 + R_W = 78\Omega + 60\Omega$) for data 01 $_H$. The third connection is the next tap point representing 216 Ω ($78\Omega \times 2 + 60\Omega$) for data 02 $_H$ and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 19982 Ω [$R_{AB} - 1\text{LSB} + R_W$]. Figure 4 shows a simplified diagram of the equivalent RDAC circuit where the last resistor string will not be accessed; therefore, there is 1 LSB less of the

nominal resistance at full scale in addition to the wiper resistance.

The general equation determining the digitally programmed output resistance between W and B is:

$$R_{WB}(D) = \frac{D}{256} \cdot R_{AB} + R_W \quad (1)$$

where:

D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register

R_{AB} is the end-to-end resistance

R_W is the wiper resistance contributed by the on-resistance of the internal switch

In summary, if $R_{AB} = 20\text{k}\Omega$ and the A-terminal is open circuited, the following output resistance R_{WB} will be set for the following RDAC latch codes.

Table III. Codes and Corresponding Resistances

D (DEC)	R_{WB} (Ω)	Output State
255	19982	Full-Scale ($R_{AB} - 1\text{LSB} + R_W$)
128	10060	Mid-Scale
1	138	1 LSB
0	60	Zero-Scale (Wiper contact resistance)

Note that in the zero-scale condition a finite wiper resistance of 60 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA} . When these terminals are used, the B-terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is:

$$R_{WA}(D) = \frac{256 - D}{256} \cdot R_{AB} + R_W \quad (2)$$

For $R_{AB} = 20\text{k}\Omega$ and B-terminal open circuited, the following output resistance R_{WA} will be set for the following RDAC latch codes (see Table IV).

Table IV. Codes and Corresponding Resistances

D (DEC)	R _{WA} (Ω)	Output State
255	138	Full-Scale
128	10060	Mid-Scale
1	19982	1 LSB
0	20060	Zero-Scale

The typical distribution of the end-to-end resistance R_{AB} from channel-to-channel matches within ±1%. Device to device matching is process lot dependent and is possible to have ±30% variation. Since the resistance element is processed in thin film technology, the change in R_{AB} with temperature has a very low 30 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A to be proportional to the input voltage at A-to-B. Unlike the polarity of V_{DD}-V_{SS}, which must be positive, voltage across A-B, W-A, and W-B can be at either polarity provided that V_{SS} is powered by a negative supply.

If ignoring the effect of the wiper resistance for approximation, connecting A-terminal to 5V and B-terminal to ground produces an output voltage at the wiper-to-B starting at zero volts up to 1 LSB less than 5V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 256 positions of the potentiometer divider. Since the AD5263 can be supplied by dual supplies, the general equation defining the output voltage at V_w with respect to ground for any valid input voltage applied to terminals A and B is:

$$V_w(D) = \frac{D}{256}V_A + \frac{256-D}{256}V_B \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance, V_w can be found as:

$$V_w(D) = \frac{R_{WB}(D)}{256}V_A + \frac{R_{WA}(D)}{256}V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB} and not the absolute values, therefore, the temperature drift reduces to 5 ppm/°C.

PIN SELECTABLE DIGITAL INTERFACE

The AD5263 provides the flexibility of a selectable interface. When the DIS(Digital Interface Select) pin is tied low, the SPI mode is engaged. When the DIS pin is tied high, the I²C mode is engaged.

SPI COMPATIBLE 3-WIRE SERIAL BUS(DIS = '0'):

The AD5263 contains a three-wire SPI compatible digital interface (SDI, CS, and CLK). The 10-bit serial word must be loaded with address bits A1 and A0 followed by the data byte MSB first. The format of the word is shown in Table I.

Table V. AD5263 Address Decode Table

A1	A0	Latch Loaded
0	0	RDAC #1
0	1	RDAC #2
1	0	RDAC #3
1	1	RDAC #4

The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation they should be debounced by a flip-flop or other suitable means. When CS is low, the clock loads data into the serial register on each positive clock edge (see Figure 1a).

Table VI: Input Logic Control Truth Table

CLK	CS	RS	SHDN	Register Activity
L	L	H	H	No SR effect, enables SDO pin
P	L	H	H	Shift One bit in from the SDI pin. Previous ten bits are shifted out of the SDO pin.
X	P	H	H	Load SR data into RDAC latch based on address decoder (Table V).
X	H	H	H	No Operation
X	X	L	H	Sets all RDAC latches to midscale clears SDO latch.
X	H	H	L	Open circuits all resistor A-terminals, connects W to B, turns off SDO output transistor.

NOTE: P = positive edge, X = don't care, SR = shift register

The data setup and data hold times in the specification table determine the valid timing requirements. The AD5263 uses a 10-bit serial input data register word that is transferred to the internal RDAC register when the CS line returns to logic high. Any extra bits are ignored. Also, as CS goes high, it activates the address decoder and updates the corresponding channel

During shutdown(SHDN), the SDO output pin is forced to logic high in order to avoid power dissipation in the external pull up resistor. For equivalent SDO output circuit schematic (see Figure 5).

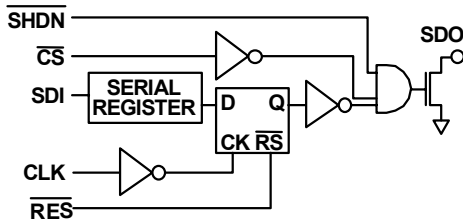


Figure 5. Detailed SDO output schematic of the AD5263

Daisy-Chain Operation

The serial data output (SDO) pin contains an open drain n-channel FET. This output requires a pull-up resistor in order to transfer data to the next package's SDI pin. This allows for daisy chaining several RDACs from a single processor serial data line. The pull-up resistor termination voltage can be larger than the V_{DD} supply voltage. It is recommended to increase the clock period when using a pull-up resistor to the SDI pin of the following device because capacitive loading at the daisy-chain node SDO-SDI between devices may induce time delay to subsequent devices. Users should be aware of this potential problem to achieve data transfer successfully (see Figure 6). If two AD5263s are daisy-chained, a total of 20 bits of data is required. The first 10 bits, complying with the format shown in Table 1, go to U2 and the second 10 bits with the same format go to U1. \overline{CS} should be kept low until all 20 bits are clocked into their respective serial registers. After this, the \overline{CS} is pulled high to complete the operation and load the RDAC latch.

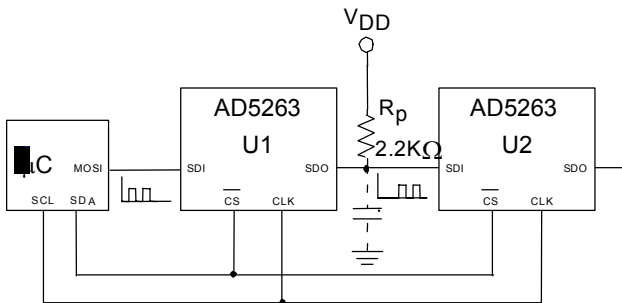


Figure 6. Daisy-Chain Configuration

I²C COMPATIBLE 2-WIRE SERIAL BUS(DIS = '1'):

The AD5263 is controlled via an I²C compatible serial bus. The RDACs are connected to this bus as slave devices.

Referring to Figures 2 and 3, the first byte of AD5263 is a Slave Address Byte. It has a 7-bit slave address and a $\overline{R/W}$ bit. The 5 MSBs are 01011 and the following two bits are determined by the state of the AD0 and AD1 pins of the device. AD0 and AD1 allow the user to place up to four of the I²C compatible devices on one bus.

The 2-wire I²C serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 3a). The following byte is the Slave

Address Byte which consists of the 7-bit slave address followed by an $\overline{R/W}$ bit (this bit determines whether data will be read from or written to the slave device).

The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the Acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the $\overline{R/W}$ bit is high, the master will read from the slave device. On the other hand, if the $\overline{R/W}$ bit is low, the master will write to the slave device.

2. A write operation contains an extra Instruction Byte more than a read operation. Such an Instruction Byte in write mode follows the Slave Address Byte. The first two bits(MSB and second MSB) of the Instruction Byte labeled A1 and A0 are the RDAC subaddress selects.

The third MSB RS is the midscale reset. A logic high of this bit moves the wiper of a selected channel to the center tap where $R_{WA} = R_{WB}$. This feature effectively writes over the contents of the register and thus when taken out of reset mode, the RDAC will remain at midscale.

The fourth MSB SD is a shutdown bit. A logic high causes the selected channel to open circuit at terminal A while shorting the wiper to terminal B. This operation yields almost 0Ω in rheostat mode or zero volt in potentiometer mode. This SD bit serves the same function at the \overline{SHDN} pin except that the \overline{SHDN} pin reacts to active low. Also, the \overline{SHDN} pin affects both channels as opposed to the SD bit which only affects the channel that is being written to. It is important to note that the shutdown operation does not disturb the contents of the register. When brought

out of shutdown, the previous setting will be applied to the RDAC.

The following two bits are O2 and O1. They are extra programmable logic outputs that can be used to drive other digital loads, logic gates, LED drivers, analog switches, and so on. The three LSBs are don't care (see Table IIA).

3. After acknowledging the Instruction Byte, the last byte in Write Mode is the Data Byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an Acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Table IIA).
4. In the Read Mode, the Data Byte follows immediately after the acknowledgment of the Slave Address Byte. Data is transmitted over the serial bus in sequences of nine clock pulses (a slight difference with the Write mode, where there are eight data bits followed by an

Acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 3b).

- When all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In Write Mode, the master will pull the SDA line high during the tenth clock pulse to establish a Stop condition (see Figure 3a). In Read mode, the master will issue a No Acknowledge for the ninth clock pulse (i.e., the SDA line remains high). The master will then bring the SDA line low before the tenth clock pulse which goes high to establish a STOP condition (see Figure 3b).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. During the write cycle, each data byte will update the RDAC output. For example, after the RDAC has acknowledged its slave address and instruction bytes, the RDAC output will update after these two bytes. If another byte is written to the RDAC while it is still addressed to a specific slave device with the same instruction, this byte will update the output of the selected slave device. If different instructions are needed, the write mode has to start with a new Slave Address, Instruction, and Data Byte again. Similarly, a repeated read function of the RDAC is also allowed.

READBACK RDAC VALUE

AD5263 allows the user to read back the RDAC values in the Read Mode. The channel of interest is the one that is previously selected in the Write Mode. In the case where users need to read the RDAC values of both channels, they need to program the first channel in the Write Mode and then change to the Read Mode to read the first channel value. After that, they need to change back to the Write Mode with the second channel selected and read the second channel value in the Read Mode again. Note that it is not necessary for users to issue the Frame 3 data byte in the write mode for subsequent readback operation. Users should refer to Tables IIA and IIB for the programming format.

ADDITIONAL PROGRAMMABLE LOGIC OUTPUT

AD5263 features additional programmable logic outputs, O₁ and O₂, which can be used to drive a digital load, analog switches, and logic gates. O₁ and O₂ default to logic 0. The logic states of O₁ and O₂ can be programmed in Frame 2 under Write Mode (see Figure IIA). These logic outputs have adequate current driving capability to sink/source milliamperes of load.

Users can also activate O₁ and O₂ in three different ways without affecting the wiper settings. They may do the following:

- Start, Slave Address Byte, Acknowledge, Instruction Byte with O₁ and O₂ specified, Acknowledge, Stop.
- Complete the write cycle with Stop, then Start, Slave Address Byte, Acknowledge, Instruction Byte with O₁ and O₂ specified, Acknowledge, Stop.

REV. PrE 1/23/03

- Do not complete the write cycle by not issuing the Stop, then Start, Slave Address Byte, Acknowledge, Instruction Byte with O₁ and O₂ specified, Acknowledge, Stop.

SELF-CONTAINED SHUTDOWN FUNCTION

Shutdown can be activated by strobing the $\overline{\text{SHDN}}$ pin or programming the SD bit in the Write Mode Instruction Byte. In addition, Shutdown can even be implemented with the device digital output as shown in Figure 5. In this configuration, the device will be shutdown during power up, but users are allowed to program the device. Thus when O₁ is programmed high, the device will exit from the shutdown mode and respond to the new setting. This self-contained shutdown function allows absolute shutdown during power up, which is crucial in hazardous environment, without adding extra components.

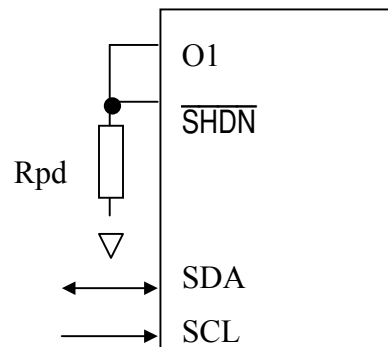


Figure 5. Shutdown by internal logic output

MULTIPLE DEVICES ON ONE BUS

Figure 8 shows four AD5263 devices on the same serial bus. Each has a different slave address since the state of their AD0 and AD1 pins are different. This allows each RDAC within each device to be written to or read from independently. The master device output bus line drivers are open-drain pull downs in a fully I²C compatible interface.

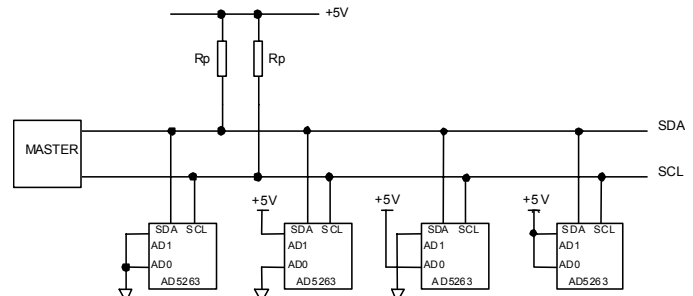


Figure 8. Multiple AD5263 Devices on One I²C Bus

LEVEL SHIFT FOR BI-DIRECTIONAL INTERFACE

While most old systems may be operated at one voltage, a new component may be optimized at another. When two systems operate the same signal at two different voltages, proper level shifting is needed. For instance, one can use a 3.3V E²PROM to interface with a 5V digital potentiometer. A level shift scheme is needed in order to enable a bi-directional communication so that the setting of the digital potentiometer can be stored to and retrieved from the E²PROM. Figure 7 shows one of the implementations. M1 and M2 can be any N-Ch signal FETs or low threshold FDV301N if V_{DD} falls below 2.5V.

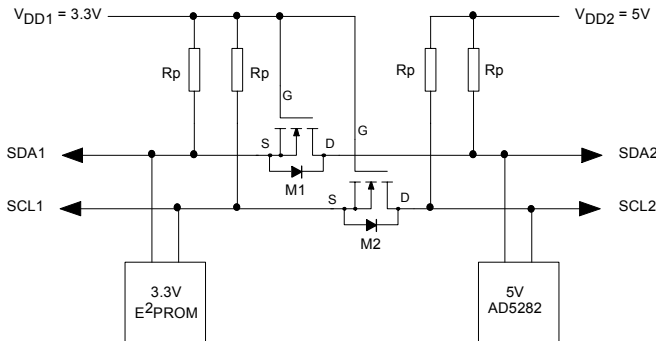


Figure 9. Level Shift for different potential operation

LEVEL SHIFT FOR NEGATIVE VOLTAGE OPERATION

The digital potentiometer is popular in laser diode driver and certain telecommunication equipment level setting applications. These applications are sometimes operated between ground and some negative supply voltage such that the systems can be biased at ground to avoid large bypass capacitors which may significantly impede the ac performance. Like most digital potentiometers, AD5263 can be configured with a negative supply (see Figure 10).

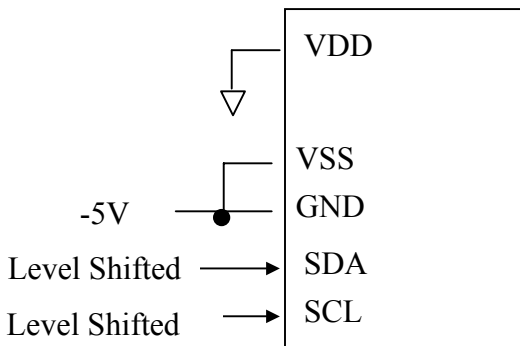


Figure 10. Biased at Negative Voltage

However, the digital inputs must also be level shifted to allow proper operation since the ground is now referenced to the negative potential. As a result, Figure 11 shows one implementation with a few transistors and a few resistors. When V_{IN} is below Q3's threshold value, Q3 is off, Q1 is off, and Q2 is on. In this state, V_{out} approaches 0V. When V_{IN} is above 2V, Q3 is on, Q1 is on, and Q2 is turned off. In this state V_{OUT} is pulled down to V_{ss}. Beware that proper time shifting is also needed for successful communication with the device.

REV. PrE 1/23/03

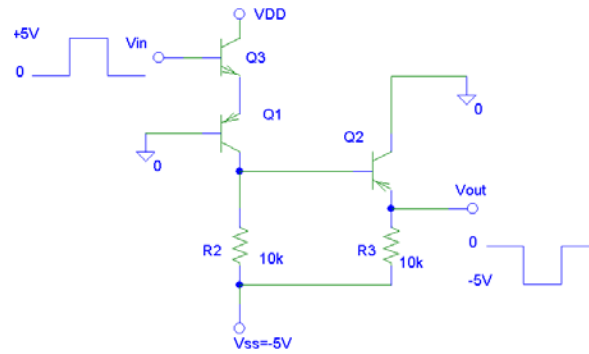


Figure 11. Level Shift for bi-polar potential operation

ESD PROTECTION

All digital inputs are protected with a series input resistor and parallel Zener ESD structures shown in Figure 12. Applies to digital input pins, SDI/SDA, CLK/SCL, $\overline{CS}/\overline{AD0}$ and \overline{SHDN} .

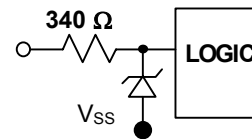


Figure 12a. ESD Protection of digital pins

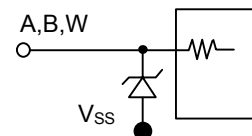


Figure 12b. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The AD5263 positive V_{DD} and negative V_{SS} power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed V_{DD} or V_{SS} will be clamped by the internal forward biased diodes (see Figure 13).

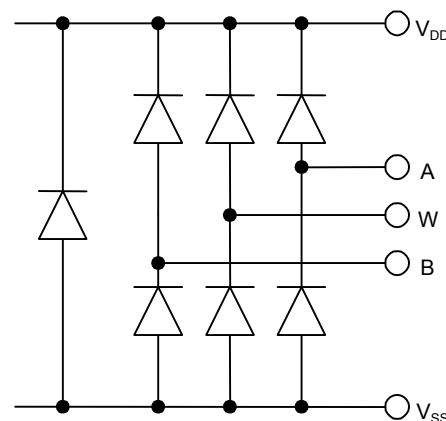


Figure 13. Maximum Terminal Voltages Set by V_{DD} & V_{SS}

POWER UP SEQUENCE

Since there are ESD protection diodes that limit the voltage compliance at terminals A, B, and W (see Figure 13), it is important to power V_{DD}/V_{SS} first before applying any voltage to terminals A, B, and W. Otherwise, the diode will be forward biased such that V_{DD}/V_{SS} will be powered unintentionally and may affect the rest of the user's circuit. The ideal power up sequence is in the following order: GND, V_{DD} , V_{SS} , digital inputs, and $V_{A/B/W}$. The order of powering V_A , V_B , V_W , and digital inputs is not important as long as they are powered after V_{DD}/V_{SS} .

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum-lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 μ F-0.1 μ F disc or chip ceramics capacitors. Low-ESR 1 μ F to 10 μ F tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 14). Notice the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

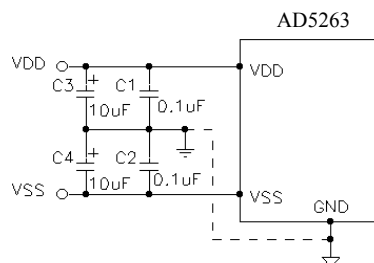


Figure 14. Power Supply Bypassing

V_{LOGIC} POWER SUPPLY

The AD5263 is capable of operating at high voltages beyond the internal logic levels, which are limited to operate at 5V. As a result, V_L needs to be tied to a separate 2.7 to 5.5V source to ensure proper digital signal levels.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

24-Lead Thin Surface Mount TSSOP Package (RU-24)

