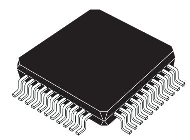
TDA7310

SERIAL BUS CONTROLLED AUDIO PROCESSOR

- INPUT MULTIPLEXER:
  - 4 STEREO INPUTS
  - ONE DIFFERENTIAL STEREO INPUT FOR REMOTE SOURCES
- SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTION TO DIFFERENT SOURCES
- INPUT AND OUTPUT FOR EXTERNAL EQUALIZER OR NOISE REDUCTION SYSTEM
- VOLUME CONTROL IN 1.25dB STEPS
- LOUDNESS FUNCTION
- TREBLE AND BASS CONTROL
- FOUR SPEAKER ATTENUATORS:
  - 4 INDEPENDENT SPEAKERS CONTROL IN 1.25dB STEPS FOR BALANCE AND FADER FACILITIES
  - INDEPENDENT MUTE FUNCTION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS
- SELECTABLE CHIP ADDRESS DEDICATED PIN



PQFP44 (10 x 10)

ORDERING NUMBER: TDA7310

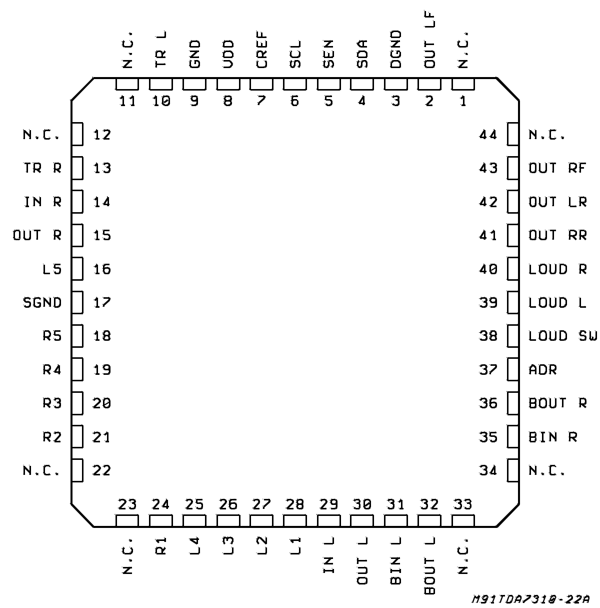
DESCRIPTION

The TDA7310 is a volume, tone (bass and treble) and fader (front/rear) processor for high quality audio applications in car radio and Hi-Fi systems.

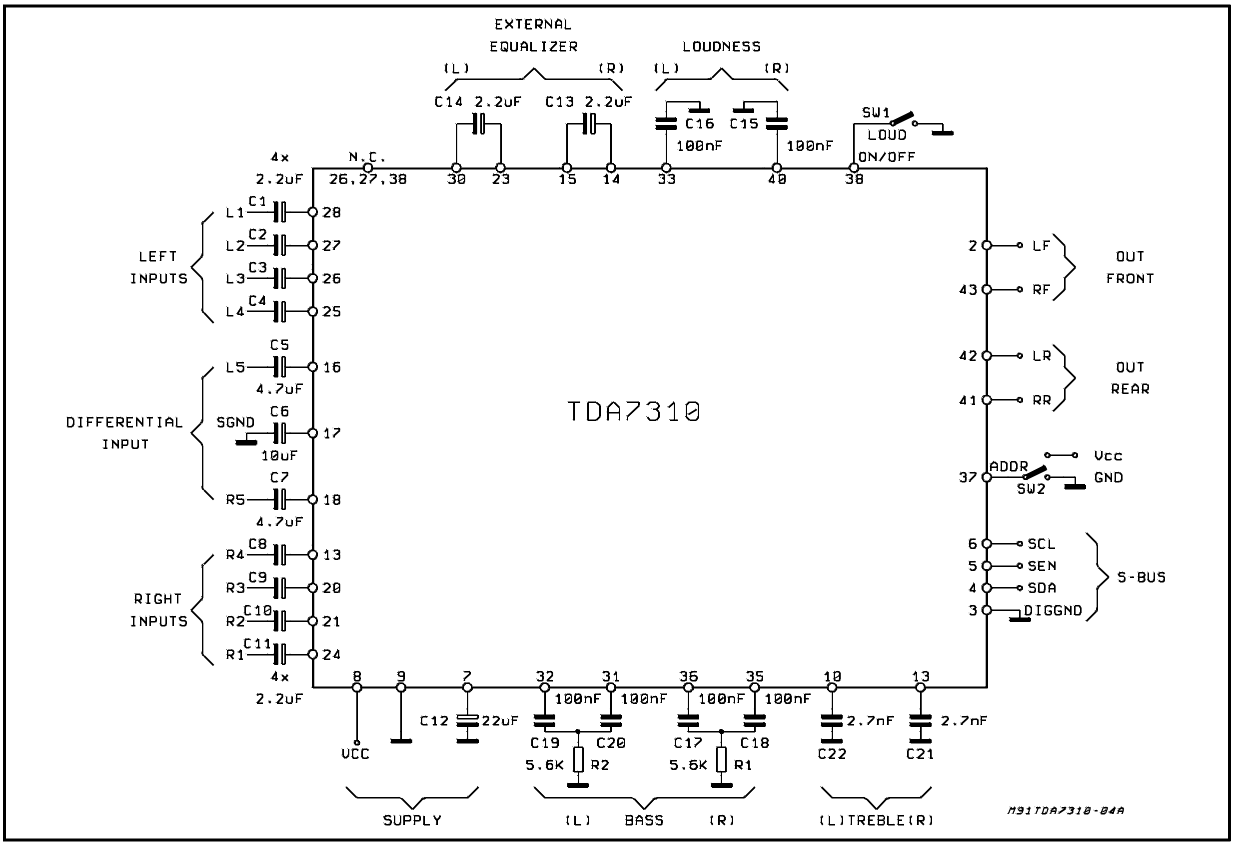
Loudness and selectable input gain are provided. The control of all fuctions is accomplished by serial bus microprocessor interface.
The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

Thanks to the used BIPOLAR/CMOS Tecnology, Low Distortion, Low Noise and DC stepping are obtained.

PIN CONNECTION (Top view)



TEST CIRCUIT



THERMAL DATA

Symbol	Description	Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins max	85	°C/W

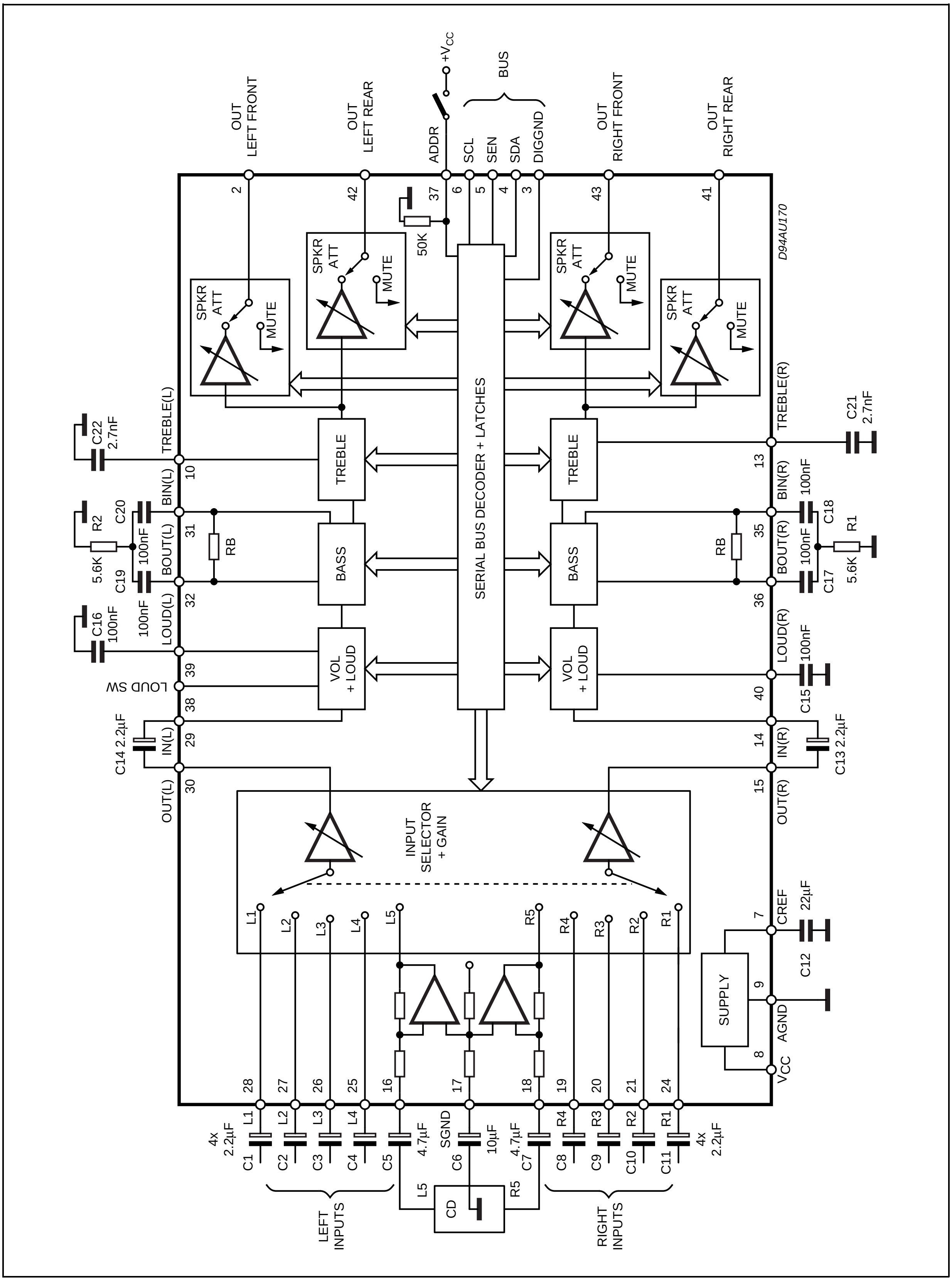
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.2	V
T_{amb}	Ambient Temperature	-40 to 85	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	6	9	10	V
V_{CL}	Max. input signal handling	2			Vrms
THD	Total Harmonic Distortion V = 1Vrms f = 1KHz		0.01		%
S/N	Signal to Noise Ratio		106		dB
S_C	Channel Separation f = 1KHz		103		dB
	Volume Control 1.25dB step	-78.75		0	dB
	Bass and Treble Control 2dB step	-14		+14	dB
	Fader and Balance Control 1.25dB step	-38.75		0	dB
	Input Gain 6.25dB step	0		18.75	dB
	Mute Attenuation		100		dB

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 9V, R_L = 10KΩ, R_G = 600Ω, G_V=0dB, f = 1KHz unless otherwise specified) (refer to the test circuit)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		6	9	10	V
I_S	Supply Current		4	8	11	mA
SVR	Ripple Rejection		60	85		dB
INPUT SELECTORS						
R_{II}	Input Resistance	Input 1, 2, 3, 4		50		KΩ
		Differential Input		10		KΩ
V_{CL}	Clipping Level		2	2.5		Vrms
CMRR	Common Mode Rejection Differential Input			65		dB
INS	Input Separation (2)		80	100		dB
R_L	Output Load resistance		2			KΩ
G_{INmin}	Min. Input Gain		-1	0	1	dB
G_{INmax}	Max. Input Gain			18.75		dB
G_{STEP}	Step Resolution			6.25		dB
e_{IN}	Input Noise	G = 18.75dB		2		µV
V_{DC}	DC Steps	adjacent gain steps		4		mV
		G = 18.75 to Mute		4		mV
VOLUME CONTROL						
R_{IN}	Input Resistance			33		kΩ
C_{RANGE}	Control Range			75		dB
A_{VMIN}	Min. Attenuation		-1	0	1	dB
A_{VMAX}	Max. Attenuation			75		dB
A_{STEP}	Step Resolution			1.25		dB
E_A	Attenuation Set Error	A_V = 0 to -20dB A_V = -20 to -60dB	-1.25 -3	0	1.25 2	dB dB
E_T	Tracking Error				2	dB
V_{DC}	DC Steps	adjacent attenuation steps From 0dB to A_{Vmax}		0.1 0.5		mV mV
SPEAKER ATTENUATORS						
	Control Range			37.5		dB
	Step Resolution			1.25		dB
	Attenuation set error				1.5	dB
	Output Mute Attenuation		80	100		dB
	DC Steps	adjacent att. steps from 0 to mute		0 1		mV mV
BASS CONTROL (1)						
	Control Range			±14		dB
	Step Resolution			2		dB
R_B	Internal Feedback Resistance			50		KΩ
V_{DC}	DC Steps	adjacent control steps		0.1		mV

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
TREBLE CONTROL (1)						
	Control Range			±14		dB
	Step Resolution			2		dB
V_{DC}	DC Steps	adjacent control steps		0.1		mV
AUDIO OUTPUTS						
	Clipping Level	d = 0.3%		2.5		Vrms
	Output Load Resistance		2			KΩ
	Output Load Capacitance				10	nF
	Output resistance			75	120	Ω
	DC Voltage Level		4.2	4.5	4.8	V
GENERAL						
e_{NO}	Output Noise	BW = 20-20KHz, flat output muted all gains = 0dB		 2.5 5	 15	 µV µV
S/N	Signal to Noise Ratio	all gains = 0dB; V_O = 1Vrms		106		dB
d	Distortion	V_{IN} = 1Vrms		0.01		%
Sc	Channel Separation left/right		80	103		dB
	Total Tracking error	A_V = 0 to -20dB -20 to -60 dB		0 0	1 2	dB dB
BUS INPUTS						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA			0.4	V
LOUDNESS SWITCH						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current		-5		+5	µA
	DC Step	ON ← → OFF position		0.1		mV

Loudness OFF = pin38 Open; Loudness ON = pin 38 Closed to GND

ADDRESS PIN (Internal 50KΩ pull down resistor)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		V_{CC} -1V			V
I_{IN}	Input Current					µA

Notes:

(1) Bass and Treble response see attached diagram (fig.17). The center frequency and quality of the resonance behaviour can be choosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network

(2) The selected input is grounded thru the 2.2µF capacitor.

APPLICATION SUGGESTION (see to Test circuit)

Component	Recc. Value	Purpose	Smaller than Recc. Value	Larger than
C1 to C4, C8 to C11	2.2µF	THD optimization at low frequencies	Worse THD at very low frequencies	
C5, C7 C6	4.7µF 10µF	CMRR optimization differential input	Worse CMRR for ratio not equal to ½	
C12	22µF	C_{REF} • SVR optimization < -66 dB	Better SVR at low frequencies	Worse SVR at low frequencies
C13, C14	2.2µF	Decoupling Input-Output if external equalizer is not used		
C15, C16	100nF	Loudness characteristic		
C17, C18 R1 C!9, C20 R2	100nF 5.6kΩ 100nF 5.6kΩ	Bass Filter (standard T - type) cut freq. = 100Hz		
C21 C22	2.7nF	Treble Filter	Higher cut frequency	Lower cut frequency

Figure 1: Loudness versus Volume Attenuation

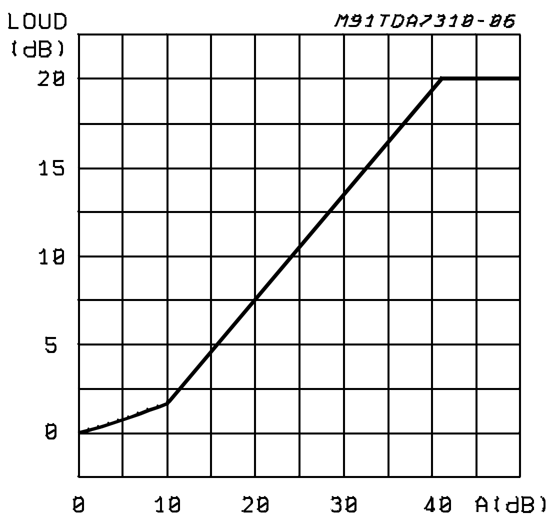


Figure 2: Loudness versus Frequency (C_{LOUD} = 100nF)

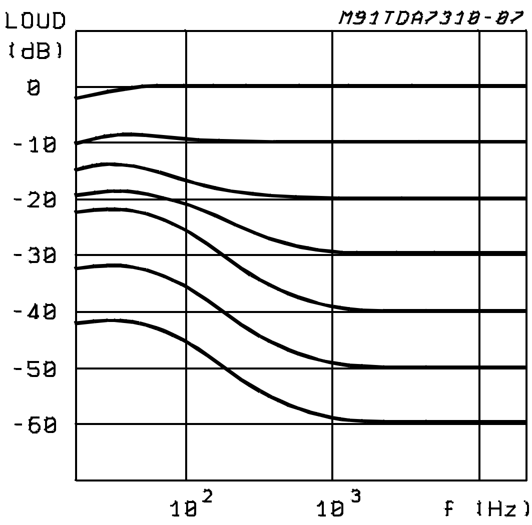
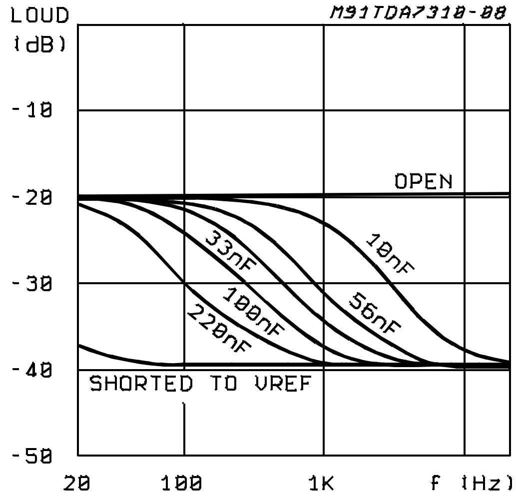


Figure 3: Loudness versus External Capacitors



LOUDNESS
V_S = 9V
Volume = -40dB
All other control flat
C_{in} = 2.2µF

Figure 4: Noise vs. Volume/Gain Settings

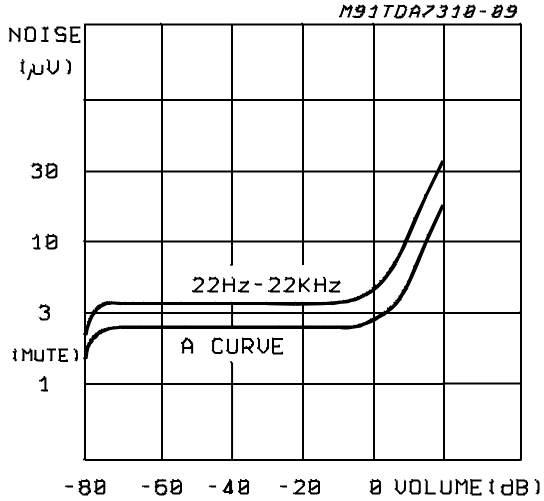


Figure 5: Signal to Noise Ratio vs. Volume Setting

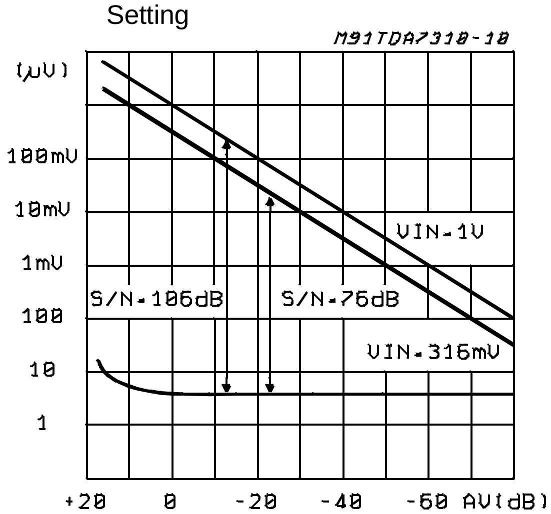


Figure 6: Distortion vs. Load Resistance

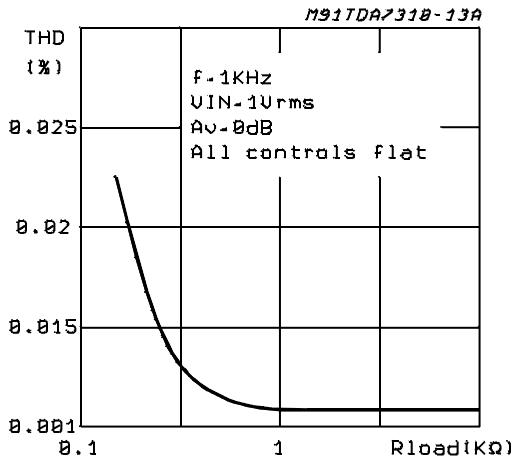


Figure 7 : Channel Separation (L → R) vs. Frequency

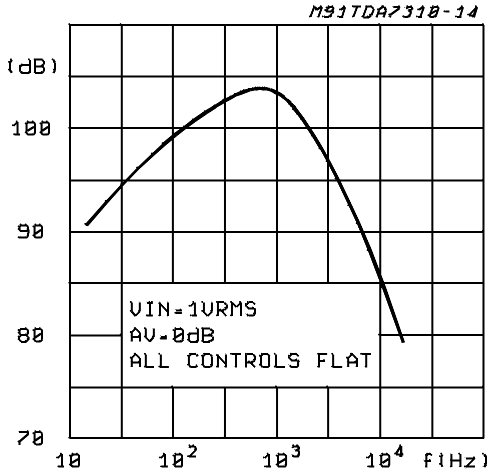


Figure 8 : Input Separation (L1 → L2, L3, L4) vs. Frequency

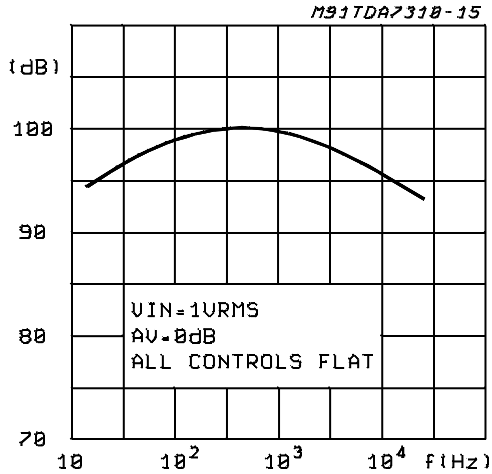


Figure 9 : Supply Voltage Rejection vs. Frequency

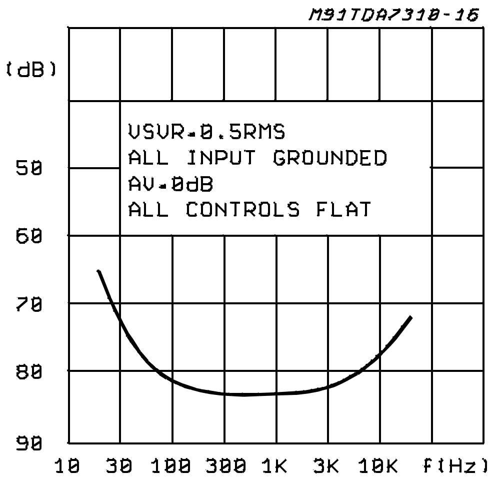


Figure 10: Output Clipping Level vs. Supply Voltage

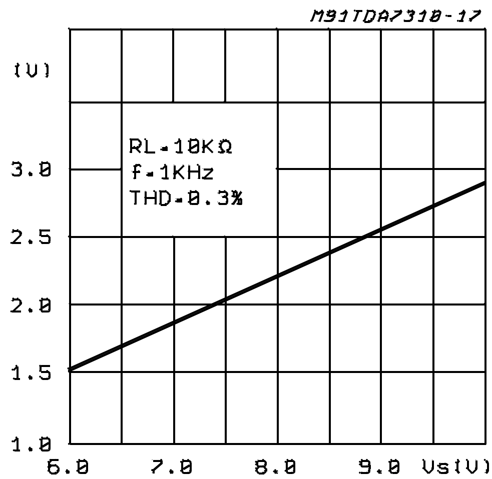


Figure 11: Quiescent Current vs. Supply Voltage

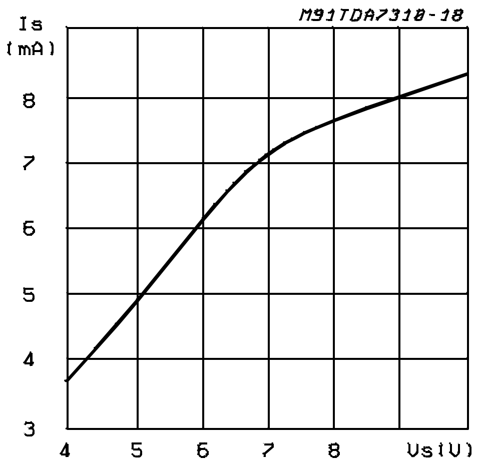


Figure 12: Supply Current vs. Temperature

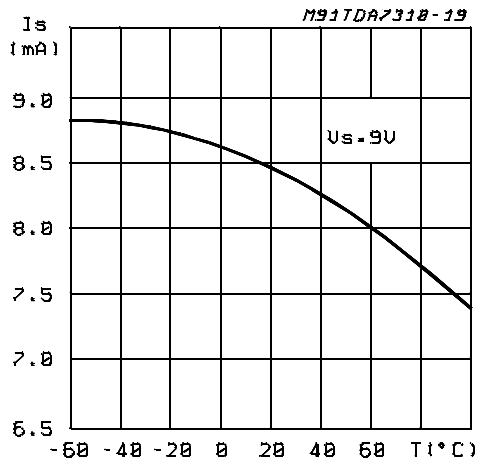


Figure 13: Bass Resistance vs. Temperature

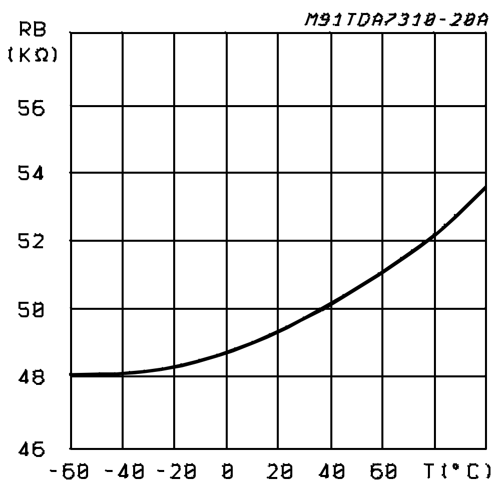
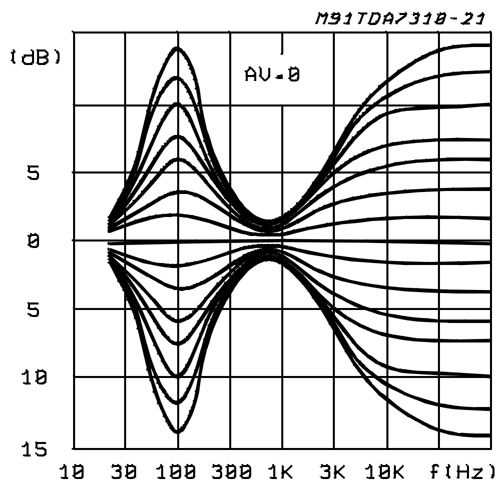


Figure 14: Typical Tone Response (with the ext. components indicated in the test circuit)



APPLICATION INFORMATION (continued)

SERIAL BUS INTERFACE

S-BUS Interface and I^{2}CBUS Compability

Data transmission from microprocessor to the TDA7310 and viceversa takes place thru the 3-wire S-BUS interface, consisting of the three lines SDA, SCL, SEN. If SDA and SEN inputs are short-circuited together, then the TDA7310 appears as a standard I^{2}CBUS slave.
According to I^{2}CBUS specification the S-BUS lines are connected to a positive supply voltage via pull-up resistors.

Data Validity

As shown in fig. 15, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

I^{2}CBUS:
as shown in fig. 16 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

S-bus:

the start/stop conditions (points 1 and 6) are detected exclusively by a transition of the SEN line (1 $\rightarrow$ 0 / 0 $\rightarrow$ 1)wile the SCL line is at the HIGH level.
The SDA line is only allowed to change during the time the SCL line is low (points 2, 3, 4, 5). after the start information (point 1) the SEN line returns to the HIGH level and remains uncharged for all the time the transmission is performed.

Byte Fornat

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 17). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock.

Figure 15: Data Validity on the I^{2}CBUS

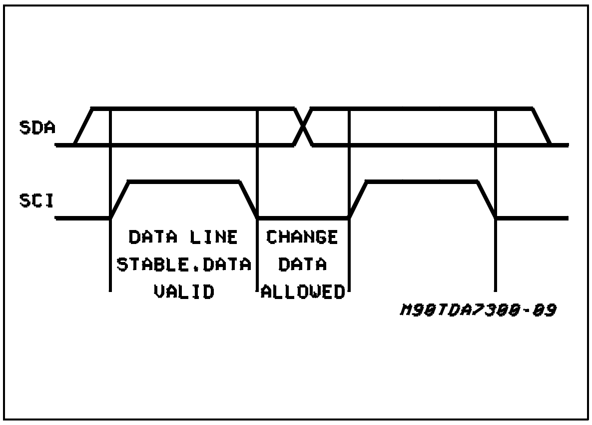


Figure 16: Timing Diagram of S-BUS and I^{2}CBUS

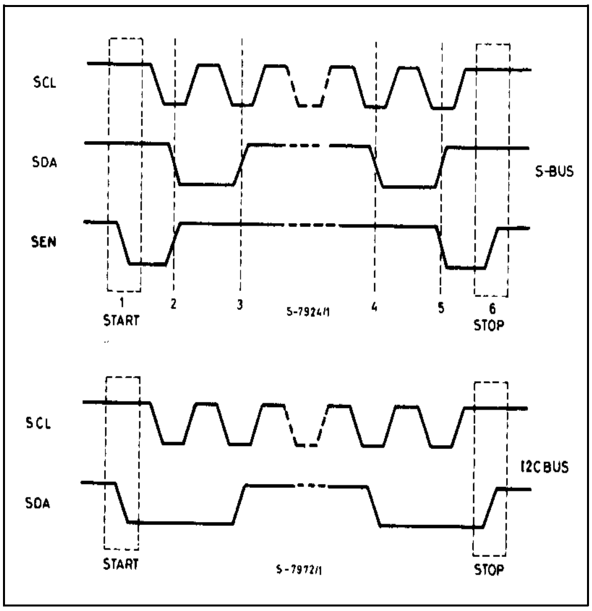
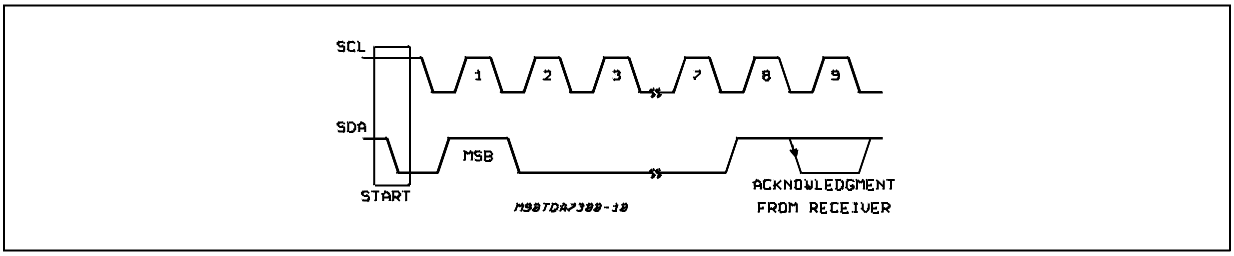


Figure 17: Acknowledge on the I^{2}CBUS



APPLICATION INFORMATION (continued)

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Transmission without Acknowledge

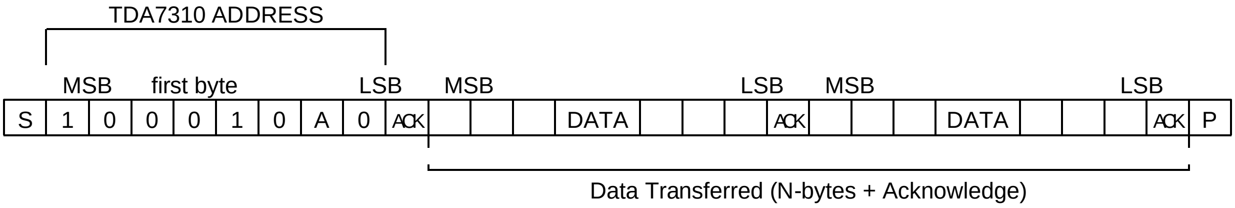
Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

Interface Protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte, containing the TDA7310 address (the 8th bit of the byte must be 0). The TDA7310 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge
S = Start
P = Stop

MAX CLOCK SPEED 100kbits/s

SOFTWARE SPECIFICATION

Chip address

1 MSB	0	0	0	1	0	A	0 LSB

A = LOGIC LEVEL ON PIN ADDR

DATA BYTES

MSB							LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Volume control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	G1	G0	S2	S1	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

Ax = 1.25dB steps; Bx = 10dB steps; Cx = 2dB steps; Gx = 6.25dB steps

STATUS AFTER POWER ON RESET

Volume	-77.5dB
speaker	-37.5dB
audio Switch	Stereo 5
bass	+2dB
treble	+2dB
gain	0dB

SOFTWARE SPECIFICATION (continued)

DATA BYTES (detailed description)

Volume

MSB							LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Volume 1.25dB steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

For example a volume of -45dB is given by:

0 0 1 0 0 1 0 0

Speaker Attenuators

MSB							LSB	FUNCTION
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	Mute

For example attenuation of 25dB on speaker RF is given by:

1 0 1 1 0 1 0 0

Audio Switch

MSB							LSB	FUNCTION
0	1	0	G1	G0	S2	S1	S0	Audio Switch
					0	0	0	Stereo 1
					0	0	1	Stereo 2
					0	1	0	Stereo 3
					0	1	1	Stereo 4
					1	0	0	Stereo 5
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
			0	0				+18.75dB
			0	1				+12.5dB
			1	0				+6.25dB
			1	1				0dB

For example to select the stereo 2 input with a gain of +12.5dB the 8bit string is:

0 1 0 0 1 0 0 1

Bass and Treble

0 0	1 1	1 1	0 1	C3 C3	C2 C2	C1 C1	C0 C0	Bass Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

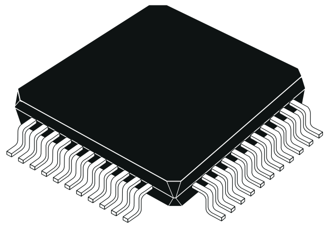
C3 = Sign

For example Bass at -10dB is obtained by the following 8 bit string:

0 1 1 0 0 0 1 0

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.45			0.096
A1	0.25			0.010		
A2	1.95	2.00	2.10	0.077	0.079	0.083
B	0.30		0.45	0.012		0.018
c	0.13		0.23	0.005		0.009
D	12.95	13.20	13.45	0.51	0.52	0.53
D1	9.90	10.00	10.10	0.390	0.394	0.398
D3		8.00			0.315	
e		0.80			0.031	
E	12.95	13.20	13.45	0.510	0.520	0.530
E1	9.90	10.00	10.10	0.390	0.394	0.398
E3		8.00			0.315	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



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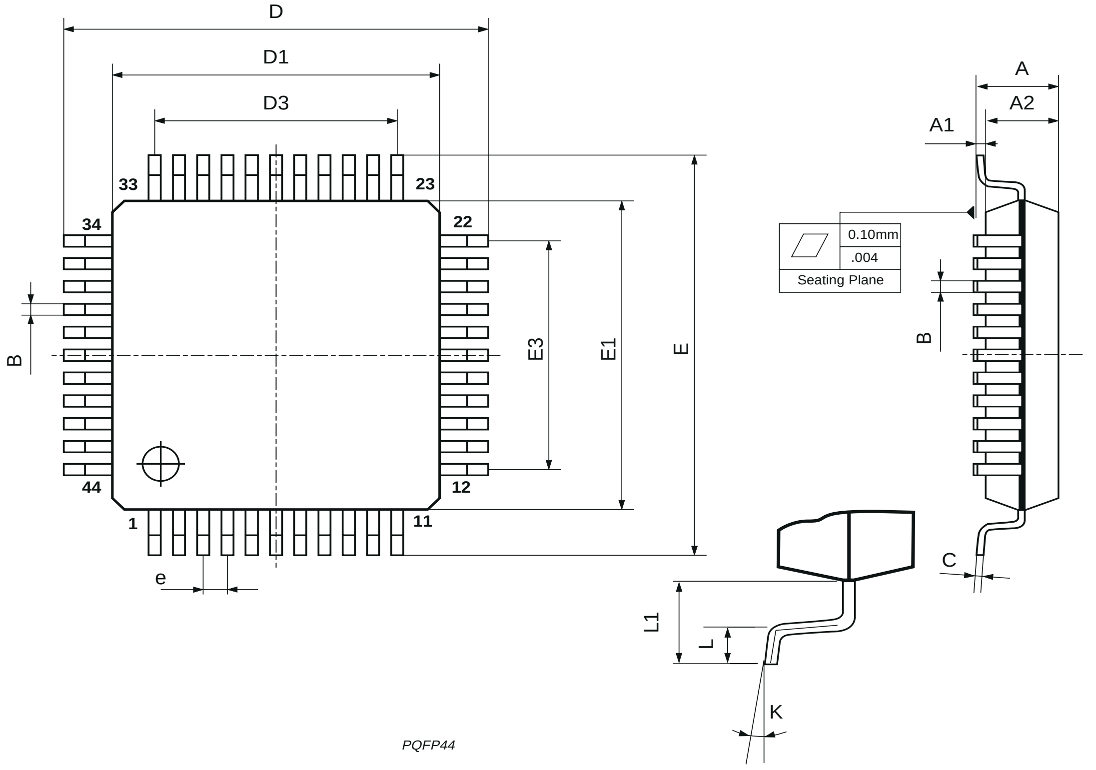

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