SONY

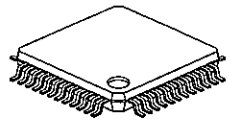
CXA1208R/Q

8mm VTR Color Signal Processing

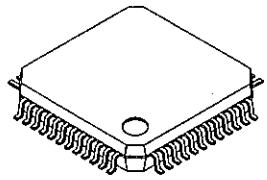
Description

The CXA1208R/Q is a consumer IC developed for 8mm VTR color signal processing. Usage in combination with CXA1207A allows for processing of Y/C main signals.

CXA1208R
48 pin LQFP (Plastic)



CXA1208Q
48 pin QFP (Plastic)



Features

- Single 5V power supply
- Formation of chroma feedback comb filter possible through combination with CXA1207A
- No adjustment VCO
- NTSC/PAL correspondence
- Low power consumption (145mW at REC, 150mW at PB)

Functions

ACC, chroma emphasis/deemphasis, burst emphasis/deemphasis, XO/VXO, APC, AFC, APCID, AFCID, BID, ACK, APC compensation, HHK, PI/PS, frequency conversion system, chrome mute, 4.2V regulator.

Structure

Bipolar silicon monolithic IC

Operating Condition

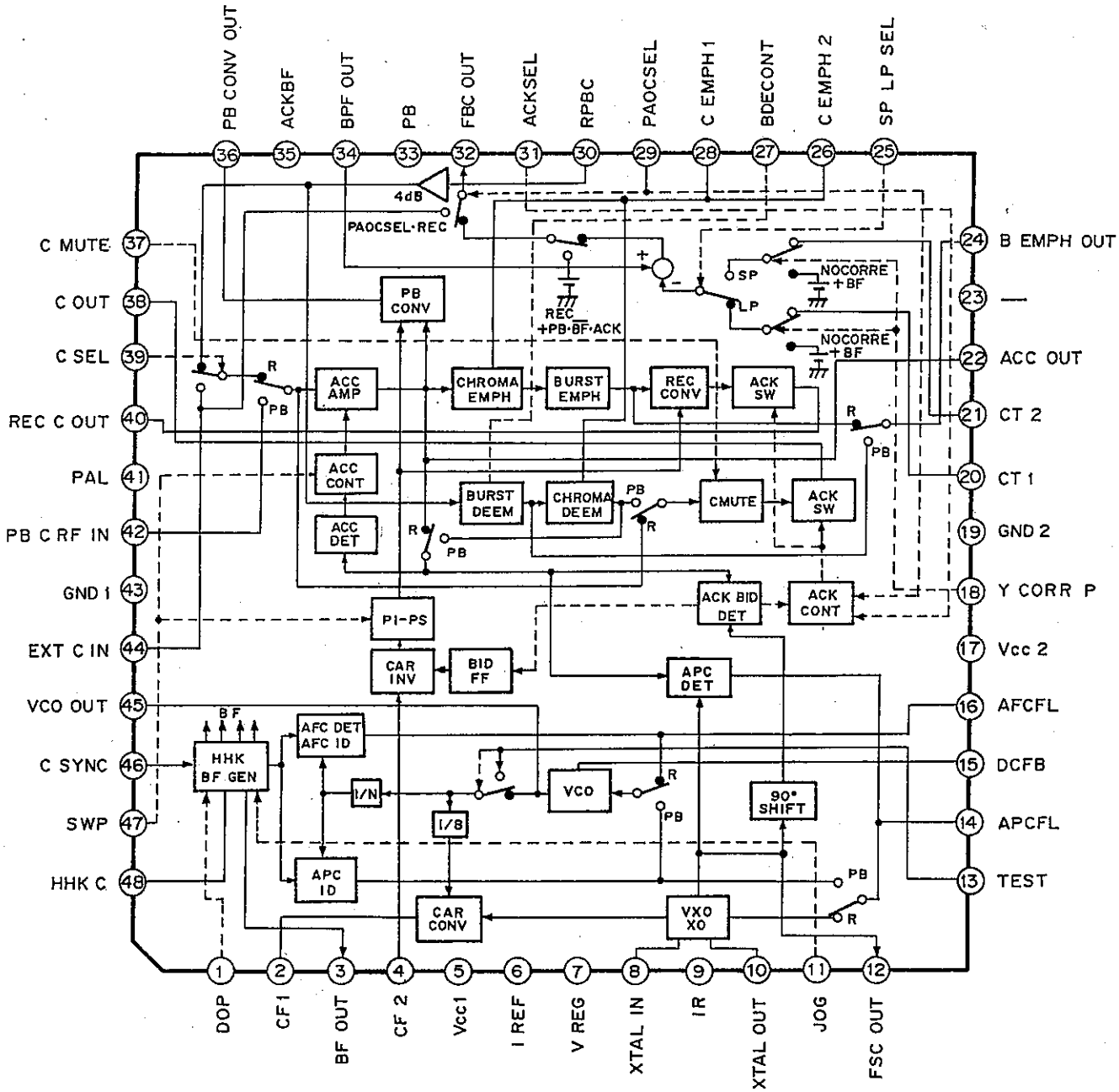
Supply voltage	Vcc	4.75 to 5.25	V

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	Vcc	7	V	
• Operating temperature	Topr	−10 to +75	°C	
• Storage temperature	Tstg	−55 to +150	°C	
• Allowable power dissipation	PD (CXA1208R)	1100	mW	(When mounted on the board)
	PD (CXA1208Q)	920	mW	(When mounted on the board)

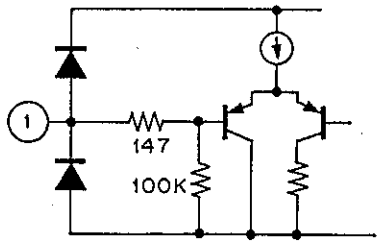
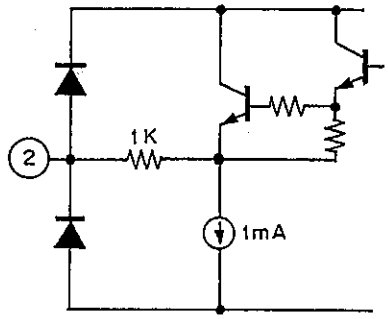
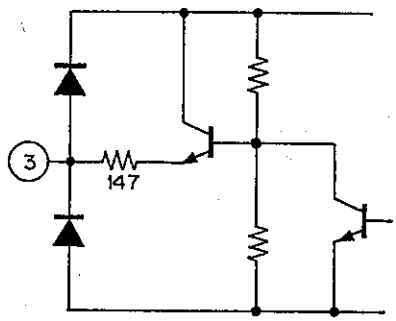
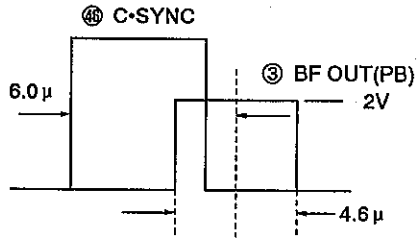
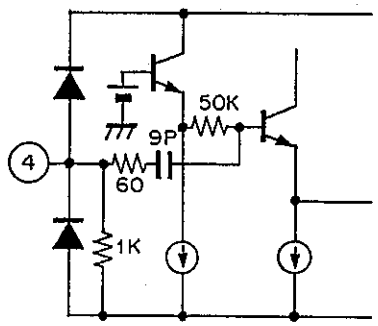
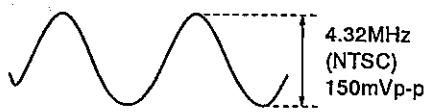
E90109B4X

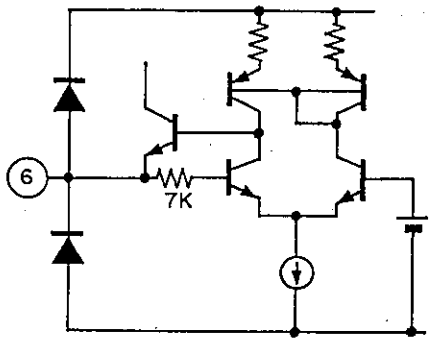
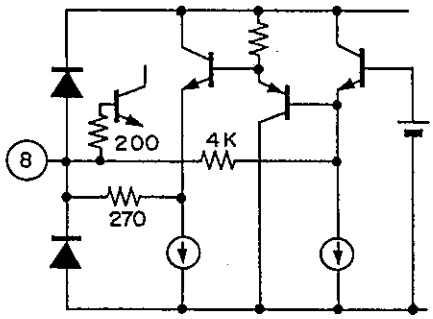
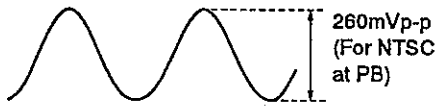
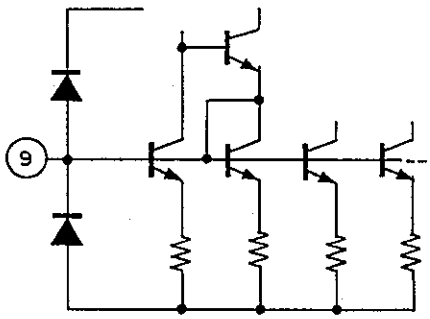
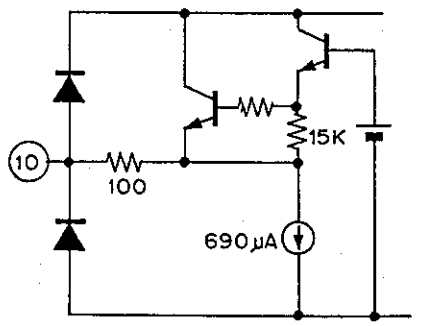
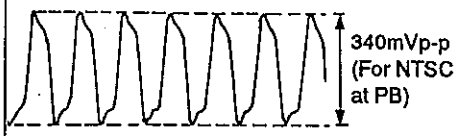
Block Diagram and Pin Configuration

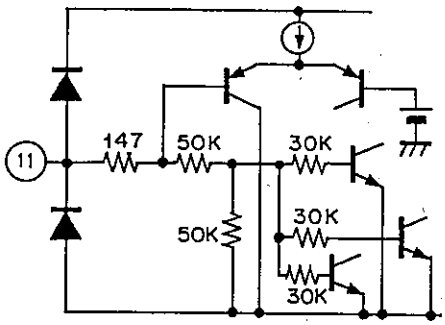
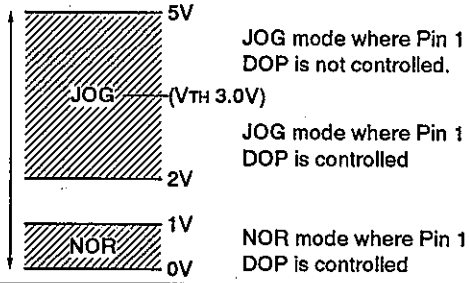
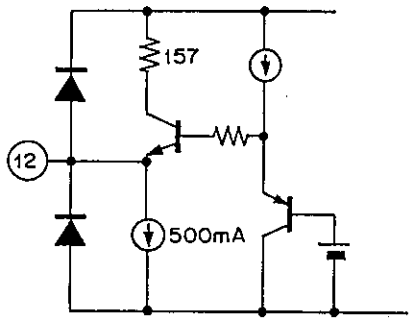
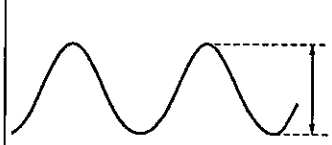
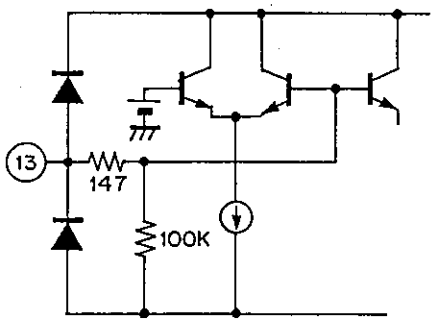
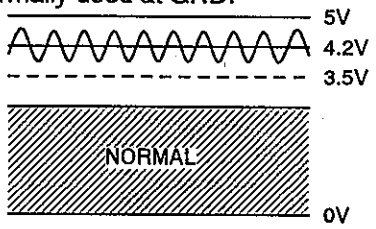
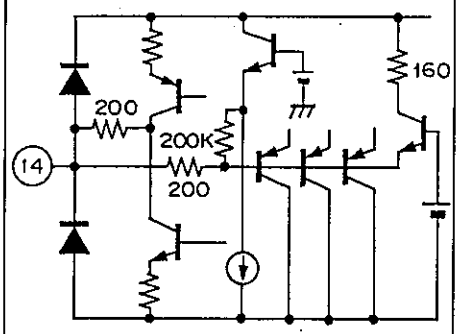


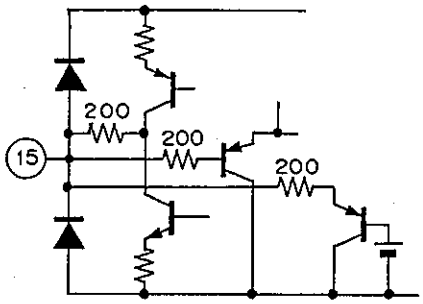
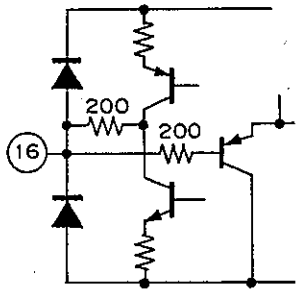
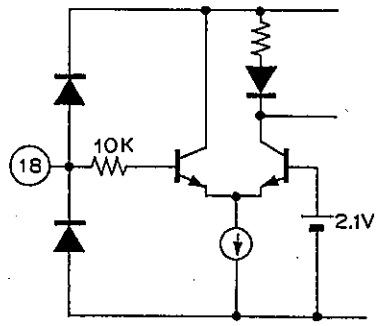
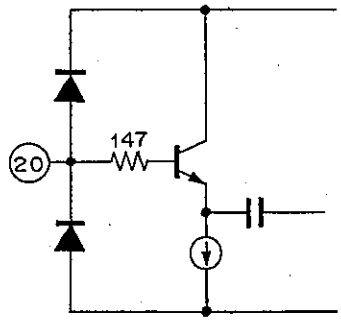
Pin Description

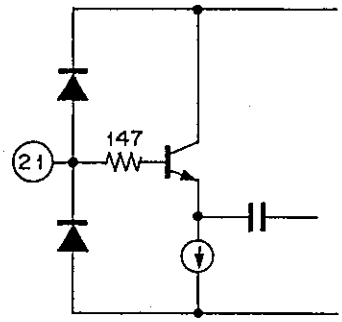
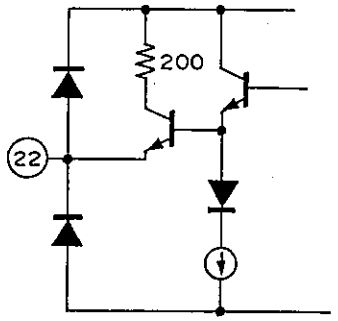
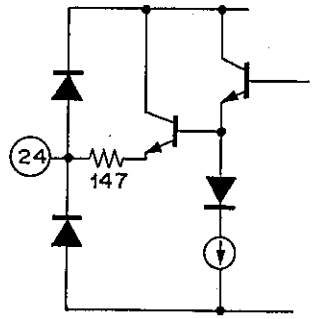
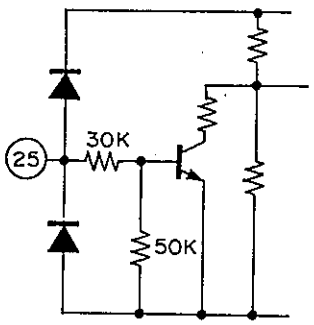
(Vcc=5.0V, Ta=25°C)

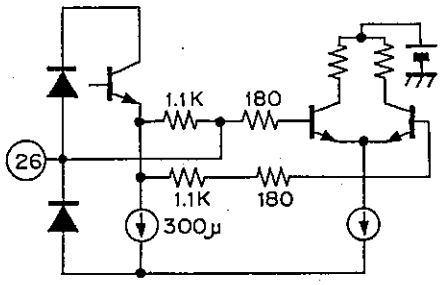
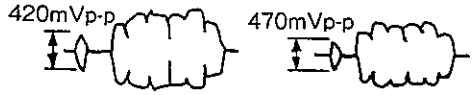
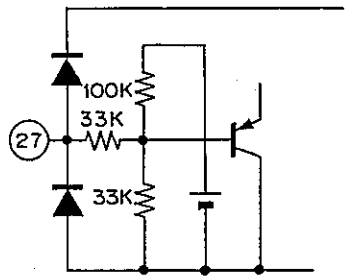
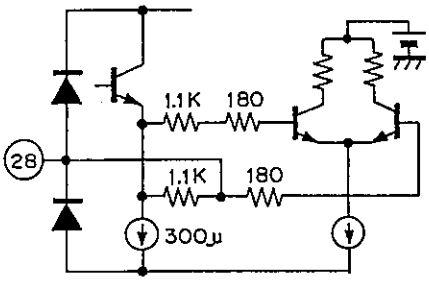
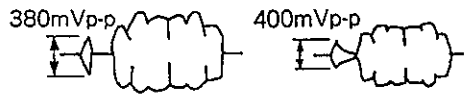
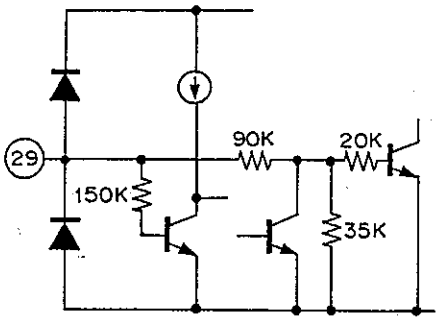
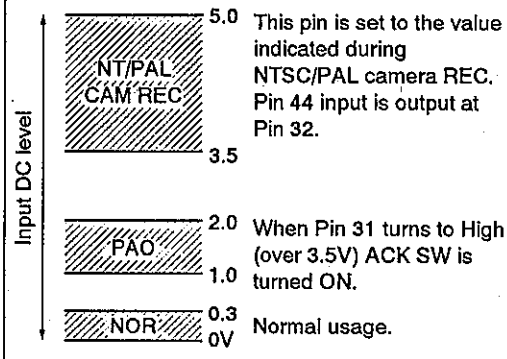
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	DOP	0V		Drop out detection pulse is input. V_{TH} is at 2.1V. (V_{MIN}=2.5V) When a drop out detection pulse of Pin 11 (JOG) is input below 3.0V, the APC and ACC systems burst gate is turned off and the error is held.
2	CF1	2.5V		Carrier converter signal output pin. The spurious factor of (fsc+fcL) and (fsc–fcL) is contained. 
3	BF OUT	2.0/0V (When resistance applied)		When a resistance (3.3kΩ) is applied to GND, the burst flag is output. There is no output in the vertical sync period. 
4	CF2	0V		Pin 2 output filtrated through BPF (4.32MHz for NTSC and 5.17MHz for PAL). The standard input level is at 150mVp-p. 
5	Vcc1	5.0V		Power supply pin of sync block.

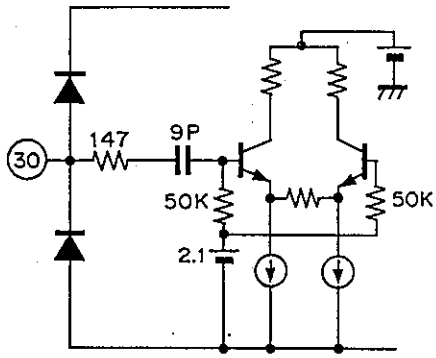
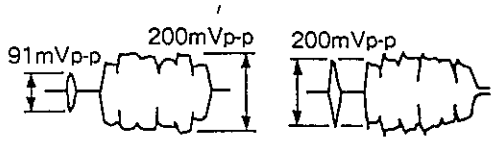
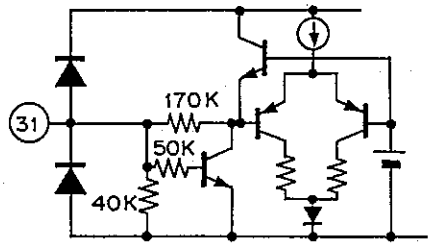
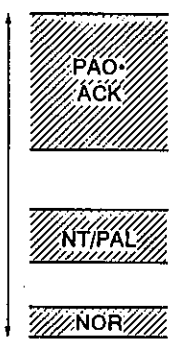
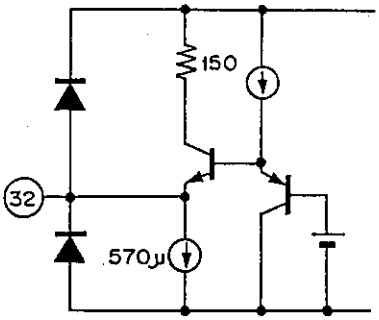
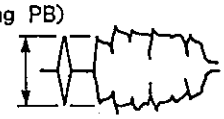
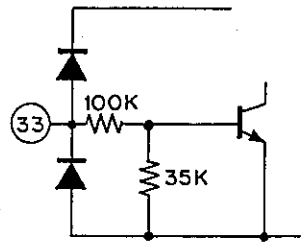
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
6	IREF	2.1V		A 100kΩ resistance is inserted to GND. This is the external reference current pin that produces the reference current. $I_{REF}=\frac{V_6}{100K}\simeq 21\ \mu A$ Watch for pin interference.
7	VREG	4.2V	—	4.2V regulator output pin
8	XTAL IN	2.1V		X'tal OSC reference input pin. Also, X'tal connecting pin. Watch for pin interference, floating capacitance. (PB) 
9	IR	0.9V		Decoupling pin
10	XTAL OUT	3.4V		X'tal OSC reference output pin. Connects a X'tal between this pin and Pin 8. 

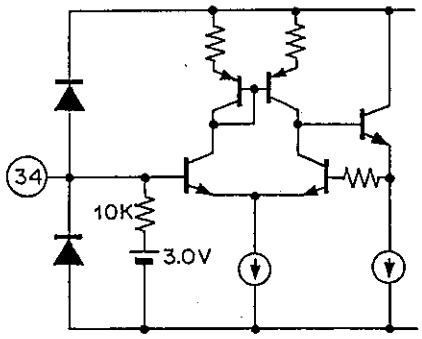
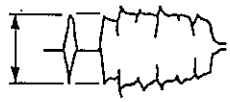
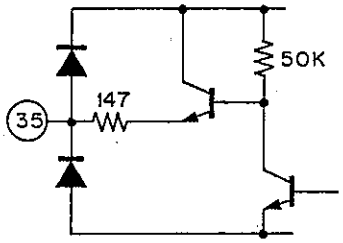
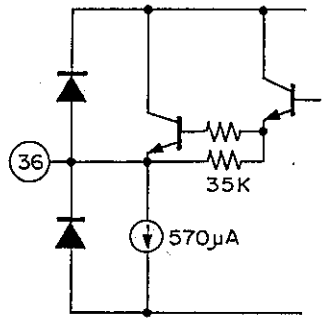
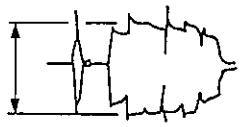
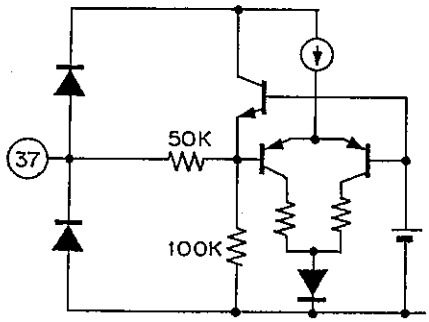
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
11	JOG	0V		Control pin during JOG PB. When JOG mode is turned on, it switches to high speed ACC and raises the APC loop gain. Whether to turn off APC and ACC blocks burst flag with this pin's DC value, can be selected at Pin 1 (DOP).  JOG mode where Pin 1 DOP is not controlled. JOG mode where Pin 1 DOP is controlled NOR mode where Pin 1 DOP is controlled
12	FSC OUT	2.3V		VXO/XO outputs pass through LPF before being output from this pin. At the same time, this fsc is used for the clock frequency of the CCD delay line.  (NTSC) 3.58MHz 460mVp-p (PAL) 4.43MHz 420mVp-p
13	TEST	0V		Turns to test mode with an external DC of 3.5 to 5.0V. At 4.2V DC center, input to the frequency divider is possible instead of VCO output. Normally used at GND. 
14	APC FL	2.4V		Connecting pin of external filter for APC.

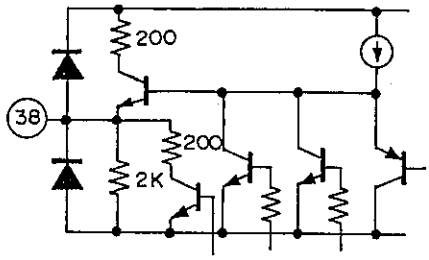
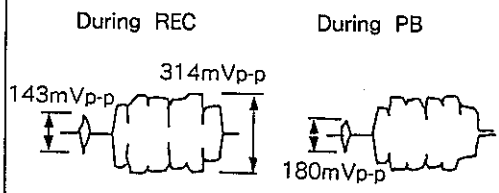
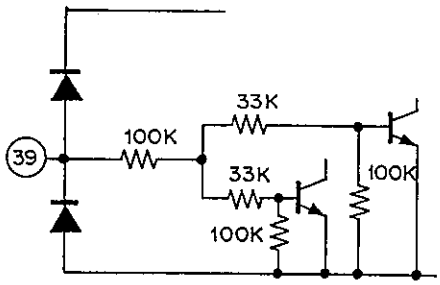
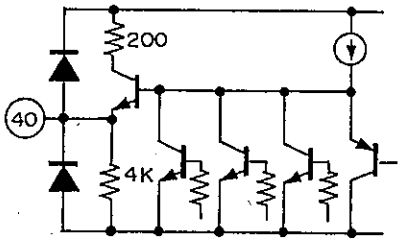
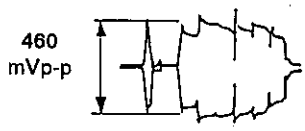
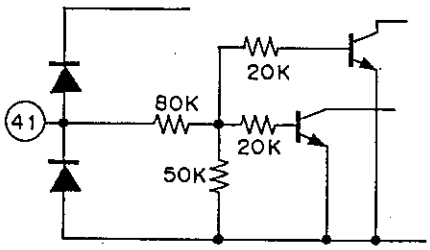
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
15	DCFB	2.4V		Connecting pin of external filter for no adjustment VCO.
16	AFC FL	2.4V (During REC)		Connecting pin of external filter for AFC.
17	Vcc2	5.0V	—	Power supply pin of main signal processing block.
18	Y CORR P	—		Input pin of the Y signal H correlation pulse from CXA1207A. At V_{TH}=2.1V, sets the chroma feedback comb filter to feedback ON at High (2.5V Min.) and to feedback OFF at Low (1.0V Max.).
19	GND2	0V	—	GND pin of main signal processing block.
20	CT1	—		When SP LP SEL (Pin 25) is at Low (LP), this pin becomes the input pin of the crosstalk (C+C_D) from CXA1207A.

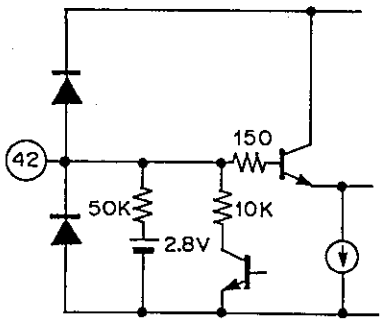
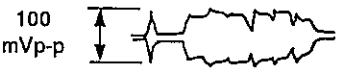
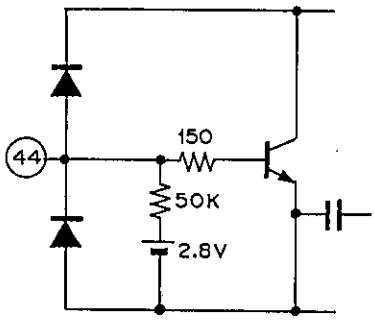
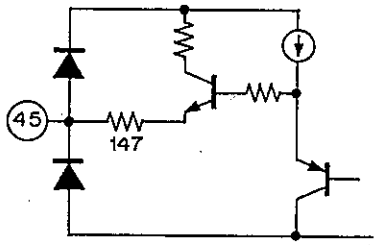
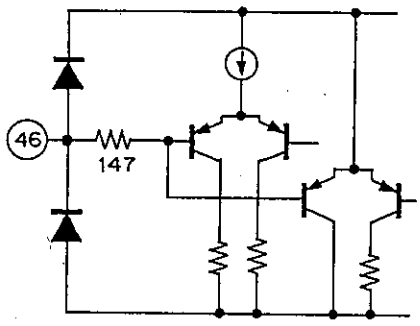
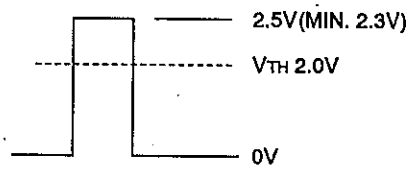
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
21	CT2	—		When SP LP SEL (Pin 25) is at High (SP), this pin becomes the input pin of the crosstalk (C+CD) from CXA1207A.
22	ACC OUT	2.0V (When resistance is applied)		When a resistance (3.3kΩ) is applied to GND, ACC AMP output can monitor. During REC 143 mVp-p 314mVp-p (75 % color bar) During PB 380mVp-p (75 % color bar)
23	—	—	—	Use in open condition.
24	B EMPH OUT	2.0V (When resistance is applied)		When a resistance (3.3kΩ) is applied to GND, the signal can be monitored after chroma emphasis and burst emphasis during REC, or after burst deemphasis during PB. During REC During PB 340mVp-p 200mVp-p (75 % color bar) NTSC
25	SP LP SEL	0V		SP/LP select control pin. At High (3.5V Min.) selects CT2 (Pin 21) input signal (SP) and at Low (0.5V Max.) CT1 (Pin 20) input signal (LP) to form a chroma feedback comb filter.

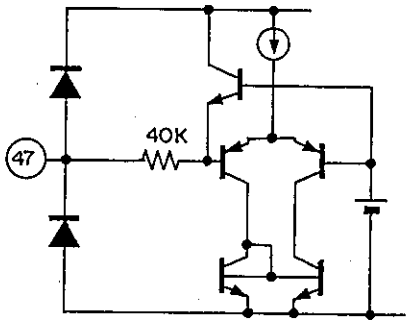
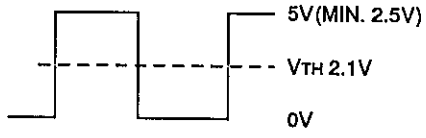
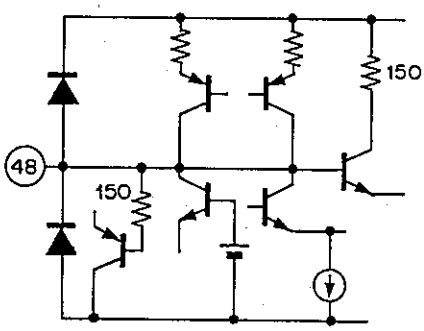
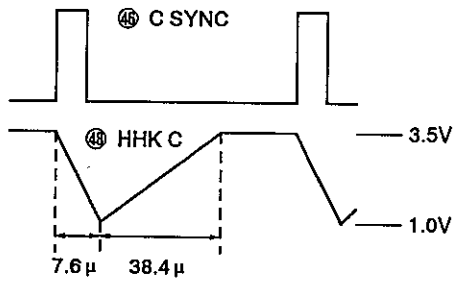
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
26	C EMPH 2	2.4V		Connects a coil for chroma emphasis phase matching between this pin and C EMPH 1 (Pin 28). During REC During PB  (75 % color bar) NTSC
27	B DE CONT	1.0V		Adjusts burst deemphasis volume during PB. Can adjust the saturation of PB chroma signals. Normally kept open for use.
28	C EMPH 1	2.4V		Connecting pin of chroma emphasis BPF. During REC During PB  (75 % color bar) NTSC
29	PAO C SEL	0V		 This pin is set to the value indicated during NTSC/PAL camera REC. Pin 44 input is output at Pin 32. When Pin 31 turns to High (over 3.5V) ACK SW is turned ON. Normal usage.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
30	R PB C	—		Input pin of the chroma signal after passage through the chroma comb filter. During REC, with C SEL (Pin 39) at Low, the input signal of this pin is processed. During REC During PB  (75% color bar) NTSC
31	ACK SEL	0.4V		This pin selects ACK SW mode.  As Pin 29 turns to PAO (1.0 to 2.0V), ACK SW turns to ON. NTSC/PAL signals are processed without ACK SW being activated. ACK SW turns to ON/OFF according to ACK DET output.
32	FBC OUT	3.0V 1.3V (During PAOCSEL. REC)		Output pin for chroma signals to process comb filter. During PB and the formation of chroma feedback comb filter, (main signal ⊖ crosstalk) signals are output. (However during ACK, only burst signals are output.) Also, during REC, PAO C SEL (Pin 29) is at High and EXT C IN (Pin 44) input signals are output. (During PB) 250 mVp-p  NTSC (75% color bar)
33	PB	0V		REC/PB modes select pin. At High (3.5V Min.) : PB mode At Low (1.0V Max.) : REC mode

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
34	BPF OUT	3.0V		Input pin for signals passed through the external BPF (fo=3.58MHz) after frequency conversion during PB. 130 mVp-p  NTSC (75% color bar)
35	ACK • BF	4.3/0V (When resistance is applied)		During ACK, BF pulse is output. In CXA1207A it is used for the replacement of the pedestal level. Output amplitude level becomes 4.3/0V. (When 10kΩ applied) However during V sync period it is not output.
36	PB CONV OUT	2.8V (During PB)		Frequency converted chroma signals are output during PB. After that they are input to BPF (fo=3.58MHz). 990 mVp-p  NTSC (75% color bar)
37	C MUTE	1.0V		Select pin to mute color signals. With V_{TH}=2.1V, At High (2.6V Min.) : Mute is ON At Low (1.6V Max.) : Mute is OFF.

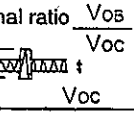
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
38	C OUT	2.1V		Output pin for chroma signals during PB. Also, during REC, chroma input signals selected by C SEL (Pin 39), are output. During ACK, output DC turns to 0V.  (75% color bar)
39	C SEL	0V		During REC, this pin selects the input pin for chroma signals. At High (3.5V Min.) EXTC IN (Pin 44) input At Low (1.0V Max.) RPBC (Pin 30) input are selected.
40	REC C OUT	2.3V		During REC, burst emphasis, chroma emphasis and frequency converted chroma signals are output. During ACK output DC turns to 0V.  NTSC (75% color bar)
41	PAL	0V		Select pin for PAL signals processing. At High (3.5V Min.) turns to PAL mode. At Low (1.0V Max.) turns to NTSC mode.

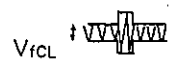
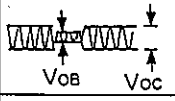
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
42	PB C RF IN	2.8V (During PB)		During PB, chroma RF signals are input. Typical input level is at 100mVp-p.  (75% color bar)
43	GND1	0V	—	GND pin for sync block.
44	EXT C IN	2.8V		During REC, chroma signals are input. Typical level during 75% color bar input is at 314mVp-p. Input possible when C SEL (Pin 39) at High. 
45	VCO OUT	2.8/2.2V (When resistance is applied)		Output pin of 378f_H (NTSC) : 5.9MHz. To output it is necessary to apply a 10kΩ resistance to GND. Normally use as Vcc. 
46	C SYNC	—		Composite sync input pin. 

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
47	SWP	2.0V		RF SW pulse input pin. Used for ACC DET time constant and PI • PS selection. 
48	HHK C	3.5/1.0V		Connecting pin of the charge/discharge capacitor for masking that turns C SYNC equivalent pulse to Half H Killer. 

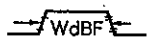
Electrical Characteristics

(Ta=25℃, Vcc=5V, See Electrical Characteristics Circuit)

No.	Test item		Symbol	Input conditions				SW set ON	Test point	Test method	Min.	Typ.	Max.	Unit37
				Signal	Input pin	Level	Frequency							
1	Current circuit 1 (REC)		$I_{CC\ REC}$						A	Current circuit during REC	21	29	37	mA
2	Current circuit 2 (PB)		$I_{CC\ PB}$					9	A	Current circuit during PB	22	30	38	mA
3	Internal reference voltage source 1		V_{REG}						4	Test DC voltage	4.05	4.2	4.35	V
4	Internal reference voltage source 2		ΔV_{REG-}						4	At Vcc=4.75V: $\Delta V_{REG-} = V_{REG1} - V_{REG}$	−6	−1	0	mV
5	Internal reference voltage source 3		ΔV_{REG+}						4	At Vcc=5.25V: $\Delta V_{REG+} = V_{REG2} - V_{REG}$	0	+1	+6	mV
6	Reference current source		I_{REF}						3	I_{REF}= (No.3 Pin voltage) /100K	20.25	21	21.75	μA
7	ACC AMP(1)	Gain	$G_{CENACC1}$	1	SG1	91 mVp-p	fsc	6	6	$\frac{V_6}{SG1}$	1.5	3.0	4.5	dB
		Secondary distortion	HD_{2ACC}	1	SG1	91 mVp-p	fsc	6	6	$\frac{V_6(2fsc)}{V_6(fsc)}$			−35	dB
		Max. gain	G_{MAXACC}	1	SG1	6 mVp-p	fsc	6	6	$\frac{V_6}{SG1}$	19	23		dB
		Min. gain	G_{MINACC}	1	SG1	400 mVp-p	fsc	6	6	$\frac{V_6}{SG1}$		−10	−8	dB
8	ACC AMP gain (2)		$G_{CENACC2}$	1	SG3	143 mVp-p	fsc	6, 10, 12	6	$\frac{V_6}{SG3}$	−2.8	−1.4	0	dB
9	C OUT level (REC)		$C_{OUT\ REC}$	1	SG3	143 mVp-p	fsc	10, 12	8	$\frac{V_8}{SG3}$	−1.1	0.4	1.9	dB
10	Gain difference between PB COUT and ACC CH	1ch output level	V_{O1CH}	1	SG2	100 mVp-p	f_{CL}	8, 9, 11	8	Output chroma level V_{O1CH} 	180	260	350	mVp-p
		Gain difference	ΔG_{CH}	5	SG2	100 mVp-p	f_{CL}	8, 9, 11, 14	8	Test gain difference between respective channels	−0.5	0	0.5	dB
11	High speed ACC suppress ratio		$F_{ACC\ (JOG)}$	2	SG1	—	—	3, 6	6	See details 1 on Test method			−6	dB
12	Burst emphasis characteristics		BE	1	SG1	91 mVp-p	fsc	7	7	V_7 chroma burst signal ratio $\frac{V_{O5}}{V_{OC}}$  V_{O5} V_{OC}	4.8	5.8	6.8	dB

No.	Test item		Symbol	Input conditions				SW set ON	Test point	Test method	Min.	Typ.	Max.	Unit
				Signal	Input pin	Level	Frequency							
13	Chroma emphasis characteristics	Output level (1)	CE 0dB (fsc)	3	SG1	Vc= 200 mVp-p (0dB)	fsc	7	7	Chroma output level V_{70}(fsc)	250	340	450	mVp-p
		Emphasis characteristics (1)	CE 0dB (500K)				fsc+ 500kHz			$\frac{V_{70}(fsc+500K)}{V_{70}(fsc)}$	− 1.4	0.7	2.6	dB
		Emphasis characteristics (2)	CE 0dB (− 500K)				fsc − 500kHz			$\frac{V_{70}(fsc-500K)}{V_{70}(fsc)}$	− 1.4	0.7	2.6	dB
		Output level (2)	CE − 10dB (fsc)			Vc= 63.2 mVp-p (− 10dB)	fsc			Chroma output level V_{71}(fsc)	80	108	150	mVp-p
		Emphasis characteristics (3)	CE − 10dB (500K)				fsc+ 500kHz			$\frac{V_{71}(fsc+500K)}{V_{71}(fsc)}$	1.4	3.2	5.4	dB
		Emphasis characteristics (4)	CE − 10dB (− 500K)				fsc − 500kHz			$\frac{V_{71}(fsc-500K)}{V_{71}(fsc)}$	1.4	3.2	5.4	dB
14	REC C RF output level		V_{fCL}	1	SG1	91 mVp-p	fsc		10	Chroma output level 	80	110	140	mVp-p
15	REC C RF DC	ACK OFF	DC ACK OFF	1	SG1	12 mVp-p	fsc		9	Test output DC level	1.9	2.2	2.5	V
		ACK ON	DC ACK ON	1	SG1	1 mVp-p	fsc		9	Test output DC level			100	mV
16	Burst deemphasis		BDE	1	SG1	200 mVp-p	fsc	7, 9	7	V_7 chroma burst signal ratio $\frac{V_{OB}}{V_{OC}}$ 	− 5.4	− 4.4	− 3.4	dB
17	Carrier converter output level		V_{CAR}	1	SG1	91 mVp-p	fsc		2	Test output level	110	150	190	mVp-p
18	XO characteristics (NTSC)	Frequency deviation	Δ fxo					9	5	Δ fxo=fsc − fxo	− 50		50	Hz
		Output level	Vxo					9	5	Test output level	360	460	560	mVp-p
		Secondary distortion	HD2xo					9	5	$\frac{V_5(2fsc)}{V_5(fsc)}$			− 25	dB
19	XO characteristics (PAL)	Frequency deviation	Δ fxoP					1, 9	5	Δ fxo= fscP − fxoP	− 50		50	Hz
		Output level	VxoP					1, 9	5	Test output level	320	420	520	mVp-p
		Secondary distortion	HD2xoP					1, 9	5	$\frac{V_5(2fscP)}{V_5(fscP)}$			− 25	dB

No.	Test item		Symbol	Input conditions				SW set ON	Test point	Test method	Min.	Typ.	Max.	Unit
				Signal	Input pin	Level	Frequency							
20	REC APC pull in range (NTSC)	Upper side frequency	Δ fvxo+	1	SG1	91 mVp-p	fsc + Δ Hz		5	SG1 (fsc+1kHz) Upper side frequency that can be pulled in within 2 sec from input time	230			Hz
		Lower side frequency	Δ fvxo −	1	SG1	91 mVp-p	fsc − Δ Hz		5	SG1 (fsc − 3kHz) Lower side frequency that can be pulled in within 2 sec from input time			− 230	Hz
21	REC APC pull in range (PAL)	Upper side frequency	Δ fvxo+	4	SG1	91 mVp-p	fscP + Δ Hz	1	5	SG1 (fscP+1kHz) Upper side frequency that can be pulled in within 2 sec from input time	200			Hz
		Lower side frequency	Δ fvxo —	4	SG1	91 mVp-p	fscP − Δ Hz	1	5	SG1 (fscP − 3kHz) Lower side frequency that can be pulled in within 2 sec from input time			− 200	Hz
22	VCO sensitivity 1 (DCFB)		fs vco1	DC	V1 V2	2.4V 1.6/3V	DC	4, 5, 9, 13	11	$\frac{f_{11}(3V) - f_{11}(1.6V)}{1.4}$	−1700	−1500	−1300	kHz/V
23	VCO sensitivity 2 (APCFL)		fs vco2	DC	V1 V2	1.6/3V 2.4V	DC	4, 5, 9, 13	11	$\frac{f_{11}(3V) - f_{11}(1.6V)}{1.4}$	200	300	400	kHz/V
24	PB APC VCO frequency (NTSC)	Upper side pull in	fvco+3%	1	SG2	100 mVp-p	1.03fCL	8, 9, 11, 13	11	f11: VCO oscillation frequency		6125979		Hz
				7	SG4		1.03fH							
		Lower side pull in	fvco − 3%	1	SG2	100 mVp-p	0.97 fCL	8, 9, 11, 13	11	f11: VCO oscillation frequency		5769126		Hz
				7	SG4		0.97fH							
25	PB APC VCO frequency (PAL)	Upper side pull in	fvco+3%	6	SG2	100 mVp-p	1.03fCLP	1, 8, 9, 11, 13	11	f11: VCO oscillation frequency		6035156		Hz
				7	SG4		1.03 fHP							
		Lower side pull in	fvco − 3%	6	SG2	100 mVpp	0.97 fCLP	1, 8, 9, 11, 13	11	f11: VCO oscillation frequency		5683594		Hz
				7	SG4		0.97 fHP							

No.	Test item		Symbol	Input conditions				SW set ON	Test point	Test method	Min.	Typ.	Max.	Unit
				Signal	Input pin	Level	Frequency							
26	REC AFC VCO frequency (NTSC)	Upper side pull in	fvco+3%	7	SG4		1.03 f_H	13	11	f_{11}: VCO oscillation frequency		6125979		Hz
		Lower side pull in	fvco − 3%	7	SG4		0.97 f_H	13	11	f_{11}: VCO oscillation frequency		5769126		Hz
27	REC AFC VCO frequency (PAL)	Upper side pull in	fvco+3%	7	SG4		1.03 f_{HP}	1, 13	11	f_{11}: VCO oscillation frequency		6035156		Hz
		Lower side pull in	fvco − 3%	7	SG4		0.97 f_{HP}	1, 13	11	f_{11}: VCO oscillation frequency		5683594		Hz
28	PI characteristics	Phase 1	PI_{180}	1	SG1	91 mVp-p	fsc	8, 9, 11	12	See details 2 on Test method		180		deg
		Phase 2	PI_0	1	SG1	91 mVp-p	fsc	8, 9, 11, 14	12	See details 2 on Test method		0		deg
29	Burst flag	Phase	Td_{BF}					2	1	㊻C・SYNC  ③BF OUT	3.4	4.0	4.6	μsec
		Width	Wd_{BF}					2	1	 	3.6	4.6	5.6	μsec

Note 1) Testing is performed with the input of 15.73426573kHz from SG4 to C SYNC (Pin 46) (when SW1 is OFF) for NTSC, and similarly the input of 15.625kHz (when SW1 is ON) for PAL. This excludes testing of T24, 25, 26 and 27.

Note 2) This IC specifications stipulate the following:

Chroma sub carrier waves for — fsc (NTSC) at 3579545.455Hz; f_{SCP} (PAL) at 4433618.75Hz

Carrier waves converted to low band — f_{CL} (NTSC) at 743444.059Hz; f_{CLP} (PAL) at 732421.875Hz

The respective relation of f_A=4.5MHz (NTSC) and f_{AP}=5.5MHz (PAL) turns out as follows.

(NTSC)

f_A=4.5MHz

$f_H = \frac{1}{286} f_A$

$f_{SC} = \frac{455}{2} f_H$

$f_{CL} = 47 \frac{1}{4} f_H$

$f_{VCO} = 378 f_H$

(PAL)

f_{AP}=5.5MHz

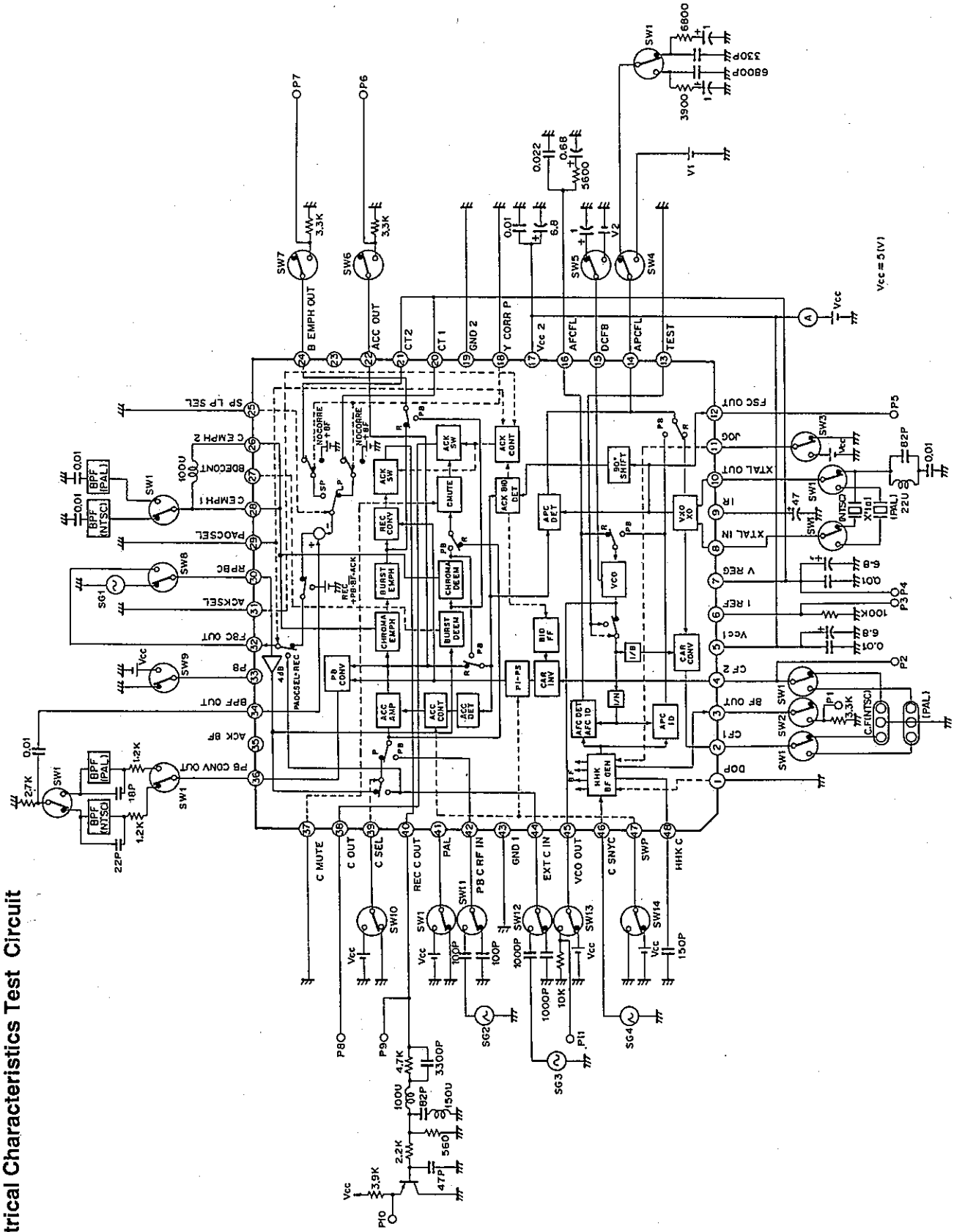
$f_{HP} = \frac{1}{352} f_{AP}$

$f_{SCP} = (284 - \frac{1}{4} + \frac{1}{625}) f_{HP}$

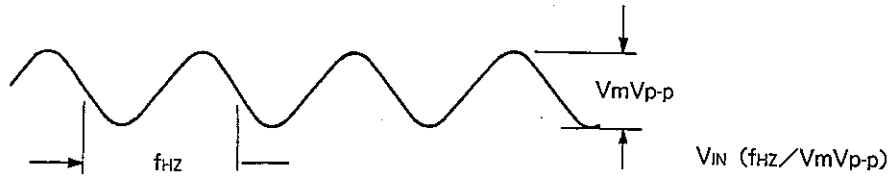
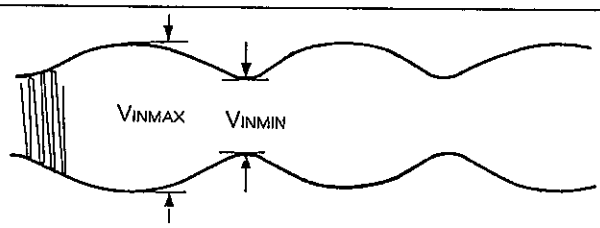
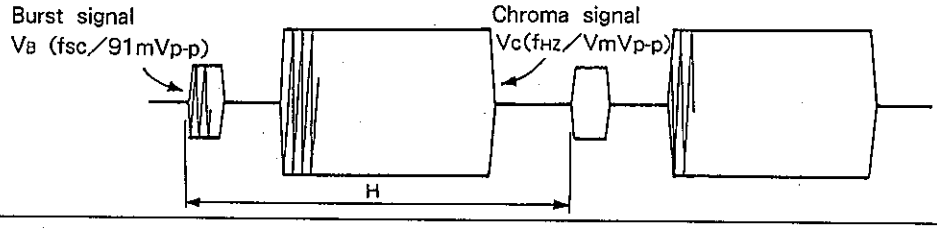
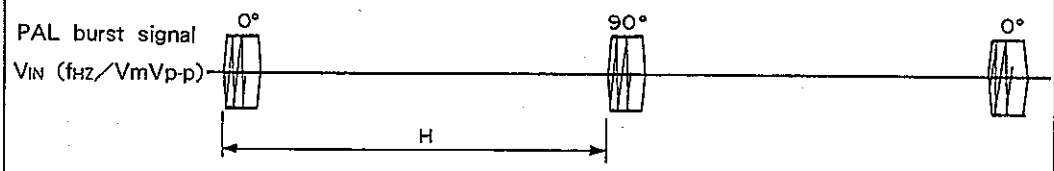
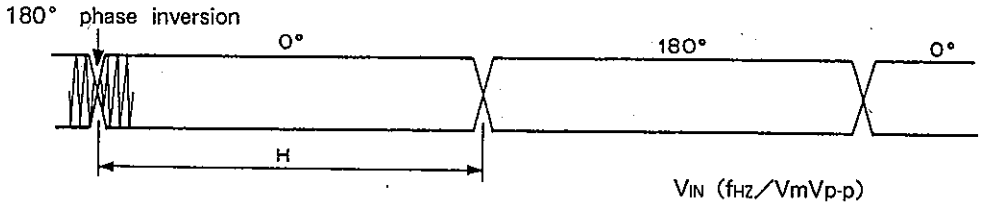
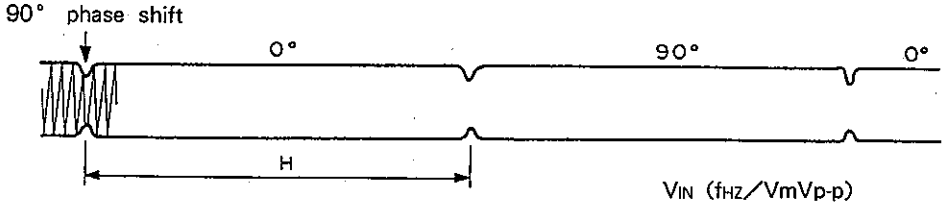
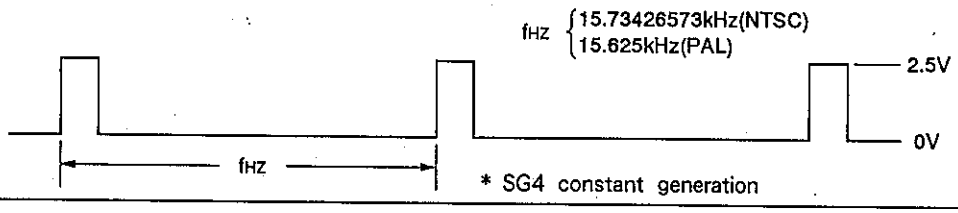
$f_{CLP} = 46 \frac{7}{8} f_{HP}$

$f_{VCOP} = 375 f_{HP}$

Electrical Characteristics Test Circuit

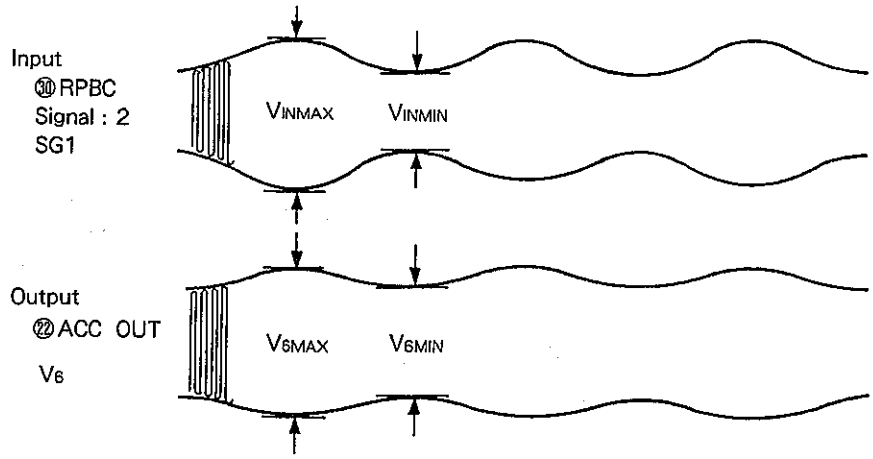


Input signal

Signal	Waveform	Signal source
1		SG1 SG2 SG3
2	 fsc/91mVp-p AM modulated to 60Hz, 35%. $\frac{V_{INMAX} - V_{INMIN}}{V_{INMAX} + V_{INMIN}} \times 100 = 35\%$	SG1
3		SG1
4		SG1
5		SG2
6		SG2
7		SG4

Test Method Details 1

Turning JOG pin (Pin 11) to High=5V (V_{TH}=1.4V) produces high speed ACC mode.

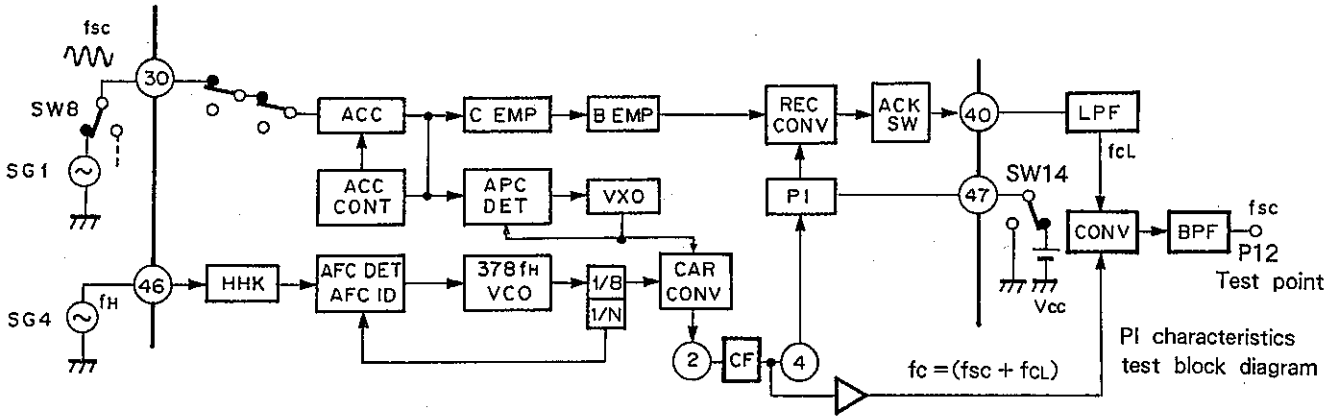


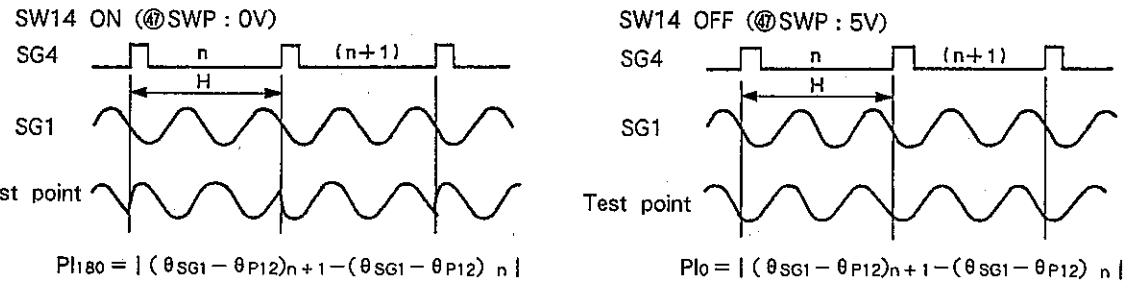
$$F_{ACC}\ (JOG)=20\log\ \frac{V_{6MAX}-V_{6MIN}}{V_{INMAX}-V_{INMIN}}$$

Test Method Details 2

Because of the chroma crosstalk cancel in NTSC mode, PI method is performed. By turning the SWP input through Pin 47 from High to Low (V_{TH}=2.1V), the following is obtained.

SWP { H (5V); PI OFF (Test P_{I0})
L (0V); PI ON (Test P_{I180})





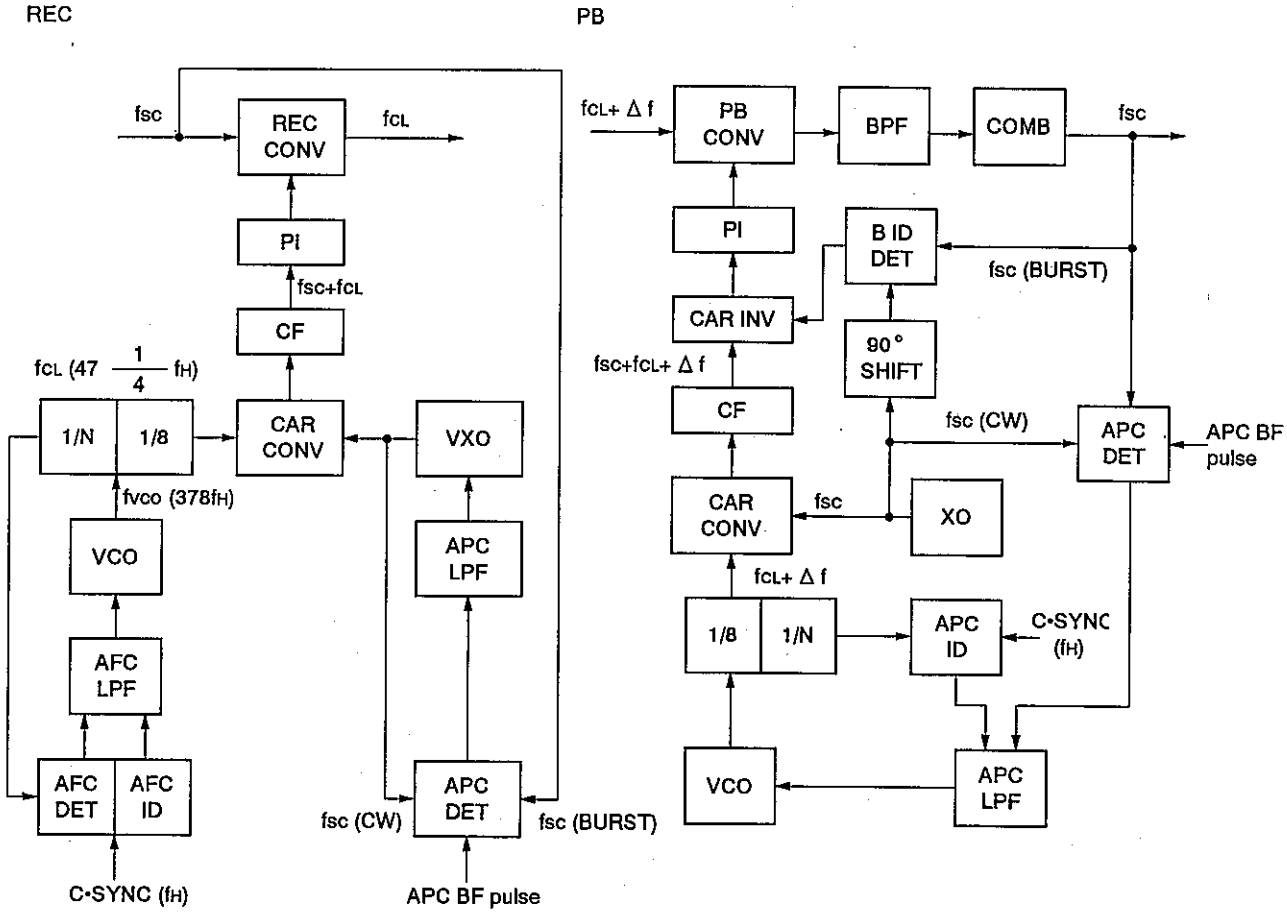
$P_{I180} = |\ (\theta_{SG1}-\theta_{P12})_{n+1}-(\theta_{SG1}-\theta_{P12})_{n}\ |$

$P_{I0} = |\ (\theta_{SG1}-\theta_{P12})_{n+1}-(\theta_{SG1}-\theta_{P12})_{n}\ |$

fsc continuous wave is input through Pin 30. f_{CL} that was low band converted inside the IC at REC CONV and fc (fc=274 3/4 f_H) output of Pin 4, are frequency converted outside the IC and fsc is obtained. The phase relation of this waveform and the phase relation of the fsc input are compared at the nH and (n+1) H stage. Through testing it is confirmed that at SW14 ON there is a 180° phase difference, while at SW14 OFF there is a 0° phase difference.

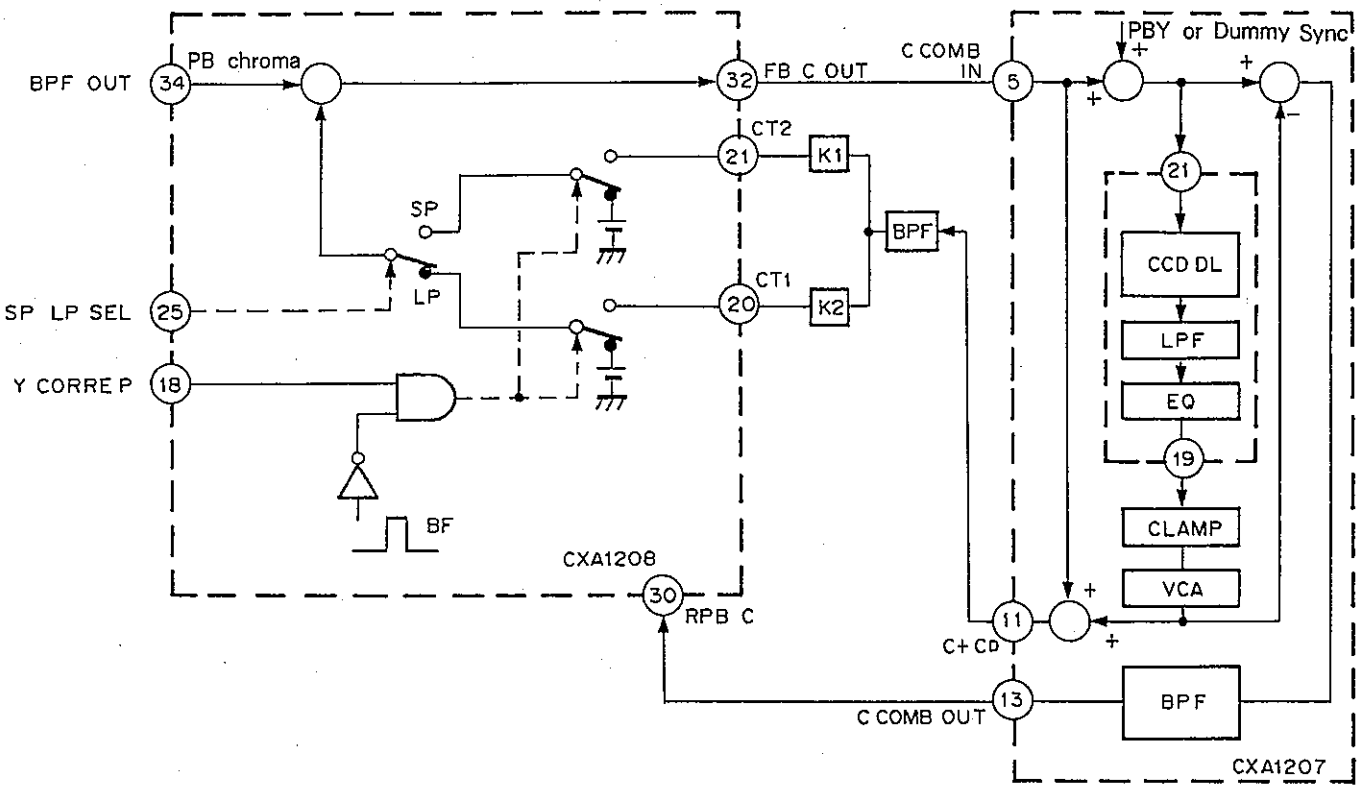
Description of Functions

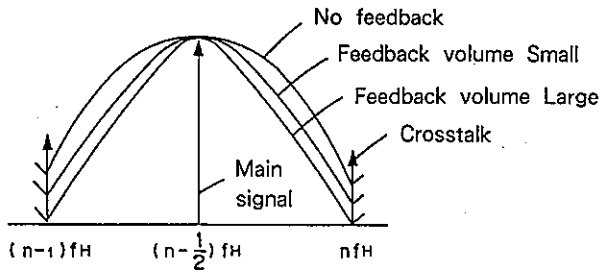
1. Color sync block (NTSC)



REC AFC LOOP	fcL (47+ 1/4)fH is composed from C SYNC (fH).
REC APC LOOP	Composes a phase locked fsc continuous wave at the input chroma burst.
REC AFC ID	Pulls in VCO in the vicinity of the lock point with the rising edge or other.
PB APC LOOP	PB chroma burst is phase locked at the XO fsc.
PB APC ID	Prevents PB APC LOOP mislock.
PB BURST ID	During a phase relation where APC response speed is slow, inverts the carrier phase to hasten the pull in.

2. PB chroma feedback comb filter



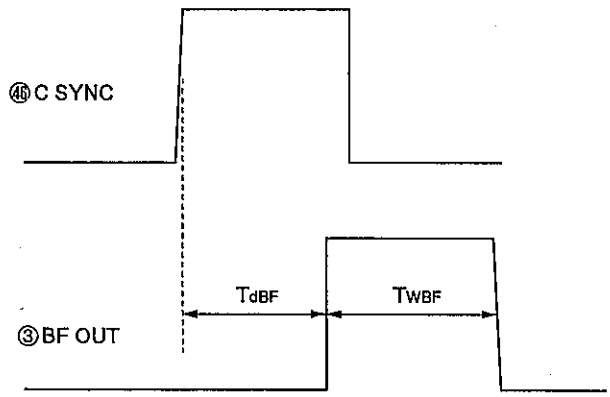


The chroma feedback comb filter is composed as shown in the Fig. above. By selecting the constant of the external ATT (K_1, K_2) the tooth depth of the comb can be varied.

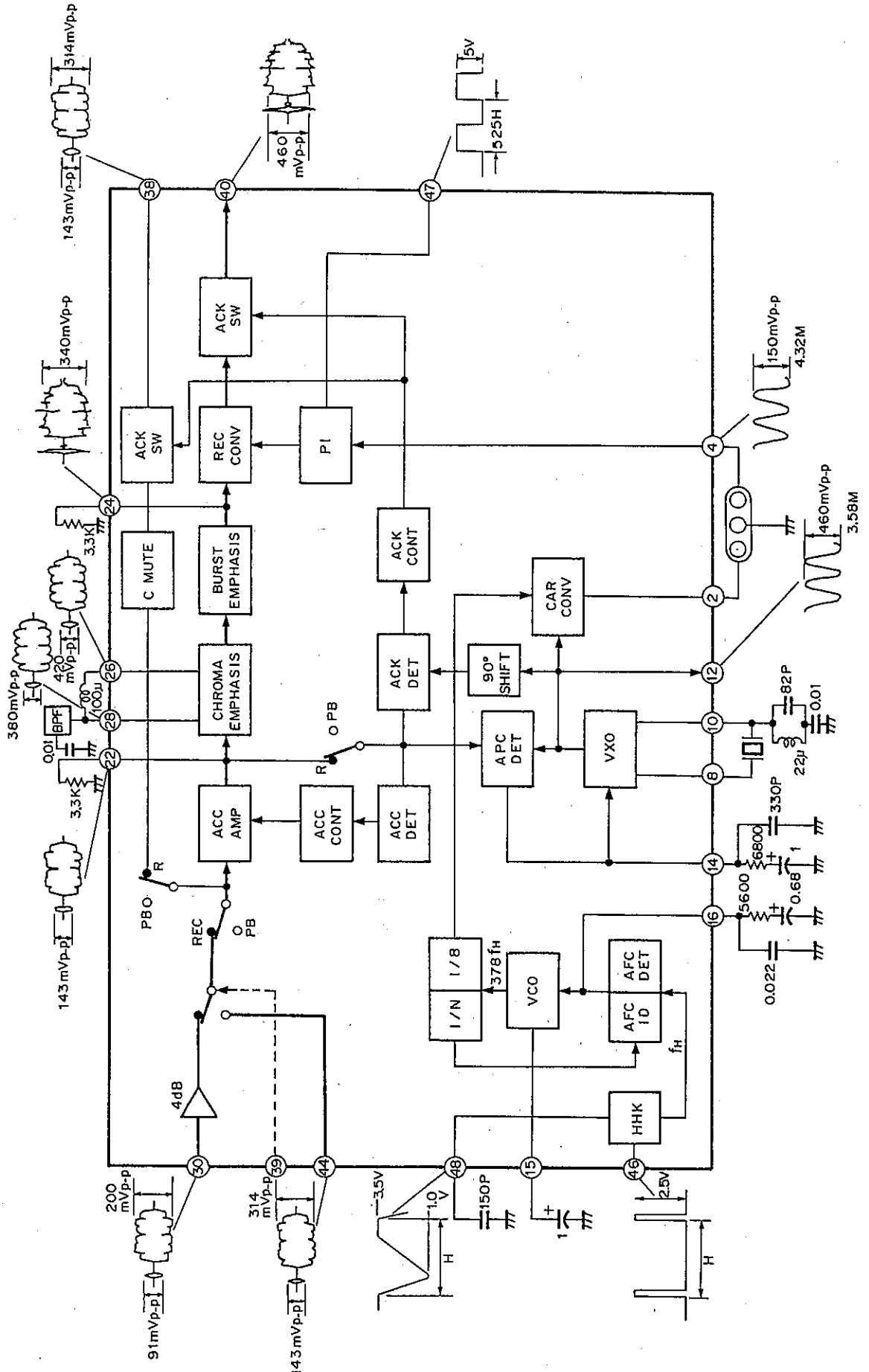
3. BF OUT pulse

Considering usage in conjunction with CXA1207A BF pulse timing changes respectively with the following modes.

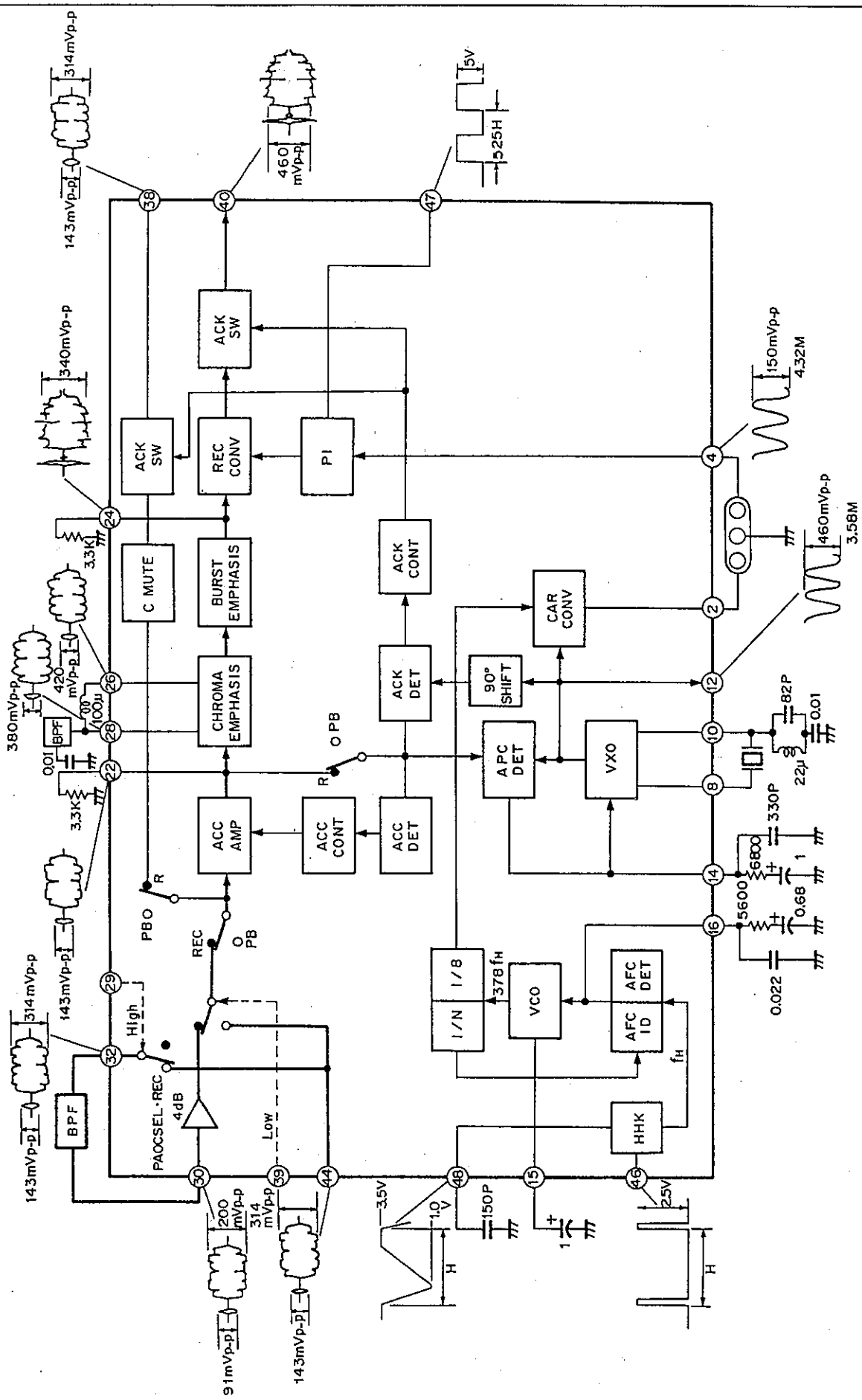
NTSC•REC	: T_{dBF}(NT•REC)	
PAL•REC	: T_{dBF}(NT•REC)	+100nsec
PB	: T_{dBF}(NT•REC)	–250nsec
Width	: T_{WBF} is constant	



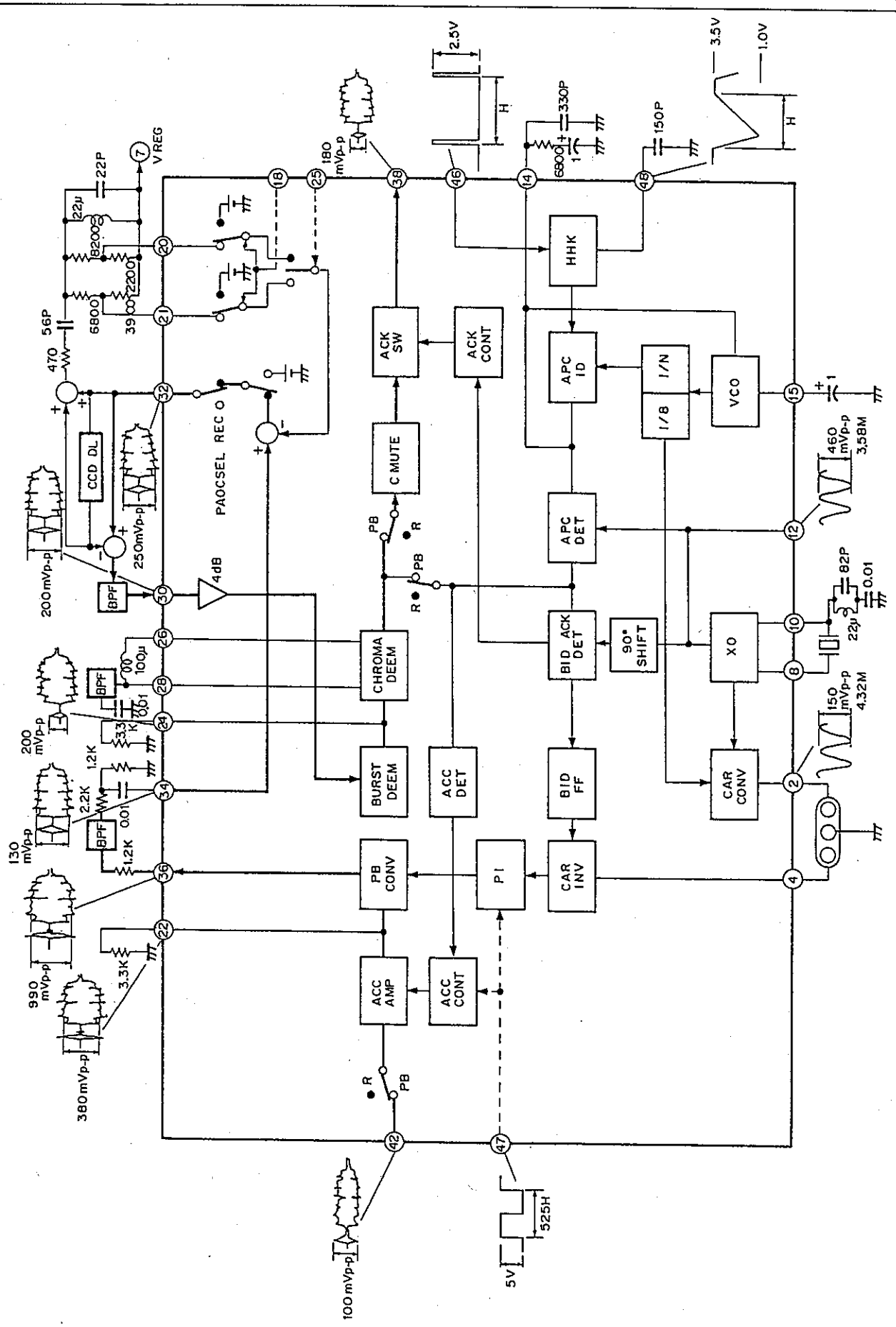
NORMAL REC Block Diagram (NTSC)



CAMERA REC Block Diagram (NTSC)



PB Block Diagram (NTSC)



Adjustment Sequence Modes

- [16], [9] and [14] indicate the data value numbers of the CXA1207A BUS DECODER.
- Recording : The CXA1207A BUS DECODER [19] PB=Low, and the CXA1208 Pin 33 (PB) is Low.
- Playback : The CXA1207A BUS DECODER [19] PB=High, and the CXA1208 Pin 33 (PB) is High.

Adjustment Procedures for CXA1207A and CXA1208 (See Application Circuit)

1. REC Y level adjustment

Mode : Recording, [16] Video AGC=High
Input signal : Color bar 500mVp-p (CXA1207A Pin 32 VIN 1)
Adjustment method : With 75Ω connection to the CXA1207A Pin 38 VIDEO OUT, adjust RV102 (EE LEVEL) to get 1Vp-p.

2. Y/C separation adjustment

Mode : Recording
Input signal : Color bar 500mVp-p (CXA1207A Pin 32 VIN 1)
Adjustment method : Adjust in sequence RV113 (YC SEP), RV110 (COMB ADJ), RV113 (YC SEP), so that the CXA1207A Pin 11 C+CD residual chroma component is minimum.

3. IR adjustment

Mode : Recording, with 2.5V to 3.5V applied to CXA1207A Pin 51 SWP.
Input signal : Color bar 500mVp-p (CXA1207A Pin 32 VIN 1)
Adjustment method : Adjust the IR adjustment variable resistor (RV109), so that the CXA1207A Pin 7 Y COMB OUT residual chroma component is minimum. The residual chroma component should be –20dB (Typ.) to the input chroma level.

4. Emphasis input Y level adjustment

Mode : Recording
Input signal : Color bar 500mVp-p (CXA1207A Pin 32 VIN 1)
Adjustment method : Adjust RV115 (EMPH Y LEVEL), so that the CXA1207A Pin 3 EMPH IN Y signal level is 500mVp-p.

5. YFM carrier adjustment

Mode : Recording, [9] E=Low (Normal mode), [9] E=High (Hi8 mode)
Input signal : 100% white 500mVp-p (CXA1207A Pin 32 VIN 1)
Adjustment method : Watching the signal on the CXA1207A Pin 43 Y RF OUT with a spectral analyzer, adjust RV119 (CAR) so that the H SYNC spectrum (carrier) is 4.2MHz in Normal mode and 5.7MHz in Hi8 mode.

6. YFM deviation adjustment

Mode : Recording, [9] E=Low (Normal mode), [9] E=High (Hi8 mode)
Input signal : 100% white 500mVp-p (CXA1207A Pin 32 VIN 1)
Adjustment method : Watching the signal on the CXA1207A Pin 43 Y RF OUT with a spectral analyzer, adjust RV120 (DEV) so that the 100% white Y level spectrum is 5.4MHz in Normal mode and 7.7MHz in Hi8 mode.

7. Playback Y level adjustment

Mode : Playback, 14 W CCD=Low (Using 1 CCD delay line), 14 W CCD=High (Using 2 CCD delay lines)
Input signal : PB Y RF 100mVp-p (CXA1207A Pin 41 PB RF IN)
Adjustment method : Adjust RV114 (PB Y LEVEL 1) to get 500mVp-p on the CXA1207A Pin 21 DL IN1 when using 1 CCD delay line and on the CXA1207A Pin 15 DL IN2 when using 2 CCD delay lines.

8. Playback Y level 2 adjustment

Mode : Playback
Input signal : PB Y RF 100mVp-p (CXA1207A Pin 41 PB RF IN)
Adjustment method : With 75Ω connection to the CXA1207A Pin 38 VIDEO OUT, adjust RV121 (PB Y LEVEL 2) to get 1Vp-p.

9. Chroma emphasis fo adjustment

Mode : Recording
Input signal : Color bar 500mVp-p (CXA1207A Pin 32 VIN 1)
Adjustment method : Adjust the core of the C EMPH FL107 attached to the CXA1208 Pin 28 C EMPH 1, so that the level of the flat portion of the chroma signal on the CXA1208 Pin 24 B EMPH OUT is minimum. (The CXA1208 Pin 24 should have 3.3kΩ connected to ground.)

Precautions on Usage of CXA1208R/Q

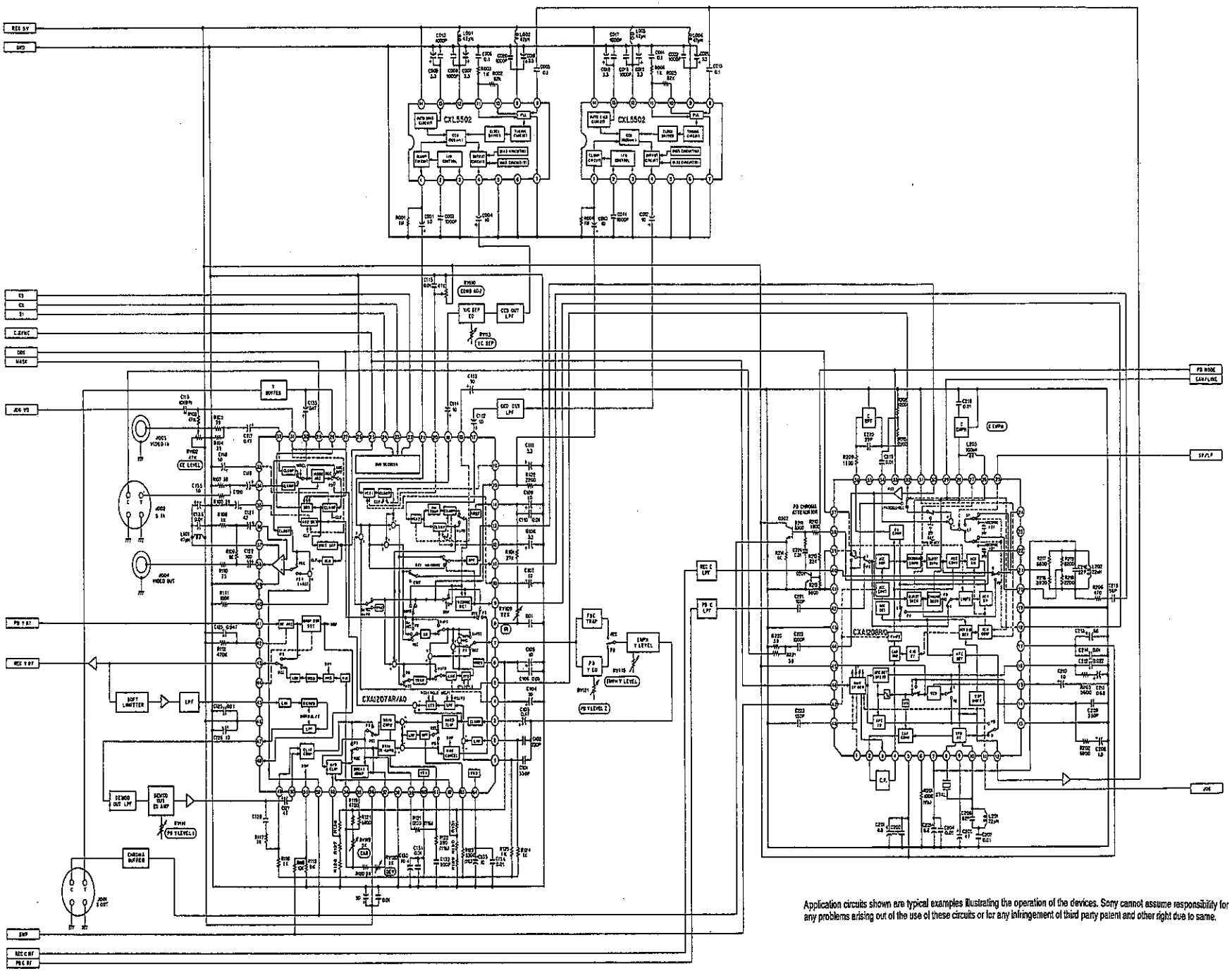
(1) When FSC OUT (Pin 12) signal is utilized as the CCD clock frequency, be careful with the routing. Avoid by all means crossing signal lines.

(2) X'tal (crystal) fo varies according to the floating capacity, and others. Set as close to the IC as possible, and keep wiring short.

(3) HHK C capacity 150P of Pin 48 determines BF timing. Accordingly set close to the IC to avoid the influence of the floating capacity, and others, and keep wiring short. Also, use a CH for temperature compensation of the type that does not sustain much effects from temperature differences.

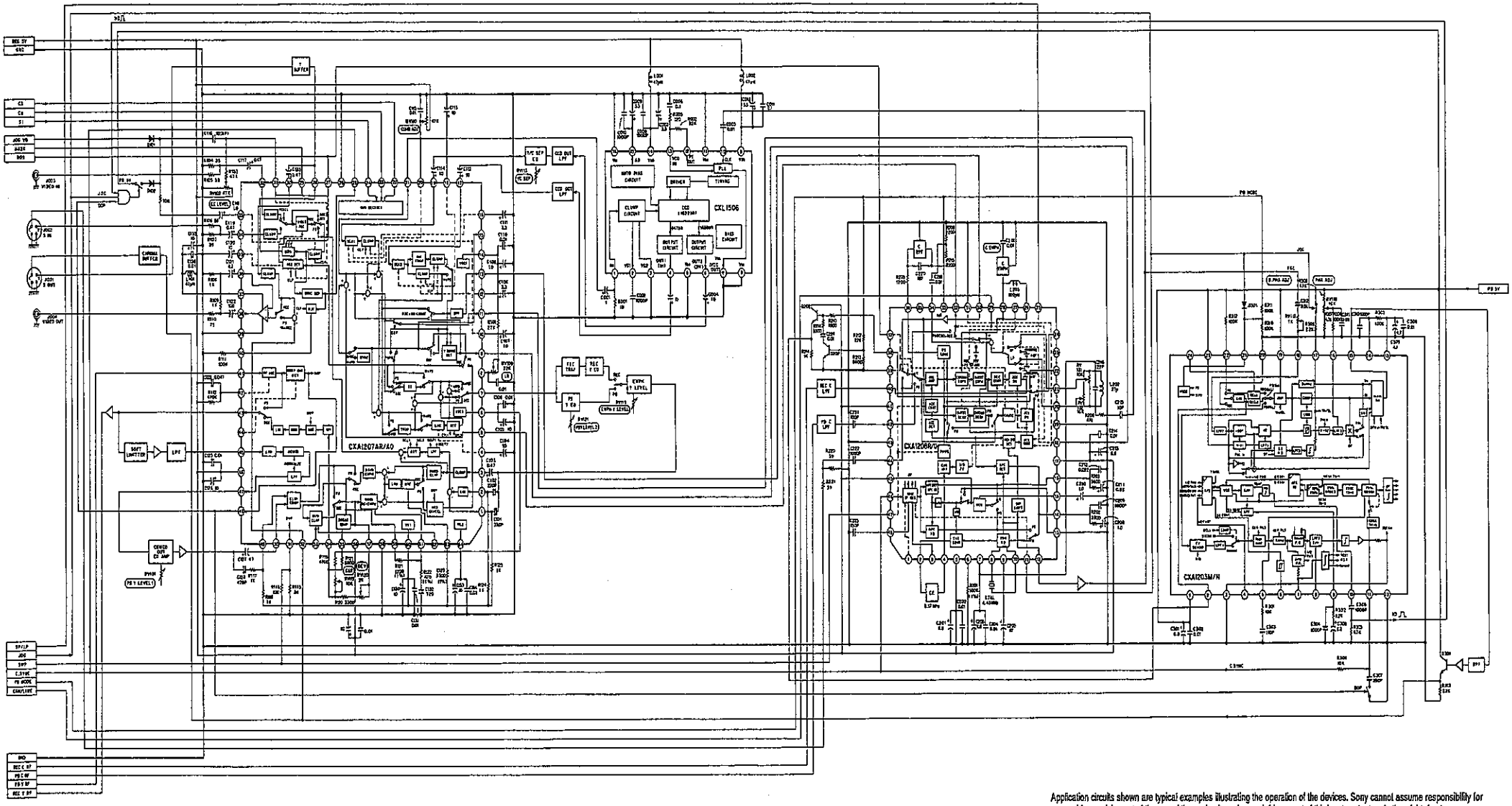
(4) I REF (Pin 6) resistance 100K, determines the external reference current. Employ a metallic film resistance and of allowable difference ± 1%.

Application Circuit (NTSC, Hi8 mode)



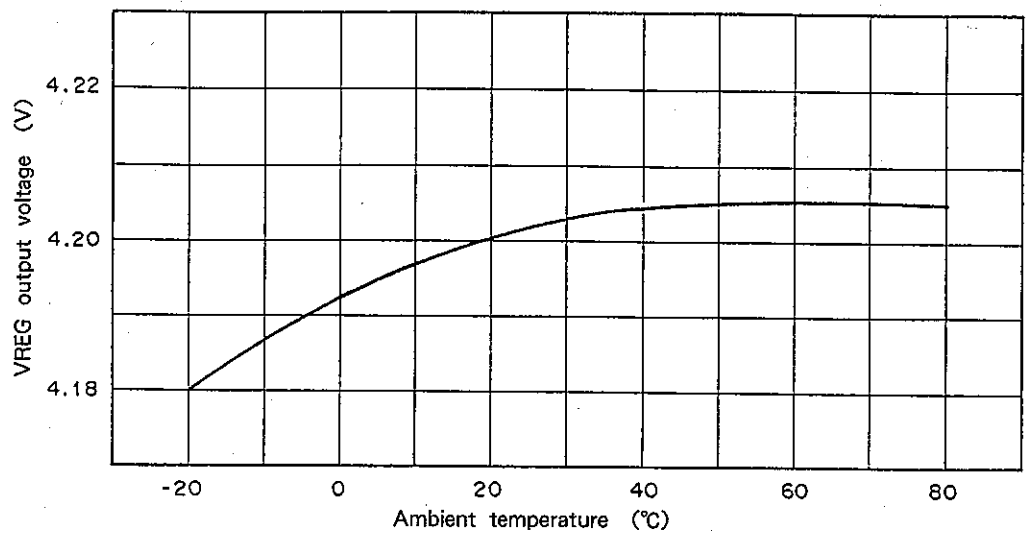
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit (PAL, Normal mode)

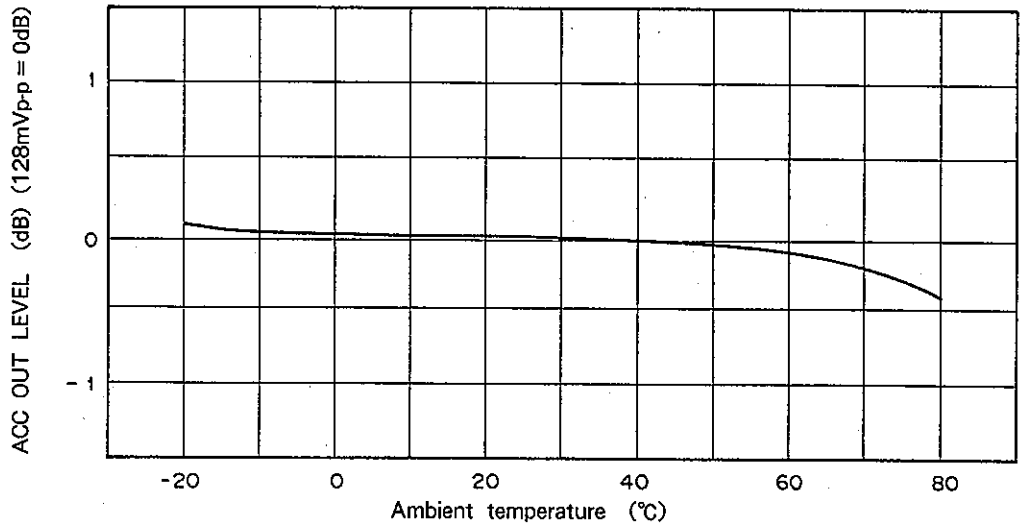


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

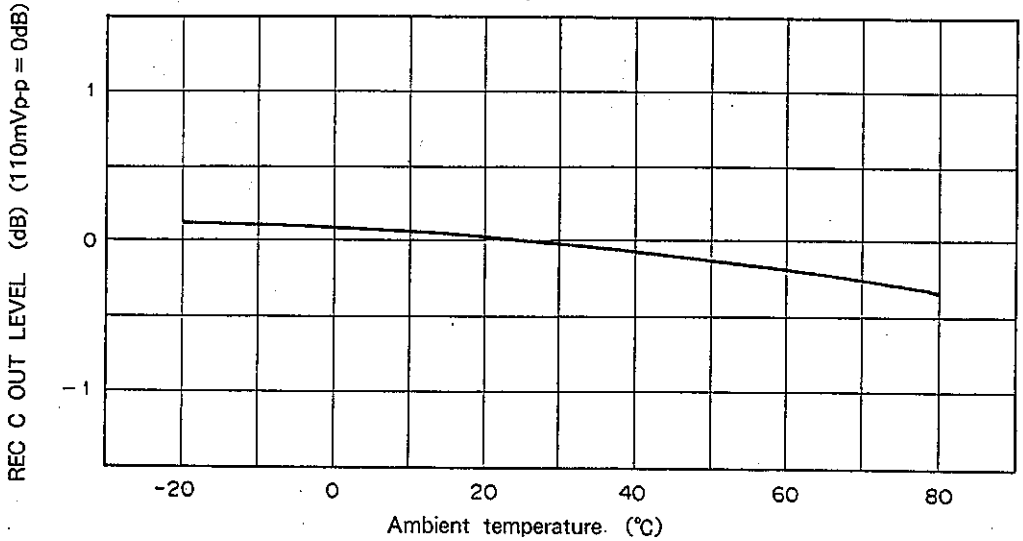
VREG temperature characteristics



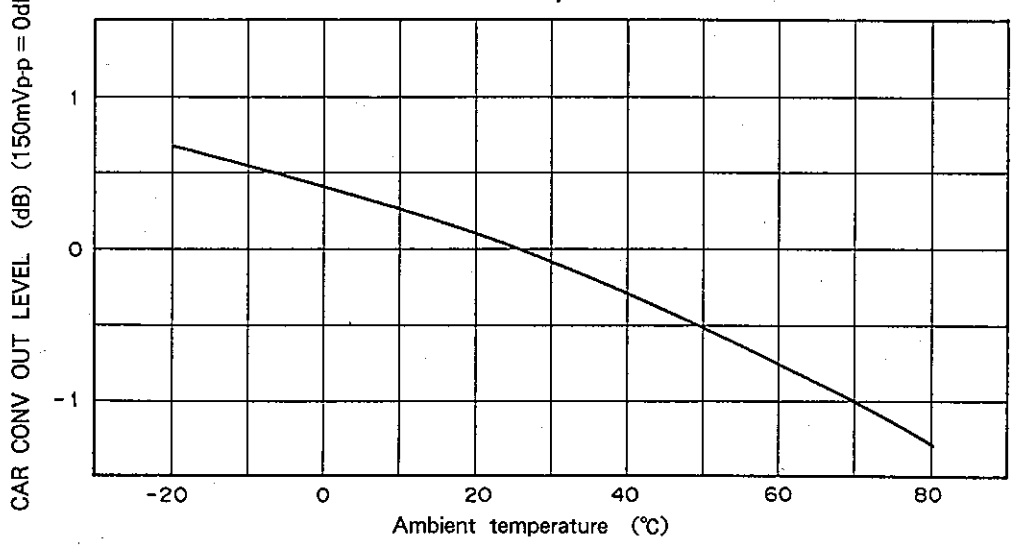
ACC OUT LEVEL temperature characteristics



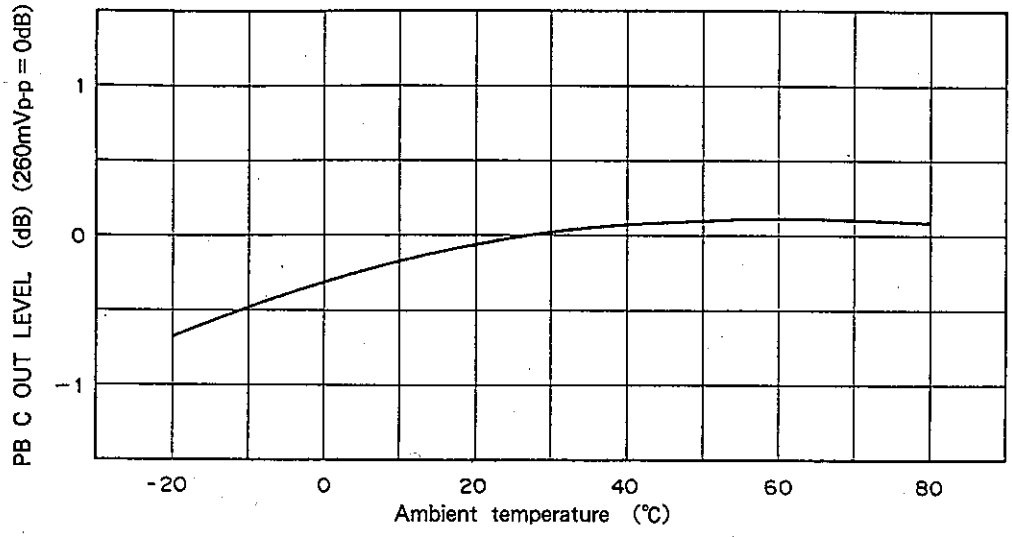
REC C OUT LEVEL temperature characteristics



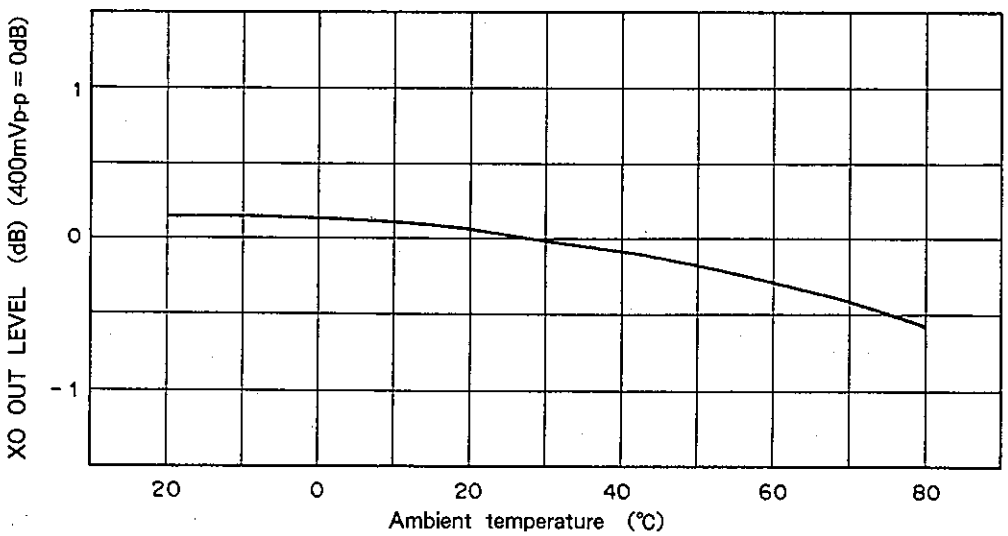
CAR CONV OUT LEVEL temperature characteristics



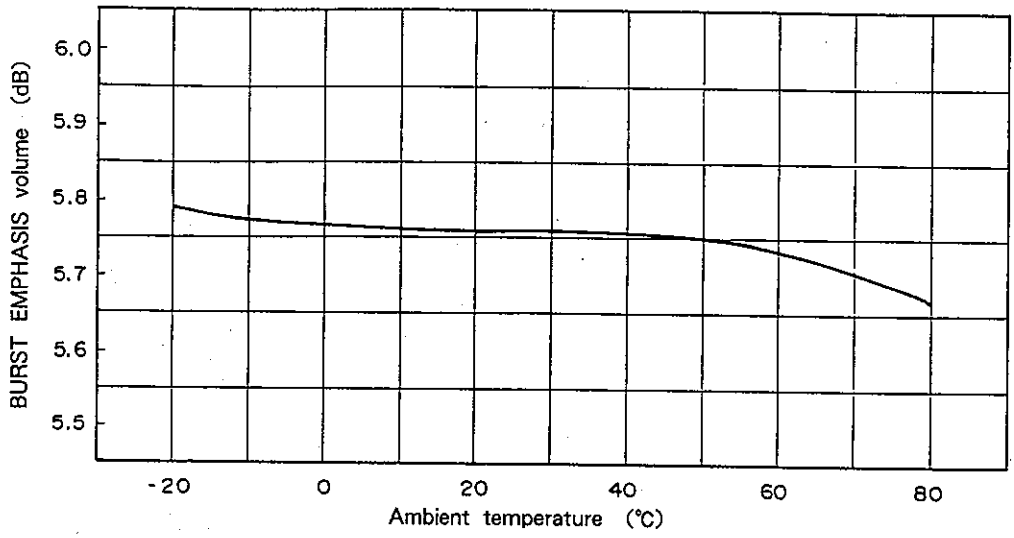
PB C OUT LEVEL temperature characteristics



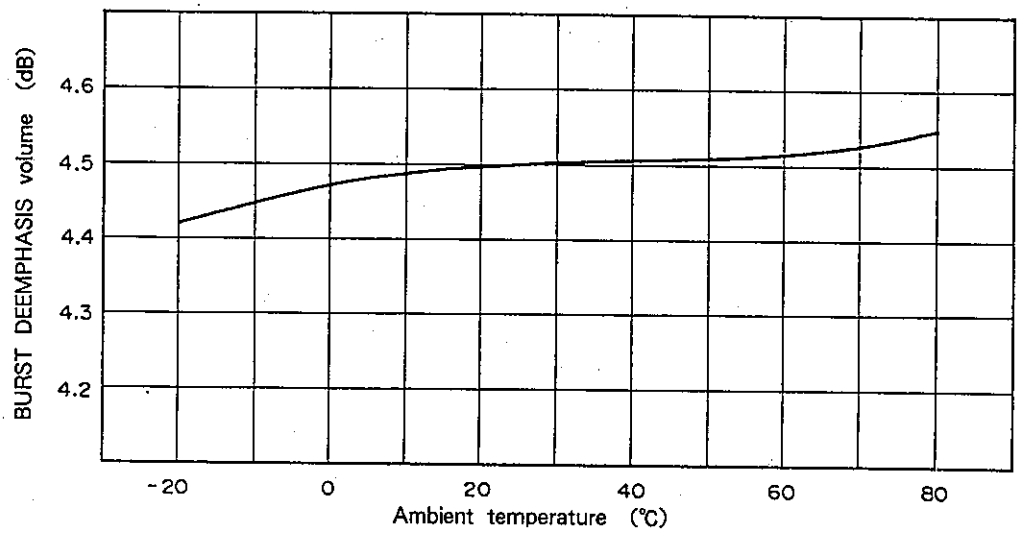
XO OUT LEVEL temperature characteristics



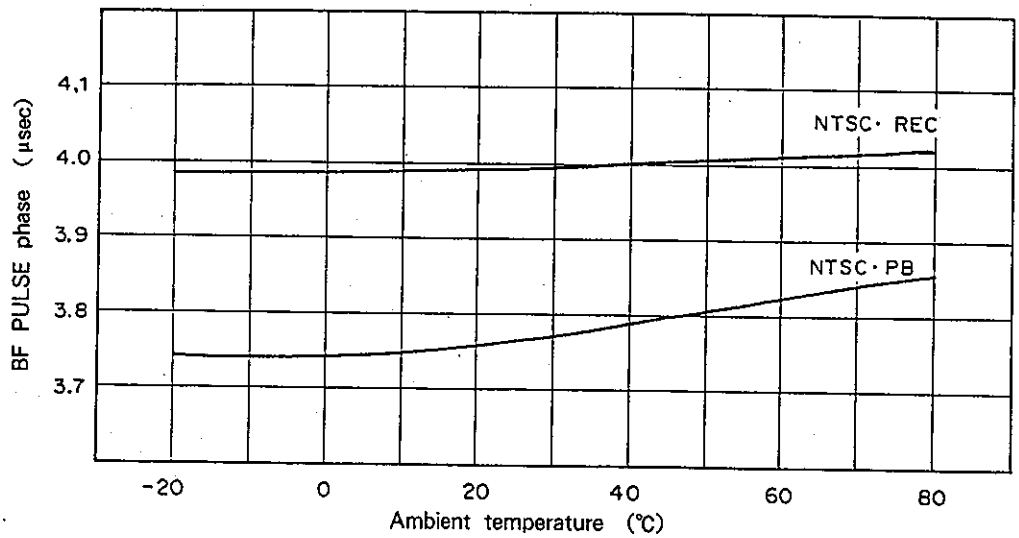
BURST EMPHASIS temperature characteristics



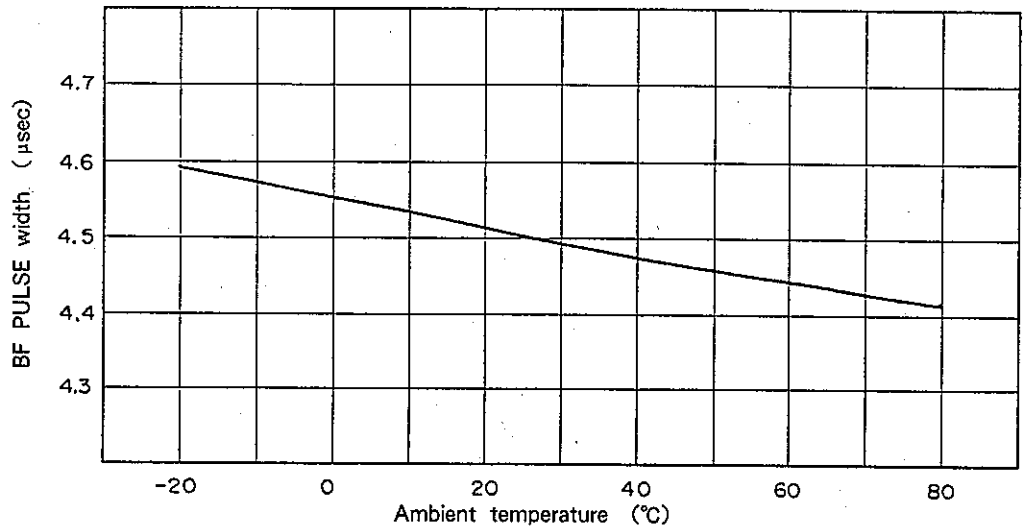
BURST DEEMPHASIS temperature characteristics



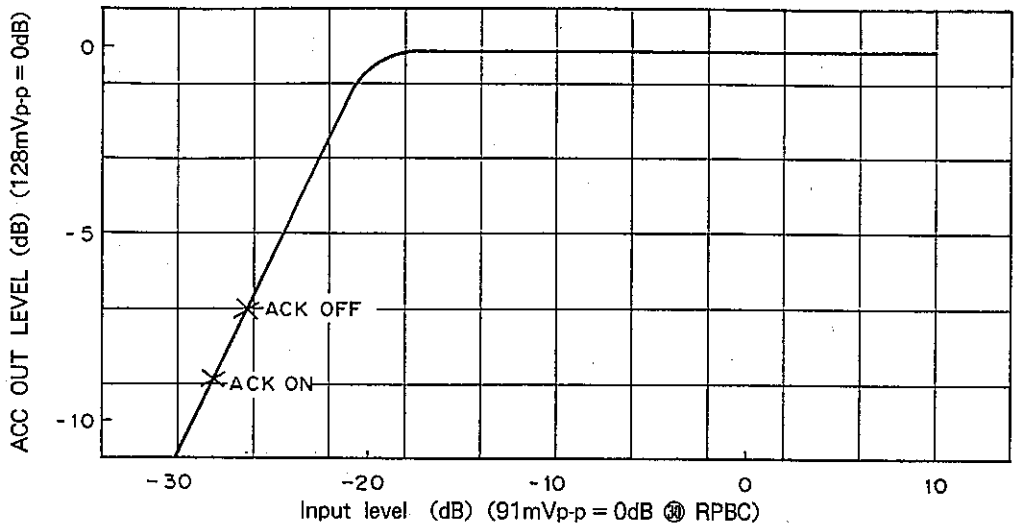
BF PULSE phase temperature characteristics



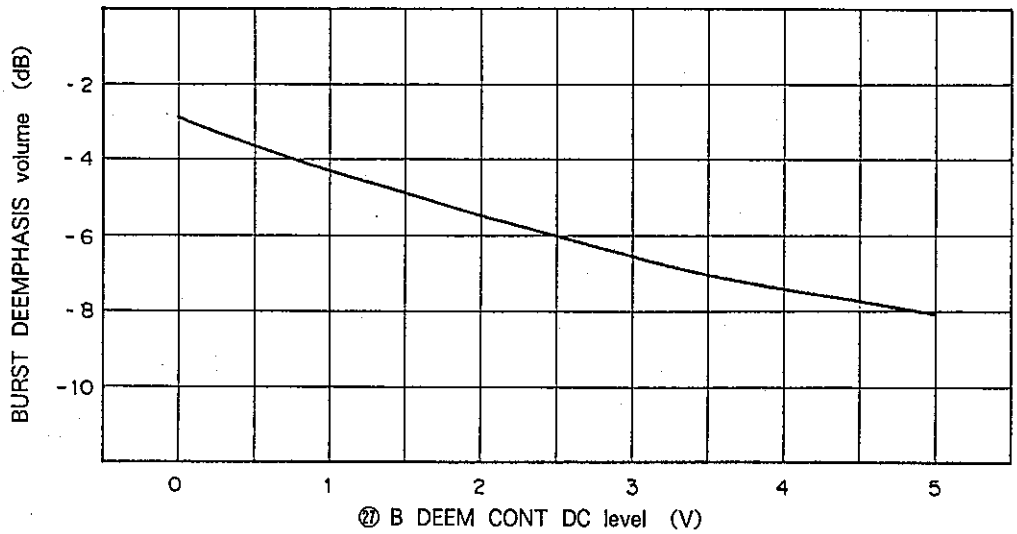
BF PULSE width temperature characteristics



ACC characteristics



BURST DEEMPHASIS control characteristics

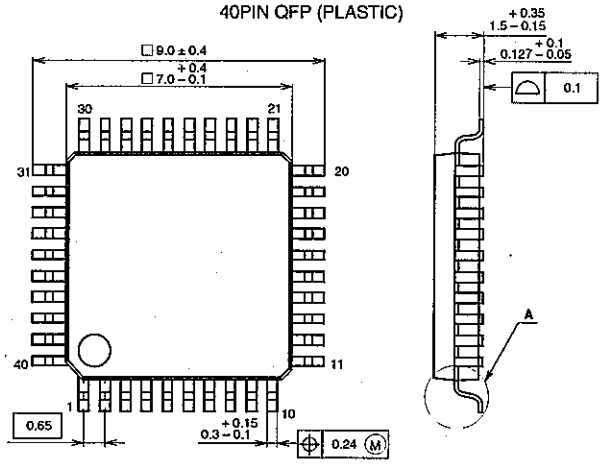


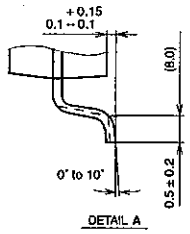
Package Outline

Unit: mm

CXA1208Q

40PIN QFP (PLASTIC)





DETAIL A

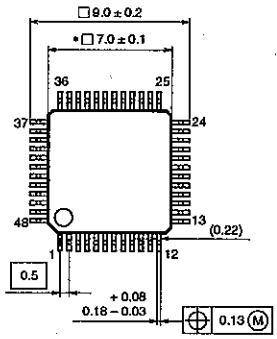
SONY CODE	QFP-40P-L01
EIAJ CODE	P-QFP40-7x7-0.65
JEDEC CODE	————

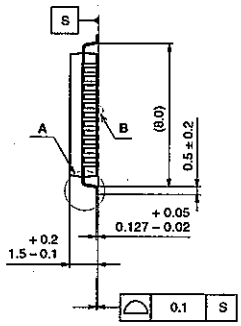
PACKAGE STRUCTURE

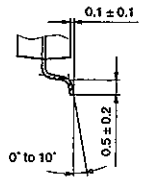
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g

CXA1208R

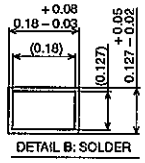
48PIN LQFP (PLASTIC)







DETAIL A



DETAIL B: SOLDER

NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	P-LQFP48-7x7-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm