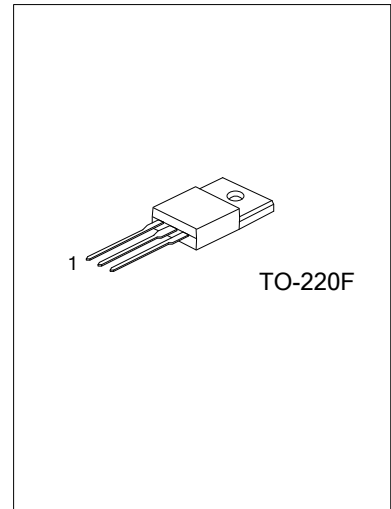
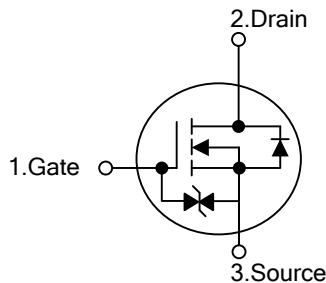


**UF830Z***Power MOSFET***4.5A, 500V, 1.5Ω, N-CHANNEL
POWER MOSFET****■ DESCRIPTION**

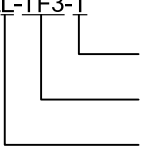
The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications, such as switching regulators, switching converters, solenoid, motor drivers and related drivers.

■ FEATURES

- * $V_{DS} = 500V$
- * $I_D = 4.5A$
- * $R_{DS(ON)} = 1.5\Omega$
- * Single Pulse Avalanche Energy Rated
- * Rugged- SOA is Power Dissipation Limited
- * Fast Switching Speeds
- * Linear Transfer Characteristics
- * High Input Impedance
- * ESD Protected

■ SYMBOL**■ ORDERING INFORMATION**

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UF830ZL-TF3-T	UF830ZG-TF3-T	TO-220F	G	D	S	Tube

UF830ZL-TF3-T 		(1) T: Tube, R: Tape Reel (2) TF3: TO-220F (3) G: Halogen Free, L: Lead Free
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■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, Unless Otherwise Specified.)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage (T _J =25°C ~125°C)		V _{DS}	500	V
Drain to Gate Voltage (R _{GS} =20kΩ, T _J =25°C ~125°C)		V _{DGR}	500	V
Gate to Source Voltage		V _{GS}	±30	V
Drain Current	Continuous	I _D	4.5	A
	Pulsed	I _{DM}	18	A
Power Dissipation (T _C = 25°C)		P _D	38	W
Single Pulse Avalanche Energy Rating (Note 2)		E _{AS}	300	mJ
Junction Temperature		T _J	+150	°C
Storage Temperature		T _{STG}	-55 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. V_{DD}=50V, starting T_J=25°C, L=25mH, R_G=25Ω, peak I_{AS}=4.5A

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ _{JA}	62.5	°C/W
Junction to Case	θ _{Jc}	3.31	°C/W

■ ELECTRICAL SPECIFICATIONS (Ta = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	500			V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} =V _{DS} , I _D =250μA	2.0		4.0	V
On-State Drain Current (Note 1)	I _{D(ON)}	V _{DS} >I _{D(ON)} ×R _{DS(ON)MAX} , V _{GS} =10V	4.5			A
Drain-Source Leakage Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} =0V			25	μA
		V _{DS} =0.8×Rated BV _{DSS}			250	μA
		V _{GS} =0V, T _J = 125°C				
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V			±800	nA
Static Drain-Source On-State Resistance (Note 2)	R _{DS(ON)}	I _D =2.5A, V _{GS} =10V		1.3	1.5	Ω
Forward Transconductance (Note 1)	g _{FS}	V _{DS} ≥10V, I _D =2.7A	2.5	4.2		S
Turn-On Delay Time	t _{D(ON)}	V _{DD} =250V, I _D ≈4.5A R _{GS} =12Ω, R _L =54Ω (Note 2)		10	17	ns
Turn-On Rise Time	t _R			15	23	ns
Turn-Off Delay Time	t _{D(OFF)}			33	53	ns
Turn-Off Fall Time	t _F			16	23	ns
Total Gate Charge	Q _G	V _{GS} =10V, I _D =4.5A		22	32	nC
Gate-Source Charge	Q _{GS}	V _{DS} =0.8×Rated BV _{DSS}		3.5		nC
Gate-Drain Charge	Q _{GD}	I _{G(REF)} =1.5mA (Note 3)		11		nC
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		600		pF
Output Capacitance	C _{OSS}			100		pF
Reverse Transfer Capacitance	C _{RSS}			20		pF

Note: 1. Pulse Test: Pulse width≤300μs, Duty Cycles≤2%.

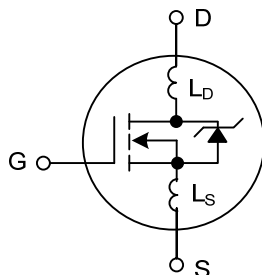
2. MOSFET Switching Times are Essentially Independent of Operating Temperature.

3. Gate Charge is Essentially Independent of Operating Temperature.

■ INTERNAL PACKAGE INDUCTANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Internal Drain Inductance					
Measured from the contact screw on tab to center of die	L _D		3.5		nH
Measured from the drain lead(6mm from package) to center of die			4.5		nH
Internal Source Inductance					
Measured from the source lead(6mm from header) to source bond pad	L _S		7.5		nH

Remark: Modified MOSFET symbol showing the internal devices inductances as below.

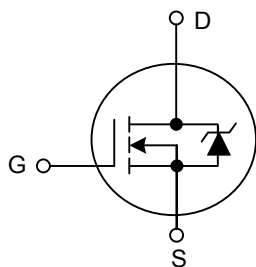


■ SOURCE TO DRAIN DIODE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Source to Drain Diode Voltage (Note 1)	V_{SD}	$T_J=25^{\circ}\text{C}$, $I_{SD}=4.5\text{A}$, $V_{GS}=0\text{V}$			1.6	V
Continuous Source to Drain Current	I_{SD}	Note 2			5.5	A
Pulse Source to Drain Current	I_{SDM}				18	A
Reverse Recovery Time	t_{RR}	$T_J=25^{\circ}\text{C}$, $I_{SD}=4.5\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$	180	350	760	ns
Reverse Recovery Charge	Q_{RR}	$T_J=25^{\circ}\text{C}$, $I_{SD}=4.5\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$	0.96	2.2	4.3	μC

NOTE : 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

2. Modified MOSFET symbol showing the integral reverse P-N junction diode as below.



■ TEST CIRCUITS AND WAVEFORMS

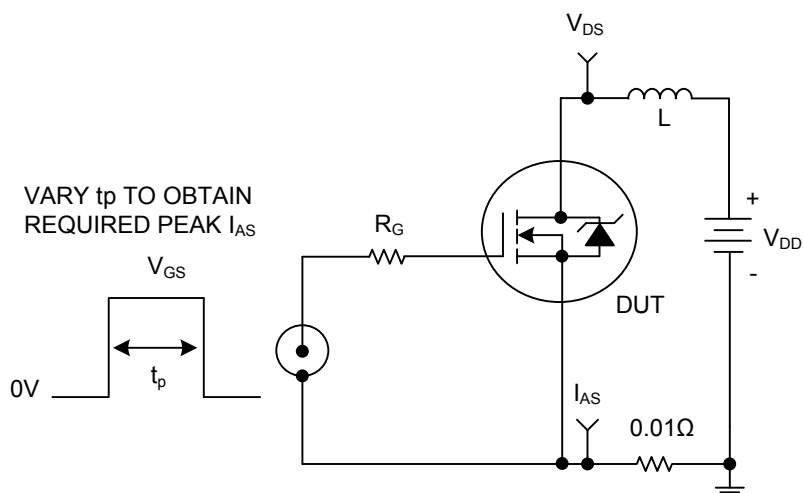


FIG 1. Unclamped Energy Test Circuit

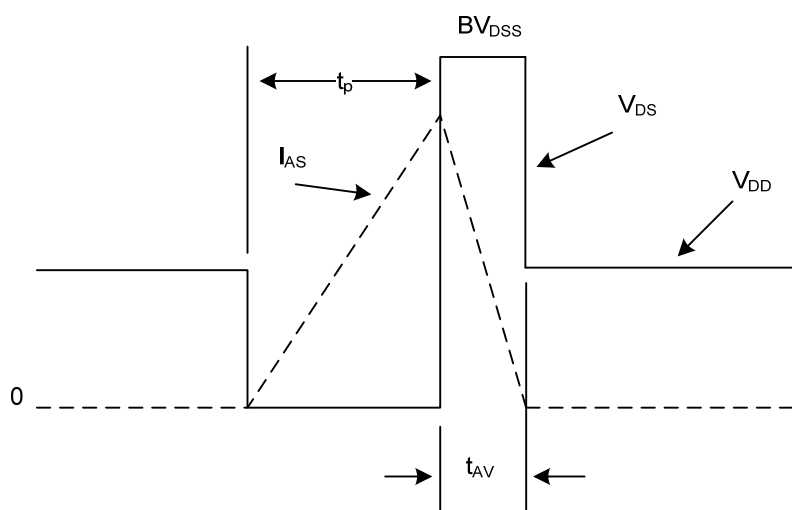


FIG 2. Unclamped Energy Waveforms

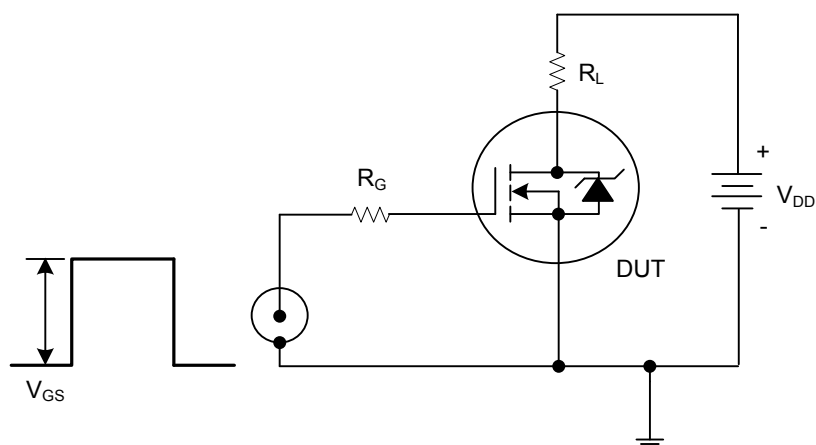


FIG 3. Switching Time Test Circuit

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

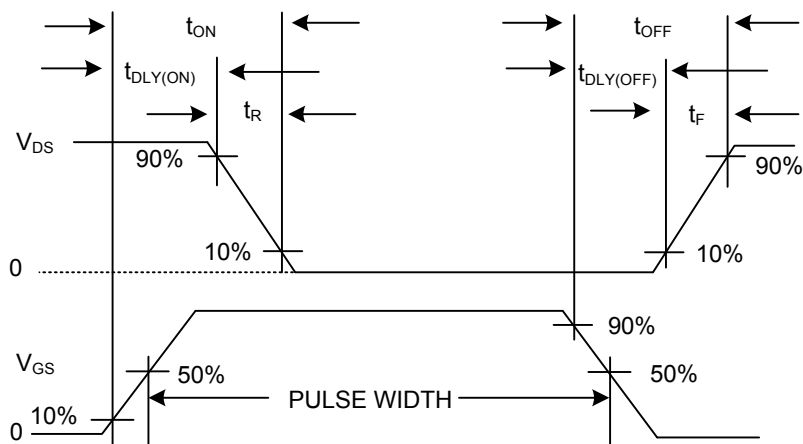


FIG 4. Resistive Switching Waveforms

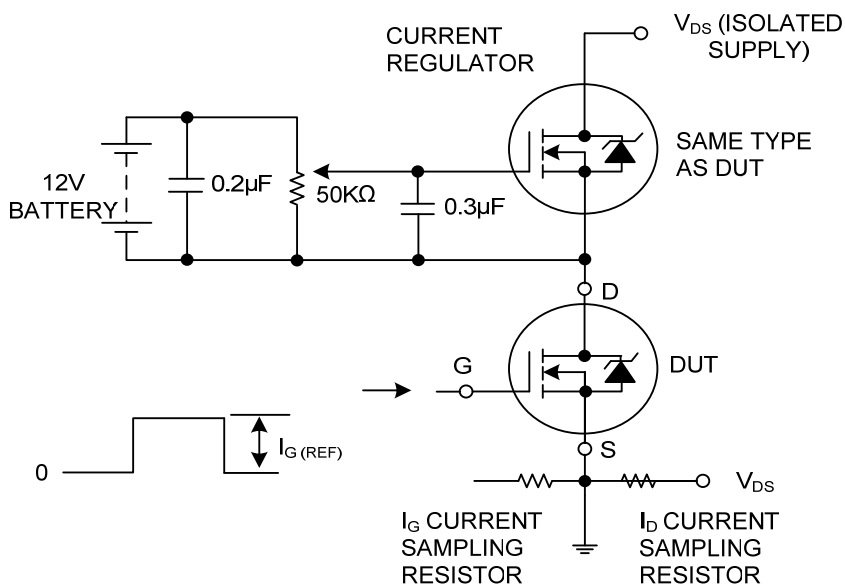


FIG 5. Gate Charge Test Circuit

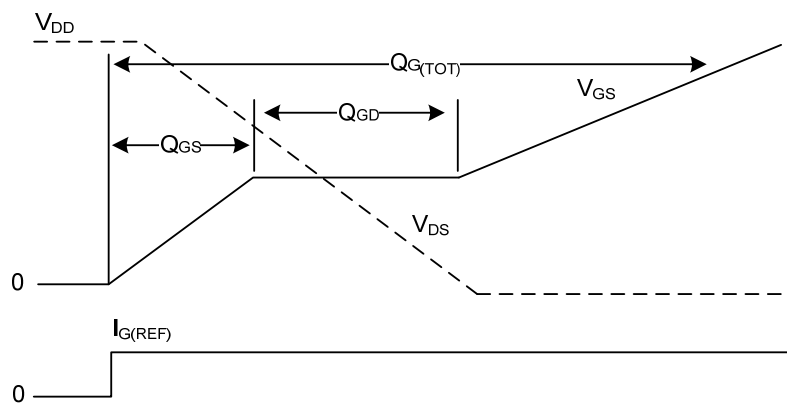
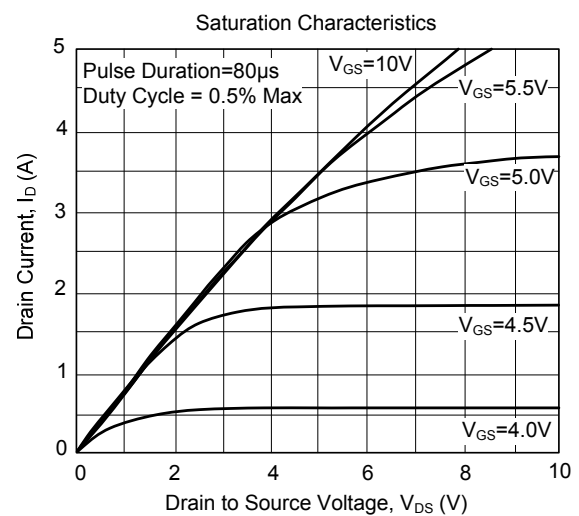
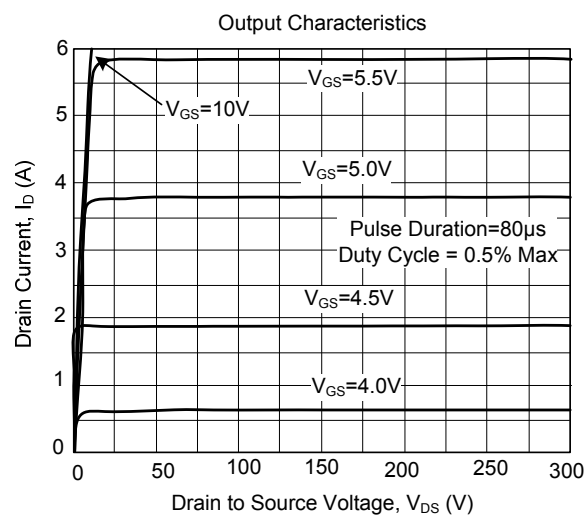
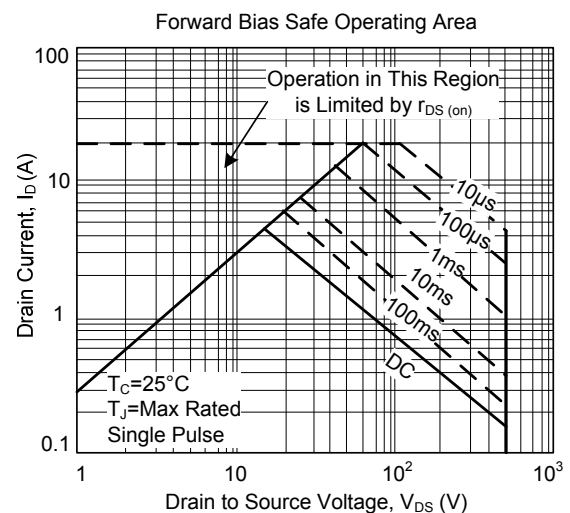
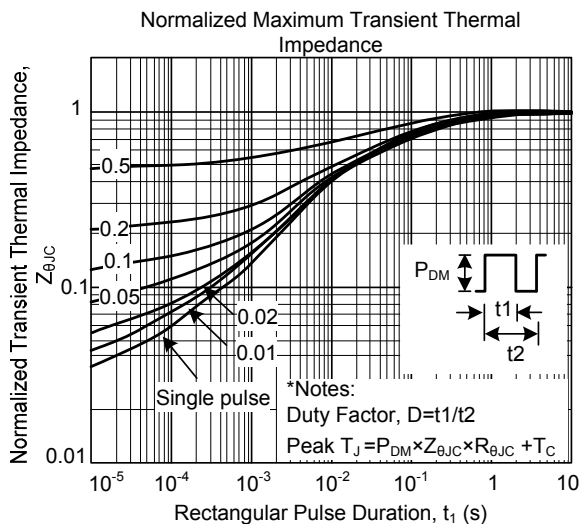
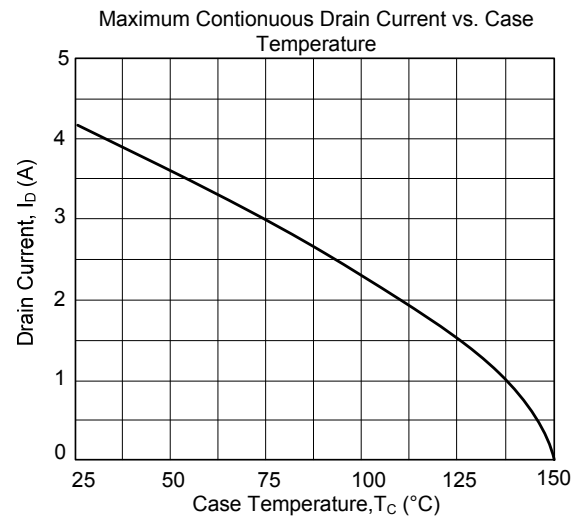
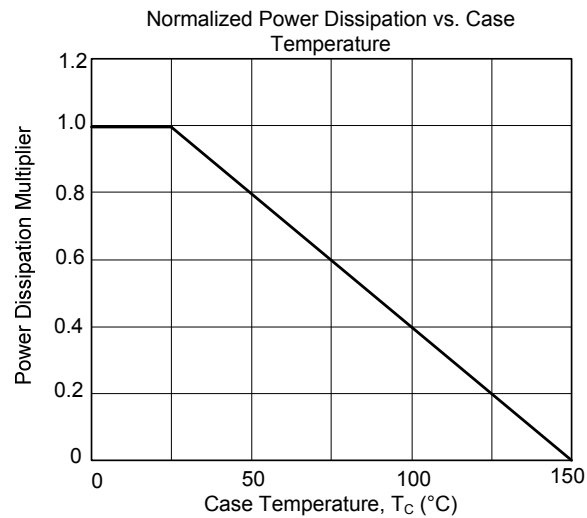
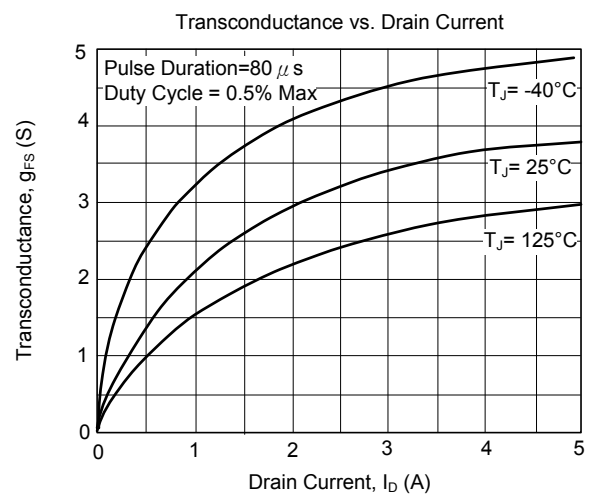
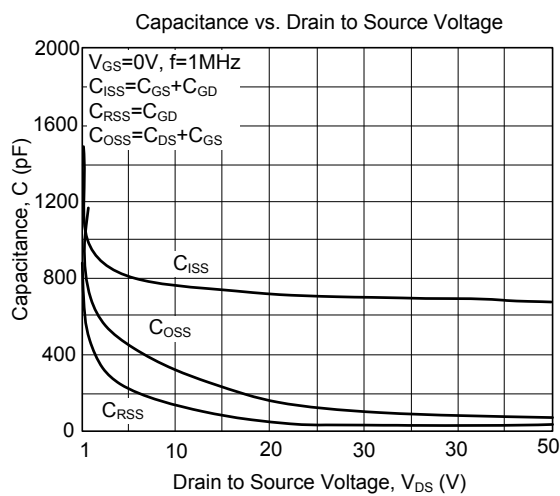
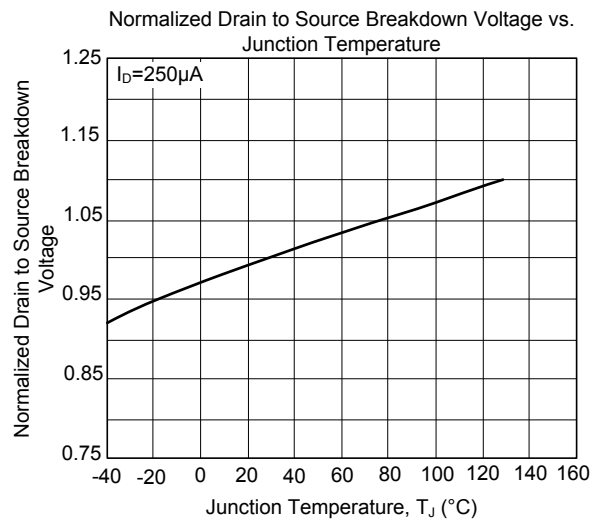
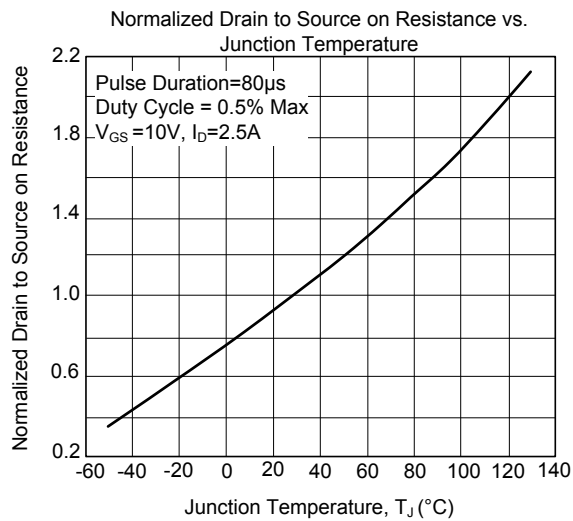
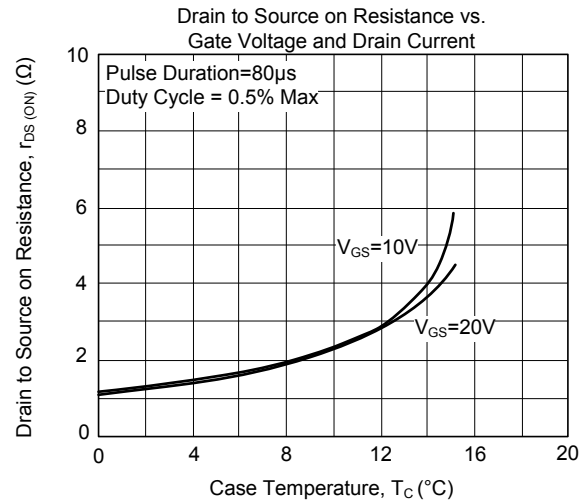
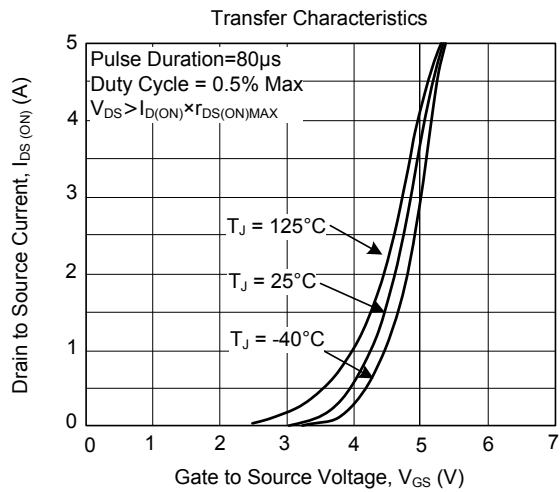


FIG 6. Gate Charge Waveforms

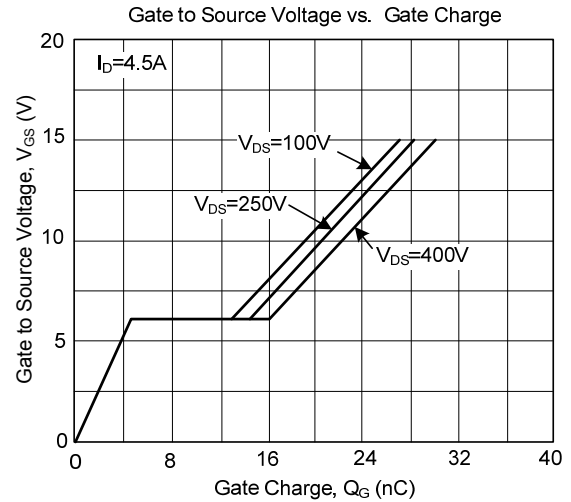
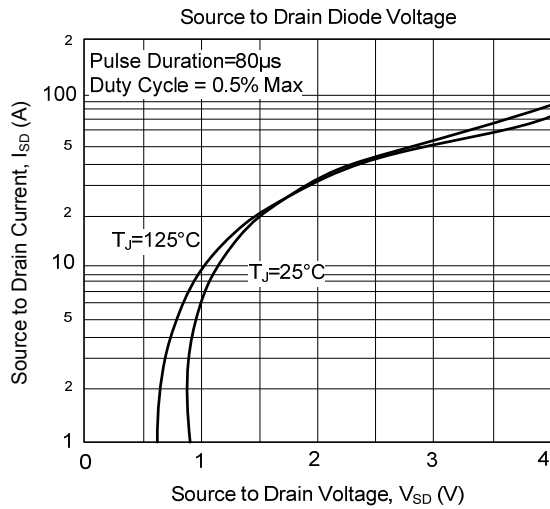
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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