

MULTIRATE (OC-48/24/12/3/GBE/FC) SONET/SDH/ATM TRANSCEIVER w/ FEC S3067

FEATURES

- SiGe BiCMOS technology
- Complies with Bellcore and ITU-T specifications
- On-chip high-frequency PLL for clock generation
- Supports:
 - OC-48 (with FEC)
 - OC-24 (with FEC)
 - OC-12 (with FEC)
 - OC-3 (with FEC)
 - Fibre Channel
- FEC capability up to 8 bytes per 255-byte block
- Reference frequency – 131.25 MHz to 178 MHz
- Interface to LVPECL and TTL logic
- 16-Bit single-ended LVPECL data path
- Compact 156 Pin TBGA package
- Diagnostic loopback mode
- Supports line timing
- Lock Detect
- Signal detect input
- Low jitter LVPECL interface
- Internal FIFO to decouple transmit clocks
- Single 3.3 V supply
- Typical power 1.5 W

- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3067 SONET/SDH transceiver chip is a fully integrated multirate serialization/deserialization SONET OC-48, OC-24, OC-12 and OC-3 interface device. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission and Forward Error Correction (FEC) standards. The device is suitable for SONET-based WDM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3067 transceiver chip allowing the use of a slower external transmit clock reference. The chip can be used with a 131.25 MHz to 178 MHz reference clock in support of existing system clocking schemes.

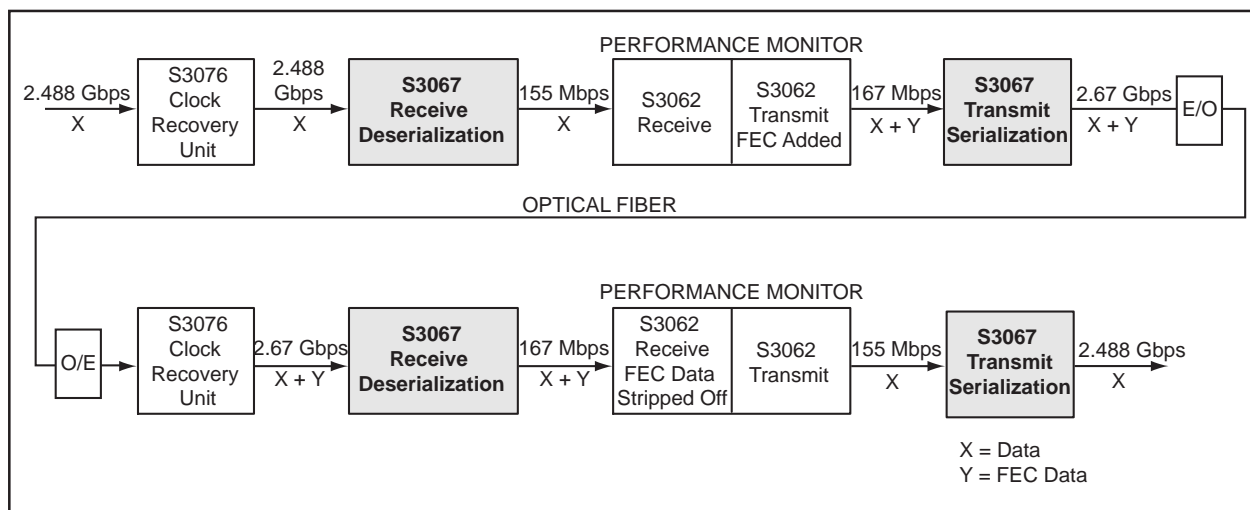
The low jitter LVPECL interface guarantees compliance with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3067 is packaged in a 156 Pin TBGA, offering designers a small package outline.

The S3067 supports FEC designs with internal dividers or external clocking modes.

APPLICATIONS

- Wavelength Division Multiplexing equipment
- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment

Figure 1. System Block Diagram



SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles

the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream, carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N*-byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3067 chip supports up to the OC-48 rate with different FEC modes.

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-48 consists of 144 transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 144 overhead and 4176 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.)

For more details on SONET operations, refer to the Bellcore SONET standard document.

Figure 2. SONET Structure

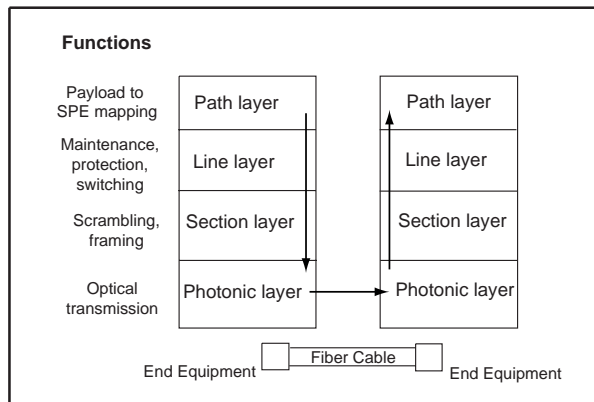
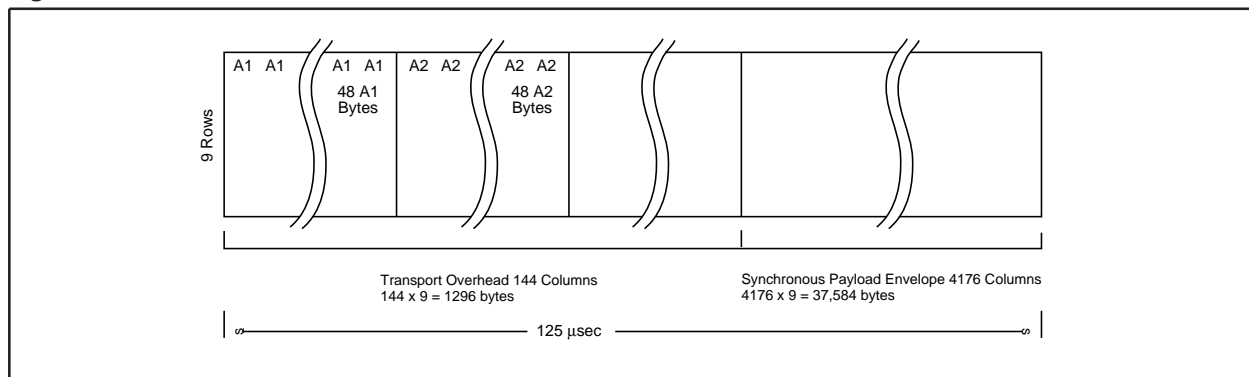


Table 1. SONET Signal Hierarchy

| Elec. | CCITT | Optical | Data Rate (Mbps) |
|--------|--------|---------|------------------|
| STS-1 | | OC-1 | 51.84 |
| STS-3 | STM-1 | OC-3 | 155.52 |
| STS-12 | STM-4 | OC-12 | 622.08 |
| STS-24 | STM-8 | OC-24 | 1244.16 |
| STS-48 | STM-16 | OC-48 | 2488.32 |

Figure 3. STS-48/OC-48 Frame Format



S3067 OVERVIEW

The S3067 transceiver implements SONET/SDH and WDM serialization/deserialization, and transmission functions. The block diagram in Figure 4 shows the basic operation of the chip. This chip can be used to implement the front end of WDM equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, and system timing. The system timing circuitry consists of management of the data stream and clock distribution throughout the front end.

S3067 has the ability to bypass the internal VCO with an external source and also with the receive clock. The device generates 14/15, 15/14, 16/17 and 17/16 clocks based upon the received clock and an external clock to incorporate the FEC capability. The dividers support the first two rates shown in Table 4.

The S3067 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

Transmitter Operations:

1. 16-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver Operations:

1. Serial input
2. Serial-to-parallel conversion
3. 16-bit parallel output

Internal clocking and control functions are transparent to the user. S3067 Supports six different code rates, besides the normal rate, for each of the four operating modes.

Suggested Interface Devices

| | | |
|------|-------|-----------------------------|
| AMCC | S3076 | OC-48 Clock Recovery Device |
| AMCC | S3062 | OC-48 Performance Monitor |

Table 2. Data Rate Select

| RATESEL 0 | RATESEL 1 | Operating Mode |
|-----------|-----------|----------------|
| 0 | 0 | OC-3 |
| 0 | 1 | OC-12 |
| 1 | 0 | OC-24/GBE/FC |
| 1 | 1 | OC-48 |

Table 3. FEC Select

| FEC 0 | 1 | 2 | VCO Divider | RSCLK Divider |
|-------|---|---|-------------|---------------|
| 0 | 0 | 1 | 17 | 16 |
| 1 | 0 | 1 | 16 | 17 |
| 0 | 1 | 1 | 15 | 14 |
| 1 | 1 | 1 | 14 | 15 |
| 0 | 0 | 0 | 17 | X |
| 1 | 0 | 0 | 16 | X |
| 0 | 1 | 0 | 15 | X |
| 1 | 1 | 0 | 14 | X |

Table 4. FEC Modes

| Error Correcting Capability | Code Rate showing Bandwidth Expansion due to code words & FSB | Example of increased input clock frequency for STS-48/STM-16 (MHz) |
|-----------------------------|---|--|
| 8 bytes per 255-byte block | $255/238 = 7.14\%$ increase | $155.52 * 255/238 = 155.52 * 15/14 = 166.63$ |
| 7 bytes per 255-byte block | $255/240 = 6.25\%$ increase | $155.52 * 255/240 = 155.52 * 17/16 = 165.24$ |
| 6 bytes per 255-byte block | $255/242 = 5.37\%$ increase | $155.52 * 255/242 = 163.87$ |
| 5 bytes per 255-byte block | $255/244 = 4.51\%$ increase | $155.52 * 255/244 = 162.53$ |
| 4 bytes per 255-byte block | $255/246 = 3.66\%$ increase | $155.52 * 255/246 = 155.52 * 85/82 = 161.21$ |
| 3 bytes per 255-byte block | $255/248 = 2.82\%$ increase | $155.52 * 255/248 = 159.91$ |

Figure 4. S3067 Transceiver Functional Block Diagram

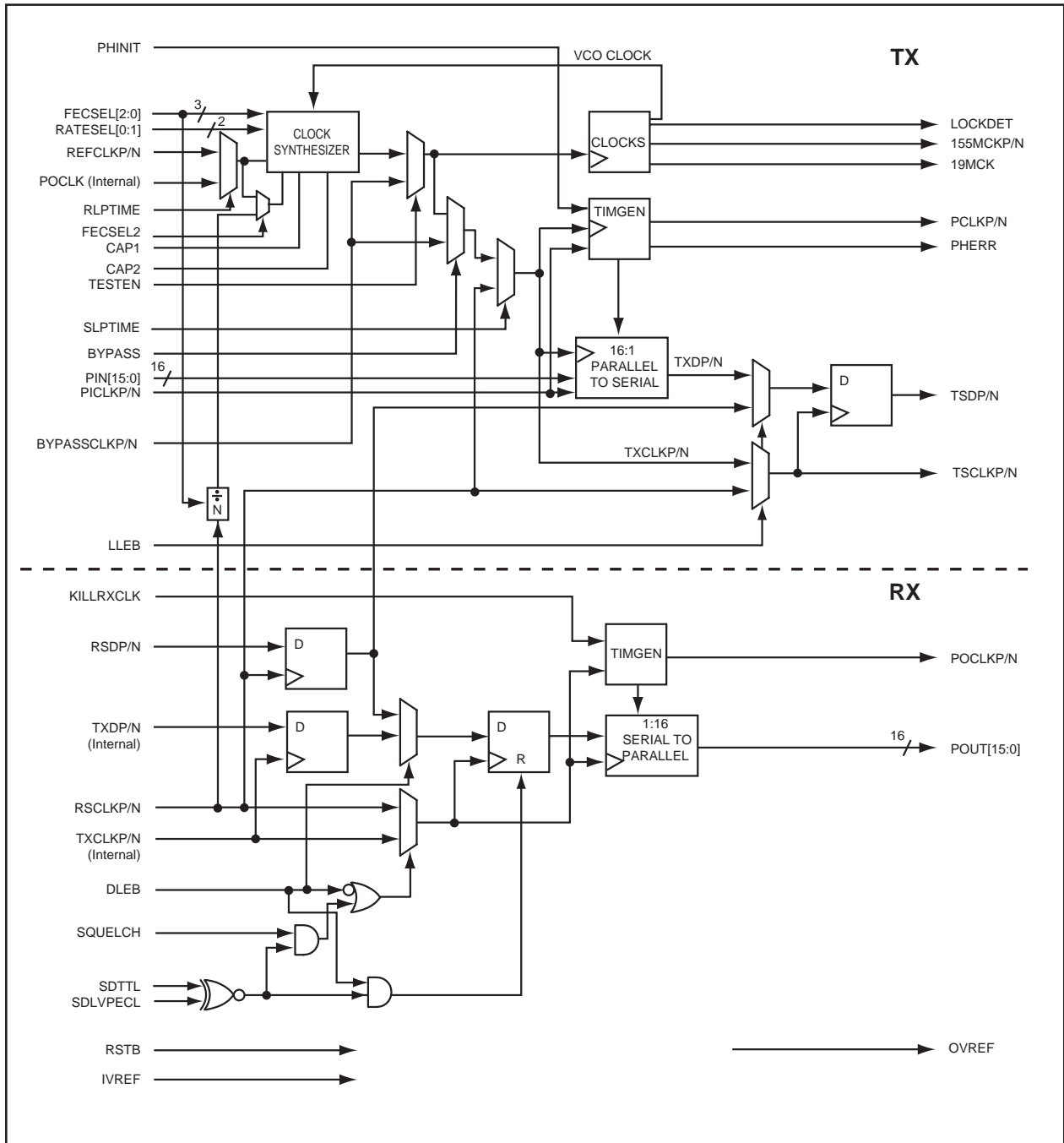
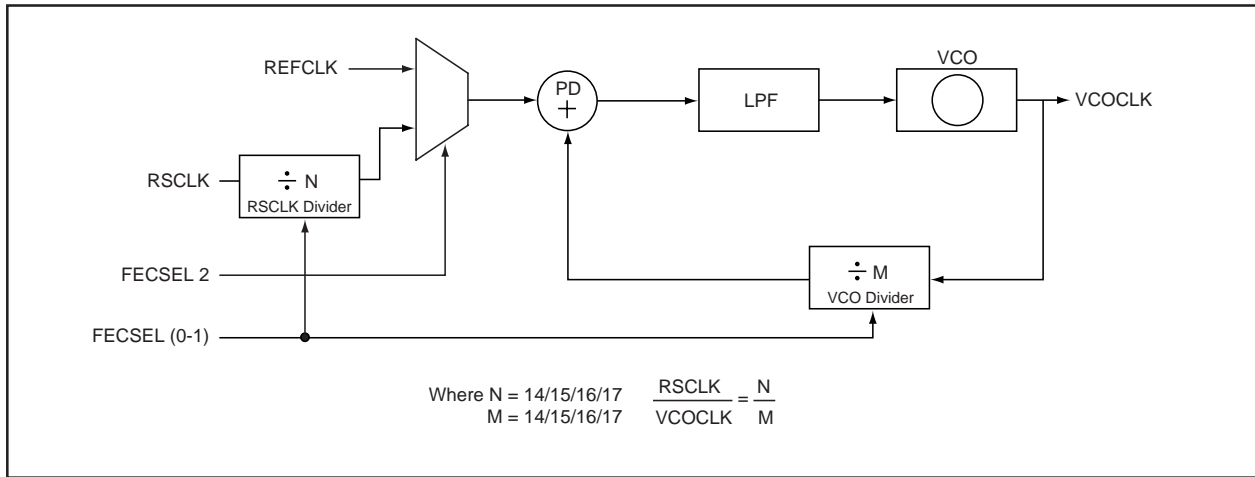


Figure 5. Clock Synthesizer



A high on FECSEL2 selects RSCLK divided by N. A low on FECSEL2 selects the REFCLK. The REFCLK or RSCLK divided by N is divided by 1/M (multiplied by M) in the loop. The value of M and N can be selected by FECSEL0 and FECSEL1.

When FECSEL2 = 0, VCOCLK = REFCLK * M. The user must select the proper value of REFCLK and M to get the desired VCOCLK frequency. When FECSEL2 = 1, VCOCLK = (RSCLK * M) ÷ N. The user must select the proper M/N ratio (with FECSEL0 and FECSEL1) to get the desired VCOCLK value. (See Tables 3 and 4.)

Example: OC-48 FEC capability of 8 bytes per 255-byte block. Required VCOCLK = 2.6656 GHz.

Method 1:

Required VCOCLK = 2.6656 GHz
 FECSEL2 = 0, selects REFCLK
 FECSEL0 = 1 and FECSEL1 = 0, selects VCO divider(M) = 16
 REFCLK = 2.6656 GHz ÷ 16 = 166.60 MHz
 VCOCLK = REFCLK ÷ (1/M) = 166.60 * 16 = 2.6656 GHz

Method 2:

Required VCOCLK = 2.6656 GHz
 FECSEL2 = 1, selects RSCLK
 FECSEL0 = 0 and FECSEL1 = 0, selects VCO divider(M) = 17 and RSCLK divider(N) = 16
 RSCLK = (2.6656 * 16) ÷ 17 = 2.5088 GHz
 VCOCLK = RSCLK ÷ N ÷ (1/M) = 2.5088 GHz ÷ 16 * 17 = 2.6656 GHz.

S3067 TRANSCEIVER FUNCTIONAL DESCRIPTION

Transmitter Operation

The S3067 transceiver chip performs the serialization stage in the processing of a transmit SONET STS-48/STS-24/STS-12/STS-3/GBE/FC data stream depending on the data rate selected. It converts 16-bit parallel data to bit serial format.

A high-frequency bit clock can be generated from a 131.25 MHz to 178 MHz frequency reference by using an integral frequency synthesizer consisting of a phase-locked loop circuit with a divider in the loop.

Diagnostic loopback (transmitter to receiver) and line loopback (receiver to transmitter) is provided. See *Other Operating Modes*.

The bypass signal selects between the BYPASSCLK and the VCO clock. BYPASSCLK can be used to provide an alternative clock to the internal VCO when the user selects an error correcting capability which is not provided by the S3067 dividers. The user must provide the required frequency for the BYPASSCLK when error-correcting capability of 6/5/4/3 bytes per 255-byte block is selected.

Clock Synthesizer

The clock synthesizer, shown in the block diagrams of Figures 4 and 5, is a monolithic PLL that generates the serial output clock frequency locked to the input Reference Clock (REFCLKP/N).

The REFCLKP/N input must be generated from a crystal oscillator that has a frequency accuracy better than the value stated in Table 10 in order for the TSCLK frequency to have the accuracy required for operation in a SONET system. Lower-accuracy crystal oscillators may be used in applications less demanding than SONET/SDH.

The on-chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the REFCLKP/N input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The divide by 'N' and divide by 'M' provide the counters required to support error correcting capability. The values of 'N' and 'M' can be selected by FECSEL lines.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. A single external clean-up capacitor is utilized as part of the loop filter. The loop filter's corner frequency is optimized to minimize output phase jitter.

Timing Generator

The timing generation function, seen in Figure 4, provides a divide-by-16 version of the transmit serial clock. This circuitry also provides an internally generated load signal, which transfers the PIN[15:0] data from the parallel input register to the serial shift register.

The PCLK output is a divide-by-16 rate version of transmit serial clock (divide-by-16). PCLK is intended for use as a divide-by-16 clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3067 device.

The timing generator also produces a feedback reference clock to the clock synthesizer. A counter divides the synthesized clock down to the same frequency as the reference clock REFCLK. The PLL in the clock synthesizer maintains the stability of the synthesized clock by comparing the phase of the internal clock with that of the Reference Clock (REFCLK).

Table 5. Reference Jitter Limits

| Operating Mode | Band Width | RMS Jitter |
|----------------|------------------|------------|
| STS-48 | 12 kHz to 20 MHz | -61 dBc |
| STS-24 | 12 kHz to 10 MHz | 2 ps |
| STS-12 | 12 kHz to 5 MHz | 4 ps |
| STS-3 | 12 kHz to 1 MHz | 16 ps |

Parallel-to-Serial Converter

The parallel-to-serial converter shown in Figure 4 is comprised of a FIFO and a parallel-to-serial register. The FIFO input latches the data from the PIN[15:0] bus on the rising edge of PCLK. The parallel-to-serial register is a loadable shift register which takes its parallel input from the FIFO output.

An internally generated divide-by-16 clock, which is phase aligned to the transmit serial clock as described in the *Timing Generator* description, activates the parallel data transfer between registers. The serial data is shifted out of the parallel-to-serial register at the TSCLK rate.

FIFO

A FIFO is added to decouple the internal and external (PCLK) clocks. The internally generated divide-by-16 clock is used to clock out data from the FIFO. PHINIT and LOCKDET are used to center or reset the FIFO. The PHINIT and LOCKDET signals will center the FIFO after the third PCLK pulse. This is to insure that PCLK is stable. This scheme allows the user to have an infinite PCLK-to-PCLK delay through the ASIC. Once the FIFO is centered, the PCLK-to-PCLK delay can have a maximum drift as specified in Table 20.

FIFO Initialization

The FIFO can be initialized in one of the following three ways:

1. During power up, once the PLL has locked to the reference clock provided on the REFCLK pins, the LOCKDET will go active and initialize the FIFO.
2. When RSTB goes active, the entire chip is reset. This causes the PLL to go out of lock and thus the LOCKDET goes inactive. When the PLL reacquires the lock, the LOCKDET goes active and initializes the FIFO. Note: PCLK is held reset when RSTB is active.
3. The user can also initialize the FIFO by raising PHINIT.

During the normal running operation, the incoming data is passed from the PCLK timing domain to the internally generated, divide-by-16 clock timing domain. Although the frequency of PCLK and the

internally generated clock is the same, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two timing domains, the timing generator circuitry monitors the phase relationship between PCLK and the internally generated clock. When a potential setup or hold time violation is detected, the phase error goes high. When PHERR conditions occur, PHINIT should be activated to recenter the FIFO (at least 2 PCLK periods). This can be done by connecting PHERR to PHINIT. When realignment occurs, up to 10 bytes of data will be lost. The user can also take in the PHERR signal, process it and send an output to PHINIT in such a way that idle bytes are lost during the realignment process. PHERR will go inactive when the realignment is complete.

Receiver Operation

The S3067 receiver chip provides the first stage of digital processing of a receive SONET STS-48/STS-24/STS-12/STS-3/GBE/FC bit-serial stream. The bit-serial data stream is then converted into a 16-bit half-word data format. A loopback mode is provided for diagnostic loopback (transmitter to receiver). A line loopback (receiver to transmitter) is also provided. Both line and local loopback modes can be active at the same time.

Serial-to-Parallel Converter

The serial-to-parallel converter consists of two 16-bit registers. The first is a serial-in, parallel-out shift register, which performs the serial-to-parallel conversion clocked by the clock recovery block. On the falling edge of the POCLK, the data in the parallel register is transferred to an output parallel register which drives POUT[15:0].

OTHER OPERATING MODES

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is low, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. The differential serial output data from the transmitter is routed to the serial-to-parallel block in place of the normal data stream (RSD). TSD/TSCLK outputs are active. DLEB takes precedence over SDPECL and SDTTL.

Line Loopback

The line loopback circuitry selects the source of the data and clock which is output on TSD and TSCLK. When the Line Loopback Enable input (LLEB) is high, it selects data and clock from the parallel-to-serial converter block. When LLEB is low, it forces the output data multiplexer to select the data and clock from the RSD and RSCLK inputs, and a receive-to-transmit loopback can be established at the serial data rate. Diagnostic loopback and line loopback can be active at the same time.

Loop Timing

In Serial Loop Timing mode (SLPTIME), the clock synthesizer PLL of the S3067 is bypassed, and the timing of the entire transmitter section is controlled by the Receive Serial Clock, RSCLKP/N. This mode is entered by setting the SLPTIME input to a TTL high level.

In this mode, the REFCLKP/N input is not used, and the RATESEL input is ignored for all transmit functions. It should be carefully noted that the internal PLL continues to operate in this mode and continues as the source for the 19MCK and 155MCK. Therefore these signals are being used (e.g. as the reference for an external S3076 clock recovery device), the REFCLKP/N and RATESEL inputs must be properly driven.

In Reference Loop Timing mode (RLPTIME), the Parallel Clock from the receiver (POCLK) is used as the reference clock to the transmitter. In this mode, the REFCLKP/N input is not used. The 19MCK and 155MCK are generated from the POCLK in this operating mode. When operating the S3067 in RLPTIME mode, the 19MCK and 155MCK outputs should not be used as the back-up reference clock for a clock and data recovery device (S3066, S3040). When performing loopback testing (DLEB), the S3067 must not be in RLPTIME.

Squelched Clock Operation

Some integrated optical receiver/clock recovery modules force their recovered serial receive clock output to the logic zero state if the optical signal is removed or reduced below a fixed threshold. This condition is accompanied by the expected deassertion of the Signal Detect (SD) output.

The S3067 has been designed for operation with clock recovery devices that provide continuous serial clock for seamless downstream clocking in the event of optical signal loss.

For operation with an optical transceiver that provides the *Squelched Clock* behavior as described above, the S3067 can be operated in the *Squelched Clock* mode by activating the SQUELCH pin.

In this condition, the Receive Serial Clock (RSCLKP/N) is used for all receiver timing when the SDLVPECL/SDTTL inputs are in the active state. When the SDLVPECL/SDTTL inputs are placed in the inactive state (usually by the deassertion of LOCKDET or Signal Detect from the optical transceiver/clock recovery unit), the transmitter serial clock will be used to maintain timing in the receiver section. This will allow the POCLK to continue to run and the parallel outputs to flush out the last received characters and then assume the all-zero state imposed at the serial data input.

It is important to note that in this mode there will be a one-time shortening or lengthening of the POCLK cycle, resulting in an apparent phase shift in the POCLK at the deassertion of the SD condition. Another similar phase shift will occur when the SD condition is reasserted.

In the normal operating mode, with SQUELCH inactive, there will be no phase discontinuities at the POCLK output during signal loss or reacquisition (assuming operation with continuous clocking from the CRU device such as the AMCC S3076).

Table 6. S3067 Transmitter Pin Assignment and Descriptions

| Pin Name | Level | I/O | Pin # | Description |
|--|--------------------------------|-----|--|--|
| PIN0 PIN1 PIN2 PIN3 PIN4 PIN5 PIN6 PIN7 PIN8 PIN9 PIN10 PIN11 PIN12 PIN13 PIN14 PIN15 | Single Ended LVPECL | I | A2 B3 B2 C3 A1 C2 B1 D2 E3 C1 E2 F3 F2 E1 F1 G3 | Parallel Data Input. A divide-by-16, aligned to the PCLK, parallel input clock. PIN[15] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PIN[0] is the least significant bit (corresponding to bit 16 of each PCM word, the last bit transmitted). PIN[15:0] is sampled on the rising edge of PCLK. |
| PICKP PICKN | Internally Biased Diff. LVPECL | I | A4 A3 | Parallel Input Clock. A divide-by-16, nominally 50% duty cycle input clock, to which PIN[15:0] is aligned. PCLK is used to transfer the data on the PIN inputs into a holding register in the parallel-to-serial converter. The rising edge of PCLK samples PIN[15:0]. |
| CAP1 CAP2 | Analog | I | R5 T5 | Loop Filter Capacitor. The external loop filter capacitor and resistors are connected to these pins. See Figure 26. |
| IVREF | DC | I | C4 | Single-ended LVPECL input reference voltage. |
| PHINIT | Single Ended LVPECL | I | G2 | Phase Initialization. Rising edge will realign internal timing. |
| TSDP TSDN | Diff. CML | O | R11 R12 | Transmit Serial Data. Differential CML serial data stream signals, normally connected to an optical transmitter module. |
| TSCLKP TSCLKN | Diff. CML | O | R8 R9 | Transmit Serial Clock. Differential CML TSCLKP/N can be used to retime the TSD signal. This clock frequency will be selected by RATESEL and FECSEL. |
| PCLKP PCLKN | Diff. LVPECL | O | C6 B6 | A reference clock generated by dividing the internal bit clock by 16. It is normally used to coordinate word-wide transfers between upstream logic and the S3067 device. |
| PHERR | Single Ended LVPECL | O | A5 | Phase Error. Pulses High during each PCLK cycle for which there is a potential set-up/hold timing violation between the internal byte clock and PCLK timing domains. PHERR is updated on the falling edge of the PCLK outputs. |

Table 7. S3067 Receiver Pin Assignment and Descriptions

| Pin Name | Level | I/O | Pin # | Description |
|--|---------------------------|-----|--|---|
| RSDP RSDN | Diff. CML | I | H15 G15 | Differential CML Receive Serial Data stream signals normally connected to an optical receiver module. Internally biased and terminated. |
| SDLVPECL | Single Ended LVPECL | I | N16 | LVPECL Signal Detect. LVPECL with internal pull-down. Active High when SDTTL is held at logic 0. A single-ended 10K LVPECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDLVPECL is inactive, the data on the Receive Serial Data In (RSDP/N) pins will be internally forced to a constant zero. When SDLVPECL is active, data on the RSDP/N pins will be processed normally. When SDTTL is to be connected to the optical receiver module instead of SDLVPECL, then SDLVPECL should be tied High to implement an active Low Signal Detect, or left unconnected to implement an active High Signal Detect. |
| SDTTL | LVTTTL | I | P16 | LVTTTL Signal Detect. Active High when SDLVPECL is unconnected (logic 0). Active Low when SDLVPECL is held at logic 1. A single-ended LVTTTL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDTTL is inactive, the data on the RSDP/N pins will be internally forced to a constant zero. When SDTTL is active, data on the RSDP/N pins will be processed normally. |
| RSCLKP RSCLKN | Diff. CML | I | L15 K15 | Receive Serial Clock. Used to supply a clock input for the RSDP/N inputs. Internally biased and terminated. |
| POUT0 POUT1 POUT2 POUT3 POUT4 POUT5 POUT6 POUT7 POUT8 POUT9 POUT10 POUT11 POUT12 POUT13 POUT14 POUT15 | Single Ended LVPECL | O | F14 E16 D16 E14 C16 D15 D14 C15 B15 A14 C13 A13 C12 B12 C11 B11 | Parallel data output bus, a divide by 16, aligned to the POCLK parallel output clock. POUT15 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUT0 is the least significant bit. POUT[15:0] is updated on the falling edge of POCLK. |
| POCLKP POCLKN | Diff. LVPECL | O | B10 C10 | Parallel Output Clock. A divide by 16, nominally 50% duty cycle, output clock that is aligned to POUT [15:0] word serial output data. POUT[15:0] is updated on the falling edge of POCLK. |
| OVREF | DC | O | B14 | Single-ended LVPECL reference voltage. Tracks midswing voltage of parallel output data bus. |

Table 8. S3067 Common Pin Assignment and Descriptions

| Pin Name | Level | I/O | Pin # | Description |
|--------------------|--------------------------------|-----|------------|---|
| SQUELCH | LVTTTL | I | R16 | RSCLK Clock Squelch. Active High. When SQUELCH is active and SD is inactive, the transmit clock will be used in place of the RSCLK. |
| REFCLKP REFCLKN | Internally Biased Diff. LVPECL | I | M2 L3 | Reference Clock Input. Used as the reference for the internal bit clock frequency synthesizer. |
| DLEB | LVTTTL | I | N15 | Diagnostic Loopback Enable. Active Low. Selects diagnostic loopback. When DLEB is High, the S3067 device uses the primary data (RSD) and clock (RSCLK) inputs. When Low, the S3067 device uses the diagnostic loopback clock and data from the transmitter. TSD/TSCLK are active in DLEB. |
| LLEB | LVTTTL | I | N14 | Line Loopback Enable. Active Low. Selects line loopback. When LLEB is Low, the S3067 will route the data from the RSD/RSCLK inputs to the TSD/TSCLK outputs. |
| KILLRXCLK | LVTTTL | I | M14 | Kill Receive Clock Input. For normal operation, KILLRXCLK is High. When this input is Low, it will force POCLK output to a logic "0" state. |
| SLPTIME | LVTTTL | I | T1 | Serial Clock Loop Time Select input. Active High. When High, SLPTIME enables the recovered clock from the receive section to be used in place of the synthesized transmit clock. |
| RLPTIME | LVTTTL | I | T2 | Reference Clock Looptime Select input. Active High. When High, RLPTIME enables POCLK from the receiver to be used as the reference clock input to the transmitter. |
| RSTB | LVTTTL | I | P15 | Master Reset. Reset input for the device, Active Low. During Reset, all clocks are disabled. |
| TESTEN | LVTTTL | I | N2 | Test Enable. Used for production testing. Low for normal operation. |
| 155MCKP 155MCKN | Diff. LVPECL | O | R14 T15 | VCO ÷ by 16 Clock Output from the clock synthesizer. This output should be connected to the reference clock input of the external clock recovery function (such as the S3066). It is recommended to tie 155MCKP/N to VCC when not used. |
| 19MCK | Single Ended LVPECL | O | P14 | VCO ÷ by 128 Clock Output from the clock synthesizer. This output should be connected to the reference clock input of the external clock recovery function. It is recommended to tie 19MCK to VCC when not used. |
| LOCKDET | LVTTTL | O | H1 | Lock Detect. Active High. Goes active after the PLL has locked to the clock provided on the REFCLK pins. LOCKDET is an asynchronous output. |

Table 8. S3067 Common Pin Assignment and Descriptions (Continued)

| Pin Name | Level | I/O | Pin # | Description |
|--------------------------|---------------------|-----|---|--|
| RATESEL0 RATESEL1 | LVTTTL | I | R2 P3 | Rate Select. Selects the operating mode. (See Table 2.) |
| BYPASSCLKP BYPASSCLKN | Differential CML | I | K2 J2 | Bypass Clock. Provides an alternative serial clock bypassing the internal VCO. |
| BYPASS | LVTTTL | I | M3 | Active High. Selects between BYPASS clock and the VCO clock. |
| FECSEL [2:0] | LVTTTL | I | R1, P2, N3 | FEC Select. Selects the error correcting capability. (See Table 3.) |
| AGND | GND | | P4, P5, R4, R6, T6 | Ground (0V) |
| AVCC | +3.3V | | P6, T3, T4 | Power Supply |
| LVPECLPOW | +3.3V | | A6, A10, A12, B4, C14, D1, E15, G14, J1, K3, L14, N1, P8, P9, P10, P12, R15 | Power Supply |
| LVPECLGND | GND | | A11, B5, B13, B16, C5, D3, F15, F16, G1, H2, H14, J3, K14, M1, P7, R7, T14 | Ground (0V) |
| COREPOW | +3.3V | | A7, A9, J16, L2, P13 | Power Supply |
| COREGND | GND | | A8, B8, K16, L1, T13 | Ground (0V) |
| TTLPOW | +3.3V | | P1, T16 | Power Supply |
| TTLGND | GND | | M15, R3 | Ground (0V) |
| TCGND | GND | | T7, T9 | Ground (0V) |
| TDGND | GND | | R10, T12 | Ground (0V) |
| NC | | | A15, A16, B7, B9, C7, C8, C9, H3, G16, H16, J14, J15, K1, L16, M16, P11, R13, T8, T10, T11 | Not Connected |

Figure 6. S3067 Pinout-Bottom View

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | | | | | | | | | | |
|----|------------|------------|------------|-------------------------------------|-------|-------|------------|------------|-------------|-------------|----------|------------|------------|------------|------------|------------|------------|------------|----------|------------|------------|------------|-----------|-------|------------|------------|
| 1 | PIN4 | PIN6 | PIN9 | LVPECL POW | PIN13 | PIN14 | LVPECL GND | LOCKDET | LVPECL POW | NC | CORE GND | LVPECL GND | LVPECL POW | TTLPOW | FECSEL2 | SLPTIME | | | | | | | | | | |
| 2 | PIN0 | PIN2 | PIN5 | PIN7 | PIN10 | PIN12 | PHINIT | LVPECL GND | BYPASS CLKN | BYPASS CLKP | CORE POW | REFCLKP | TESTEN | FECSEL1 | RATE SEL0 | RLPTIME | | | | | | | | | | |
| 3 | PICLKN | PIN1 | PIN3 | LVPECL GND | PIN8 | PIN11 | PIN15 | NC | LVPECL GND | LVPECL POW | REFCLKN | BYPASS | FECSEL0 | RATE SEL1 | TTLGND | AVCC | | | | | | | | | | |
| 4 | PICLKP | LVPECL POW | IVREF | 156 Pin TBGA BOTTOM VIEW | | | | | | | | | | AGND | AGND | AVCC | | | | | | | | | | |
| 5 | PHERR | LVPECL GND | LVPECL GND | | | | | | | | | | | AGND | CAP1 | CAP2 | | | | | | | | | | |
| 6 | LVPECL POW | PCLKN | PCLKP | | | | | | | | | | | AVCC | AGND | AGND | | | | | | | | | | |
| 7 | CORE POW | NC | NC | | | | | | | | | | | LVPECL GND | LVPECL GND | TCGND | | | | | | | | | | |
| 8 | CORE GND | CORE GND | NC | | | | | | | | | | | LVPECL POW | TSCLKP | NC | | | | | | | | | | |
| 9 | CORE POW | NC | NC | | | | | | | | | | | LVPECL POW | TSCLKN | TCGND | | | | | | | | | | |
| 10 | LVPECL POW | POCLKP | POCLKN | | | | | | | | | | | LVPECL POW | TDGND | NC | | | | | | | | | | |
| 11 | LVPECL GND | POUT15 | POUT14 | | | | | | | | | | | NC | TSDP | NC | | | | | | | | | | |
| 12 | LVPECL POW | POUT13 | POUT12 | | | | | | | | | | | LVPECL POW | TSDN | TDGND | | | | | | | | | | |
| 13 | POUT11 | LVPECL GND | POUT10 | | | | | | | | | | | CORE POW | NC | CORE GND | | | | | | | | | | |
| 14 | POUT9 | OVREF | LVPECL POW | | | | | | | | | | | POUT6 | POUT3 | POUT0 | LVPECL POW | LVPECL GND | NC | LVPECL GND | LVPECL POW | KILLRX CLK | LLEB | 19MCK | 155MCKP | LVPECL GND |
| 15 | NC | POUT8 | POUT7 | | | | | | | | | | | POUT5 | LVPECL POW | LVPECL GND | RSDN | RSDP | NC | RSCLKN | RSCLKP | TTLGND | DLEB | RSTB | LVPECL POW | 155MCKN |
| 16 | NC | LVPECL GND | POUT4 | | | | | | | | | | | POUT2 | POUT1 | LVPECL GND | NC | NC | CORE POW | CORE GND | NC | NC | SDLV PECL | SDTTL | SQUELCH | TTLPOW |



S3067 MULTIRATE (OC-48/24/12/3/GBE/FC) SONET/SDH/ATM TRANSCEIVER w/ FEC

Figure 7. S3067 Pinout-Top View

| T | R | P | N | M | L | K | J | H | G | F | E | D | C | B | A | |
|------------|------------|------------|----------------------------------|------------|------------|-------------|-------------|------------|------------|------------|------------|------------|------------|------------|------------|----|
| SLPTIME | FECSEL2 | TTLPOW | LVPECL POW | LVPECL GND | CORE GND | NC | LVPECL POW | LOCKDET | LVPECL GND | PIN14 | PIN13 | LVPECL POW | PIN9 | PIN6 | PIN4 | 1 |
| RLPTIME | RATE SEL0 | FECSEL1 | TESTEN | REFCLKP | CORE POW | BYPASS CLKP | BYPASS CLKN | LVPECL GND | PHINIT | PIN12 | PIN10 | PIN7 | PIN5 | PIN2 | PIN0 | 2 |
| AVCC | TTLGND | RATE SEL1 | FECSEL0 | BYPASS | REFCLKN | LVPECL POW | LVPECL GND | NC | PIN15 | PIN11 | PIN8 | LVPECL GND | PIN3 | PIN1 | PICLKN | 3 |
| AVCC | AGND | AGND | 156 Pin TBGA TOP VIEW | | | | | | | | | | IVREF | LVPECL POW | PICLKP | 4 |
| CAP2 | CAP1 | AGND | | | | | | | | | | | LVPECL GND | LVPECL GND | PHERR | 5 |
| AGND | AGND | AVCC | | | | | | | | | | | PCLKP | PCLKN | LVPECL POW | 6 |
| TCGND | LVPECL GND | LVPECL GND | | | | | | | | | | | NC | NC | CORE POW | 7 |
| NC | TSCLKP | LVPECL POW | | | | | | | | | | | NC | CORE GND | CORE GND | 8 |
| TCGND | TSCLKN | LVPECL POW | | | | | | | | | | | NC | NC | CORE POW | 9 |
| NC | TDGND | LVPECL POW | | | | | | | | | | | POCLKN | POCLKP | LVPECL POW | 10 |
| NC | TSDP | NC | | | | | | | | | | | POUT14 | POUT15 | LVPECL GND | 11 |
| TDGND | TSDN | LVPECL POW | | | | | | | | | | | POUT12 | POUT13 | LVPECL POW | 12 |
| CORE GND | NC | CORE POW | | | | | | | | | | | POUT10 | LVPECL GND | POUT11 | 13 |
| LVPECL GND | 155MCKP | 19MCK | LLEB | KILLRX CLK | LVPECL POW | LVPECL GND | NC | LVPECL GND | LVPECL POW | POUT0 | POUT3 | POUT6 | LVPECL POW | OVREF | POUT9 | 14 |
| 155MCKN | LVPECL POW | RSTB | DLEB | TTLGND | RSCLKP | RSCLKN | NC | RSDP | RSDN | LVPECL GND | LVPECL POW | POUT5 | POUT7 | POUT8 | NC | 15 |
| TTLPOW | SQUELCH | SDTTL | SDLV PECL | NC | NC | CORE GND | CORE POW | NC | NC | LVPECL GND | POUT1 | POUT2 | POUT4 | LVPECL GND | NC | 16 |

Figure 8. 156 Pin TBGA Package

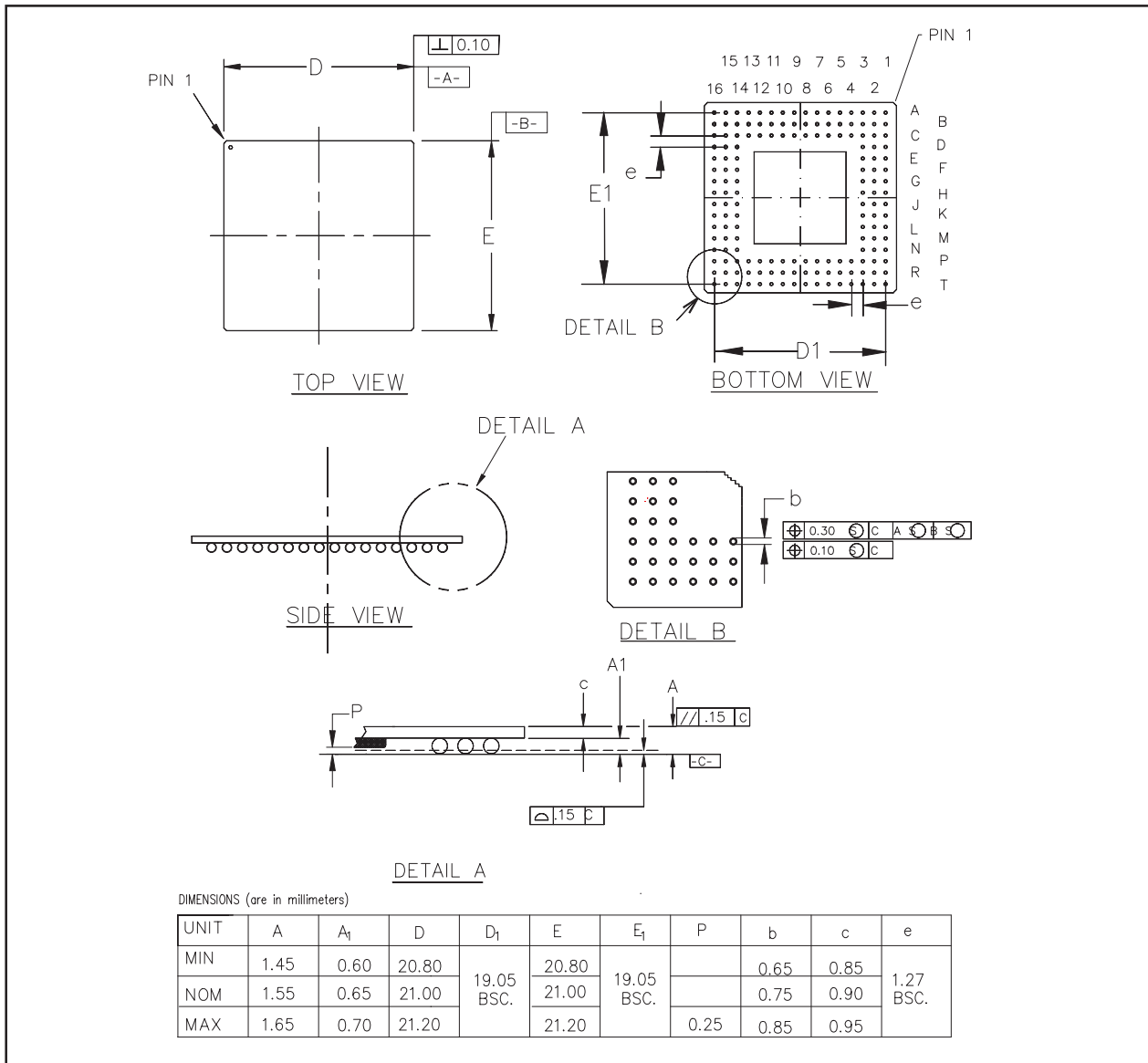


Table 9. Thermal Management

| Device | Max Package Power | Θ_{ja} (Still Air) | Θ_{jc} | Conditions |
|--------|-------------------|---------------------------|---------------|--|
| S3067 | 2.5 W | 18.6° C/W | 1° C/W | Commercial use only (0 to 70° C). |
| S3067 | 2.5 W | 15.8° C/W | | Industrial use. 100 LFPM airflow. |
| S3067 | 2.5 W | 14.57° C/W | | Industrial use (-20 to 85° C). HTS278D heatsink from chip coolers. |

Table 10. Performance Specifications

| Parameter | Min | Typ | Max | Units | Conditions |
|---|------|-----|--------------------------------------|----------|--|
| Nominal VCO Center Frequency | 2.10 | | 2.67 | GHz | |
| Output Jitter STS-48 STS-24/Gigabit Ethernet (Not tested) STS-12 STS-3 | | | 0.005 0.005 0.005 0.005 | UI (rms) | Note: Output jitter measured at SONET operating rate using appropriate filter. rms jitter, in lock. |
| Reference Clock Frequency Tolerance | -100 | | +100 | ppm | ± 20 is required to meet SONET output frequency specification. |
| Reference Clock Input Duty Cycle | 45 | | 55 | % | |
| Reference Clock Rise and Fall Times | | | 1.5 | ns | 10% to 90% of amplitude. |

Table 11. Absolute Maximum Ratings

| Parameter | Min | Typ | Max | Units |
|--|------|-----|-----------------|-------|
| Storage Temperature | -65 | | 150 | ° C |
| Voltage on V _{CC} with respect to GND | -0.5 | | +3.6 | V |
| Voltage on any LVPECL Input Pin | 0 | | V _{CC} | V |
| High Speed LVPECL Output Source Current | | | 24 | mA |

ESD Ratings

The S3067 is rated to the following voltages based on the human body model:

1. All pins are rated above 200 V.

Table 12. Recommended Operating Conditions

| Parameter | Min | Typ | Max | Units |
|--|--------------------|-----|-----------------|-------|
| Ambient Temperature Under Bias | -20 | | 85 | ° C |
| Voltage on V _{CC} with respect to GND | 3.135 | 3.3 | 3.465 | V |
| Voltage on any LVPECL Input Pin | V _{CC} -2 | | V _{CC} | V |
| Voltage on any LVTTTL Input Pin | 0 | | V _{CC} | V |
| ICC ¹ | | 455 | 606 | mA |

1. Outputs unterminated.

Table 13. LVTTTL Input/Output DC Characteristics

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|-----------|---------------------|------|-----|--------------|---------------|--|
| V_{IH} | Input High Voltage | 2.0 | | TTL V_{CC} | V | TTL $V_{CC} = \text{Max}$ |
| V_{IL} | Input Low Voltage | 0.0 | | 0.8 | V | TTL $V_{CC} = \text{Max}$ |
| I_{IH} | Input High Current | | | 50 | μA | $V_{IN} = 2.4 \text{ V}$ |
| I_{IL} | Input Low Current | -500 | | | μA | $V_{IN} = 0.5 \text{ V}$ |
| V_{OH} | Output High Voltage | 2.4 | | | V | $V_{CC} = \text{Min}$ $I_{OH} = -100 \mu\text{A}$ |
| V_{OL} | Output Low Voltage | | | 0.5 | V | $V_{CC} = \text{Min}$ $I_{OL} = 1.5 \text{ mA}$ |

Table 14. Internally Biased Differential LVPECL Input DC Characteristics

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|-----------------------|----------------------------------|-----------------|----------------|-----------------|-------|----------------|
| V_{IL} | LVPECL Input Low | $V_{CC} - 2.0$ | | $V_{CC} - 1.4$ | V | |
| V_{IH} | LVPECL Input High | $V_{CC} - 1.25$ | | $V_{CC} - 0.55$ | V | |
| ΔV_{INDIFF} | Diff. Input Voltage Swing | 400 | | 2400 | mV | See Figure 13. |
| $\Delta V_{INSINGLE}$ | Single Ended Input Voltage Swing | 200 | | 1200 | mV | See Figure 13. |
| V_{BIAS} | Input DC Bias | $V_{CC} - 0.65$ | $V_{CC} - 0.5$ | $V_{CC} - 0.35$ | V | |

Table 15. Differential LVPECL Output DC Characteristics

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|------------------------|-----------------------------------|-----------------|-----|-----------------|-------|--|
| $\Delta V_{OUTSINGLE}$ | Single Ended Output Voltage Swing | 500 | | 950 | mV | 51 Ω to $V_{CC} - 2$. See Figure 13. |
| $\Delta V_{OUTDIFF}$ | Diff. Output Voltage Swing | 1000 | | 1900 | mV | 51 Ω to $V_{CC} - 2$. See Figure 13. |
| V_{OH} | Output High Voltage | $V_{CC} - 1.2$ | | $V_{CC} - 0.65$ | V | 51 Ω to $V_{CC} - 2$ |
| V_{OL} | Output Low Voltage | $V_{CC} - 1.95$ | | $V_{CC} - 1.50$ | V | 51 Ω to $V_{CC} - 2$ |

Table 16. Single-Ended LVPECL Input DC Characteristics¹

| Parameters | Description | Min | Typ | Max | Units | Conditions |
|--------------------------|-------------------------------------|---------------------------|-----|---------------------------|-------|-----------------------|
| V _{IL} | PECL Input Low Voltage | V _{CC} -2.0 | | V _{CC} -1.5 | V | Guaranteed at -20° C. |
| V _{IL} | PECL Input Low Voltage | V _{CC} -2.0 | | V _{CC} -1.441 | V | Guaranteed at 85° C. |
| V _{IH} | PECL Input High Voltage | V _{CC} -1.2 | | V _{CC} -0.75 | V | Guaranteed at -20° C. |
| V _{IH} | PECL Input High Voltage | V _{CC} -1.023 | | V _{CC} -0.55 | V | Guaranteed at 85° C. |
| IVREF | Single-Ended LVPECL DC Bias Voltage | V _{IL} +180 | | V _{IH} -180 | mV | |
| I _I for IVREF | Maximum Input Current | | 500 | 750 | μA | |

1. The AMCC LVPECL inputs (V_{IL} and V_{IH}) are non-temperature compensated I/O which vary at 1.3 mV/°C

Table 17. Single-Ended LVPECL Output DC Characteristics¹

| Parameters | Description | Min | Typ | Max | Units | Conditions |
|--------------------------|-------------------------------------|--------------------------|-----|---------------------------|-------|--|
| V _{OL} | PECL Output Low Voltage | V _{CC} -1.98 | | V _{CC} -1.63 | V | Guaranteed at -20° C. |
| V _{OL} | PECL Output Low Voltage | V _{CC} -1.98 | | V _{CC} -1.57 | | Guaranteed at 85° C. |
| V _{OH} | PECL Output High Voltage | V _{CC} -1.1 | | V _{CC} -0.850 | V | Guaranteed at -20° C. |
| V _{OH} | PECL Output High Voltage | V _{CC} -0.95 | | V _{CC} -0.673 | | Guaranteed at 85° C. |
| OVREF | Single-Ended LVPECL DC Bias Voltage | V _{CC} -1.6 | | V _{CC} -1.20 | V | (V _{OH} -OVREF)MIN>250 mV (OVREF-V _{OL})MIN>250 mV |
| I _O for OVREF | Maximum Output Current | | 500 | 750 | μA | |

1. The AMCC LVPECL outputs are non-temperature compensated I/O which vary at 1.3 mV/°C

Table 18. CML Output DC Characteristics

| Parameter | Description | Min | Typ | Max | Units | Condition |
|-----------------------------------|--|-------------------|-----|-------------------|-------|---|
| V_{OL} (Data) | CML Output Low Voltage | V_{CC} -1.0 | | V_{CC} -0.65 | V | 100 Ω line to line. |
| V_{OH} (Data) | CML Output High Voltage | V_{CC} -0.35 | | V_{CC} -0.2 | V | 100 Ω line to line. |
| $\Delta V_{OUTDIFF}$ (Data) | CML Serial Output Differential Voltage Swing | 800 | | 1600 | mV | 100 Ω line to line. See Figure 13. |
| $\Delta V_{OUTSINGLE}$ (Data) | CML Serial Output Single-ended Voltage Swing | 400 | | 800 | mV | 100 Ω line to line at 2.5 Gbps. See Figure 13. |
| V_{OL} (Clock) | CML Output Low Voltage | V_{CC} -1.5 | | V_{CC} -0.85 | V | 100 Ω line to line. |
| V_{OH} (Clock) | CML Output High Voltage | V_{CC} -0.5 | | V_{CC} -0.25 | V | 100 Ω line to line. |
| $\Delta V_{OUTDIFF}$ (Clock) | CML Serial Output Differential Voltage Swing | 800 | | 1800 | mV | 100 Ω line to line. See Figure 13. |
| $\Delta V_{OUTSINGLE}$ (Clock) | CML Serial Output Single-ended Voltage Swing | 400 | | 900 | mV | 100 Ω line to line at 2.5 GHz. See Figure 13. |

Table 19. CML Input DC Characteristics

| Parameter | Description | Min | Typ | Max | Units | Conditions |
|-----------------------|----------------------------------|----------------|-----|----------------|----------|----------------|
| V_{IL} | CML Input Low | V_{CC} -1.7 | | V_{CC} -0.6 | V | |
| V_{IH} | CML Input High | V_{CC} -0.55 | | V_{CC} -0.15 | V | |
| ΔV_{INDIFF} | Differential Input Voltage Swing | 300 | | 2400 | mV | See Figure 13. |
| $\Delta V_{INSINGLE}$ | Single-ended Input Voltage Swing | 150 | | 1200 | mV | See Figure 13. |
| R_{DIFF} | Differential Input Resistance | 80 | 100 | 120 | Ω | |

Table 20. Transmitter AC Timing Characteristics

| Parameter | Description | Min | Max | Units |
|---------------|--|-----|-----|-------|
| | TSCLK Frequency | | 2.7 | GHz |
| | BYPASS Clock Frequency | | 2.7 | GHz |
| | TSCLK Duty Cycle | 43 | 57 | % |
| | TSCLK Duty Cycle Distortion w.r.t. RSCLK or BYPASSCLK (In SLPTIME, LLEB or BYPASS modes) | | 5.0 | % |
| | PICLK Duty Cycle | 35 | 65 | % |
| $t_{S_{PIN}}$ | PIN [15:0] Set-up Time w.r.t. PICLK (See Figure 9) | 1.5 | | ns |
| $t_{H_{PIN}}$ | PIN [15:0] Hold Time w.r.t. PICLK (See Figure 9) | 0.5 | | ns |
| $t_{P_{CLK}}$ | PCLK to PICLK drift after the FIFO is centered | | 5.2 | ns |
| $t_{S_{TSD}}$ | TSD Set-up Time w.r.t. TSCLK Rising (See Figure 9) | 100 | | ps |
| $t_{H_{TSD}}$ | TSD Hold Time w.r.t. TSCLK Rising (See Figure 9) | 100 | | ps |
| | PCLKP/N Duty Cycle | 45 | 55 | % |

Figure 9. Transmitter Input Timing¹

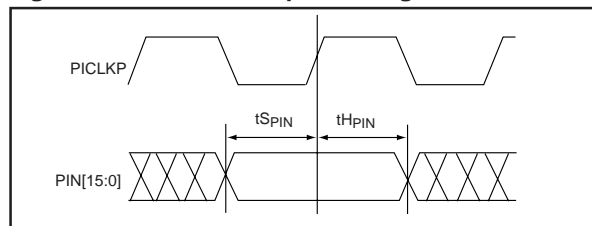
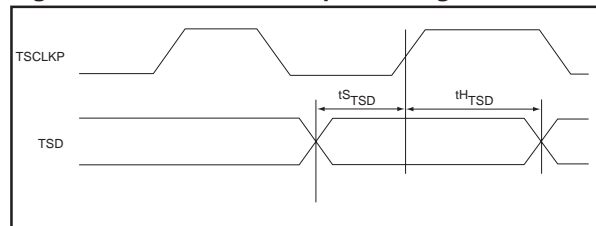


Figure 10. Transmitter Output Timing¹



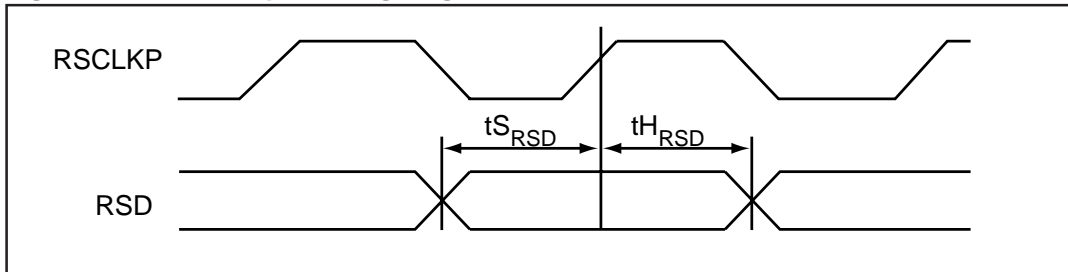
Notes on High-Speed Timing:

1. Timing is measured from the cross-over point of the reference signal to the 50% level of the input/output.

Table 21. AC Receiver Timing Characteristics

| Symbol | Description | Min | Max | Units |
|----------------|--|------|------|-------|
| | POCLK Duty Cycle | 45 | 55 | % |
| $t_{P_{POUT}}$ | POCLK Low to POUT [15:0] Valid Prop. Delay (See Figure 12) | -1.8 | +1.8 | ns |
| $t_{S_{POUT}}$ | POUT [15:0] Set-Up Time w.r.t. POCLK (2.1 GHz – 2.488 GHz) (See Figure 11) | 2.25 | | ns |
| $t_{S_{POUT}}$ | POUT[15:0] Set-up Time w.r.t. POCLK (2.488 – 2.67 GHz) (See Figure 11) | 2 | | ns |
| $t_{H_{POUT}}$ | POUT[15:0] Hold Time w.r.t. POCLK (See Figure 11) | 2 | | ns |
| $t_{S_{RSD}}$ | RSD Set-up Time w.r.t. RSCLK (See Figure 11) | 75 | | ps |
| $t_{H_{RSD}}$ | RSD Hold Time w.r.t. RSCLK (See Figure 11) | 75 | | ps |
| | RSCLK Duty Cycle | 40 | 60 | % |
| | RSCLK Frequency | | 2.7 | GHz |

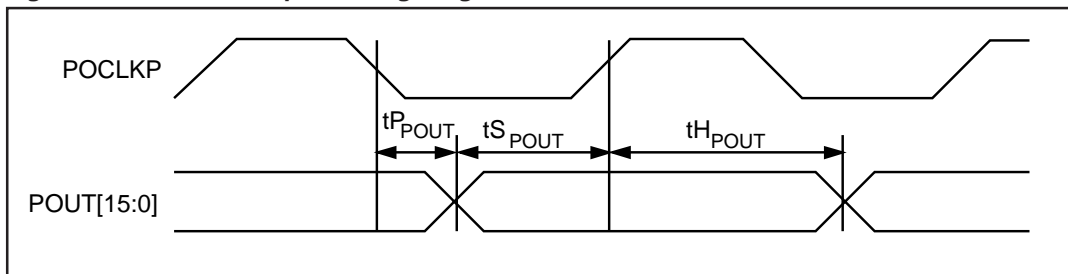
Figure 11. Receiver Input Timing Diagram¹



Notes on High-Speed LVPECL Input Timing:

1. Timing is measured from the cross-over point of the reference signal to the 50% level of the output.

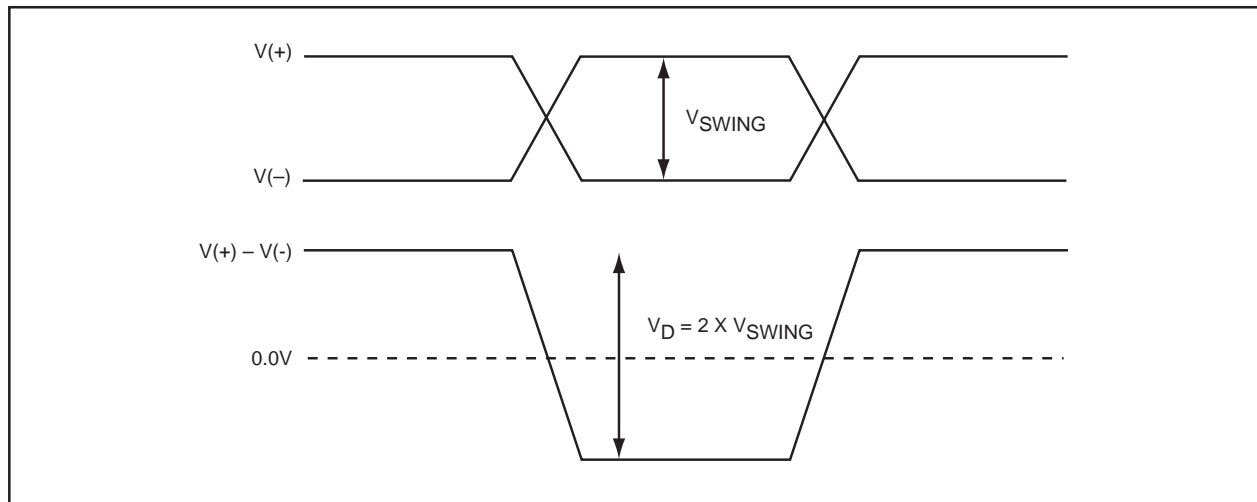
Figure 12. Receiver Output Timing Diagram¹



Notes on High-Speed LVPECL Input Timing:

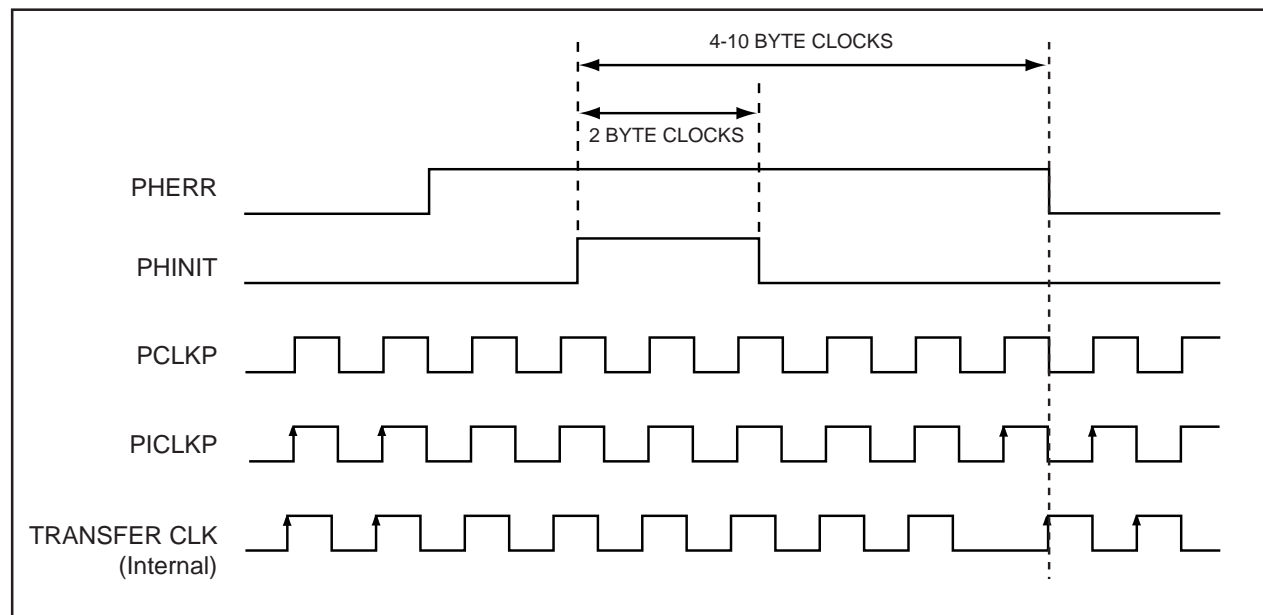
1. Timing is measured from the cross-over point of the reference signal to the 50% level of the output.

Figure 13. Differential Voltage Measurement



Note: $V(+)-V(-)$ is the algebraic difference of the input signals.

Figure 14. Phase Adjust Timing¹



1. Byte Clock = 155.52 MHz

Figure 15. S3076 to S3067 Differential CML Input Termination

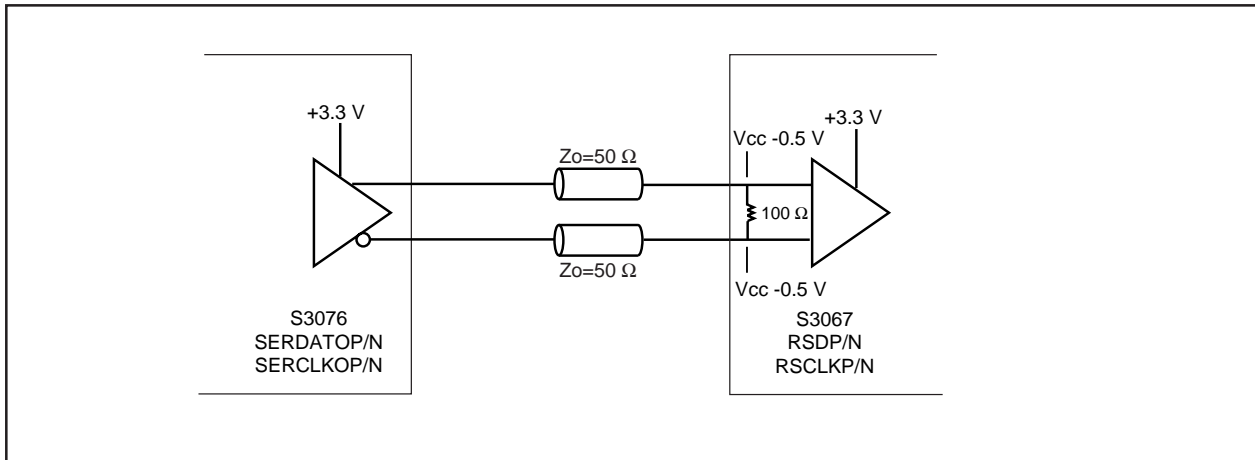


Figure 16. +5V Differential CML Driver to S3067 Differential CML Input AC Coupled Termination

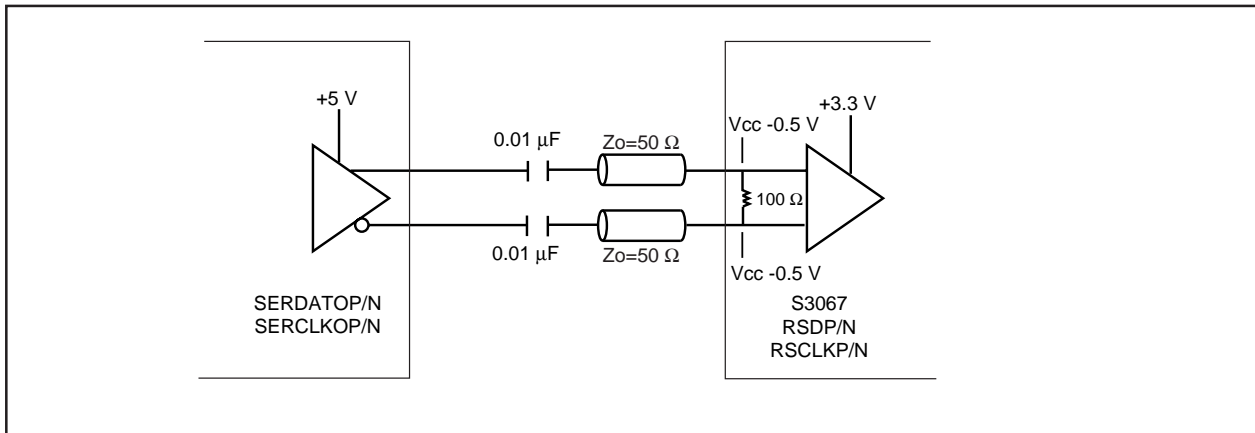


Figure 17. Single-Ended LVPECL Driver to S3067 Single-Ended LVPECL Input Termination

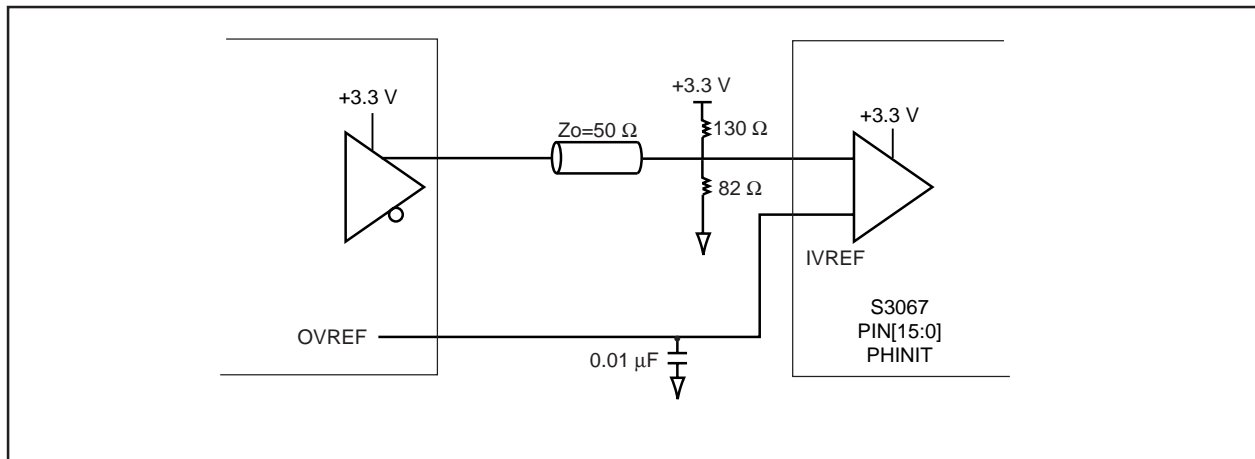


Figure 18. S3067 Differential CML Output to +5V PECL Input AC Coupled Termination

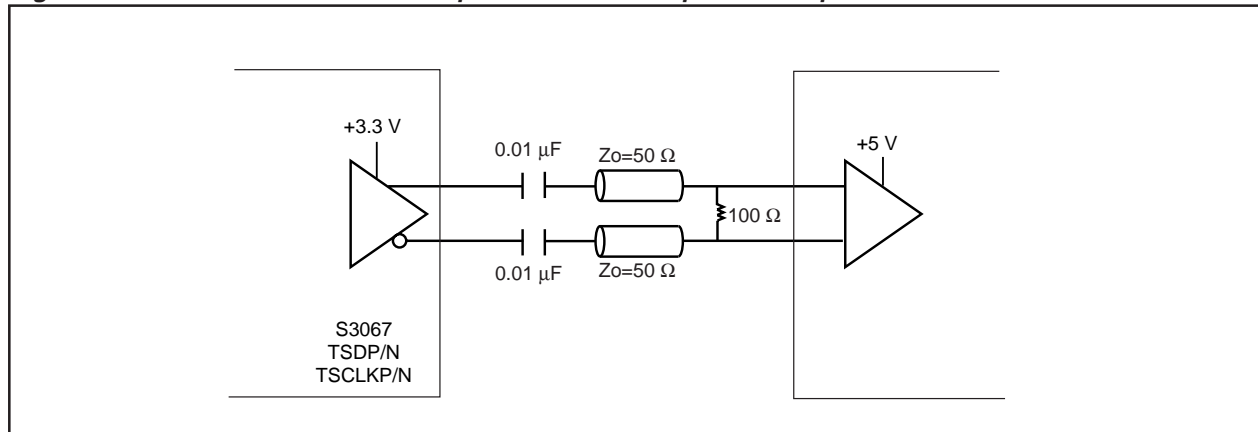


Figure 19. S3067 Single-Ended LVPECL Driver to Single-Ended LVPECL Input Termination

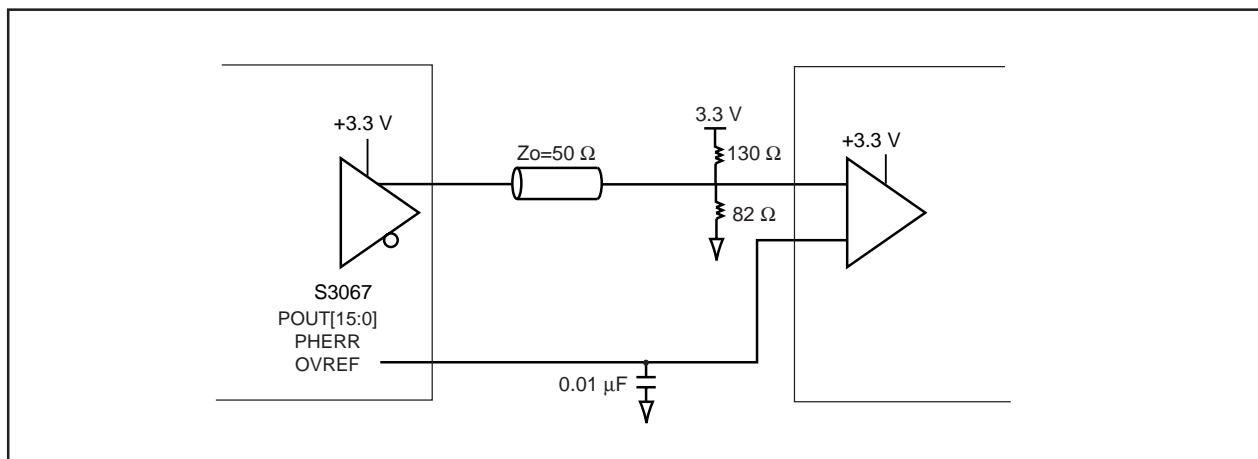


Figure 20. S3067 Single-Ended LVPECL Driver to Single-Ended LVPECL Input Termination

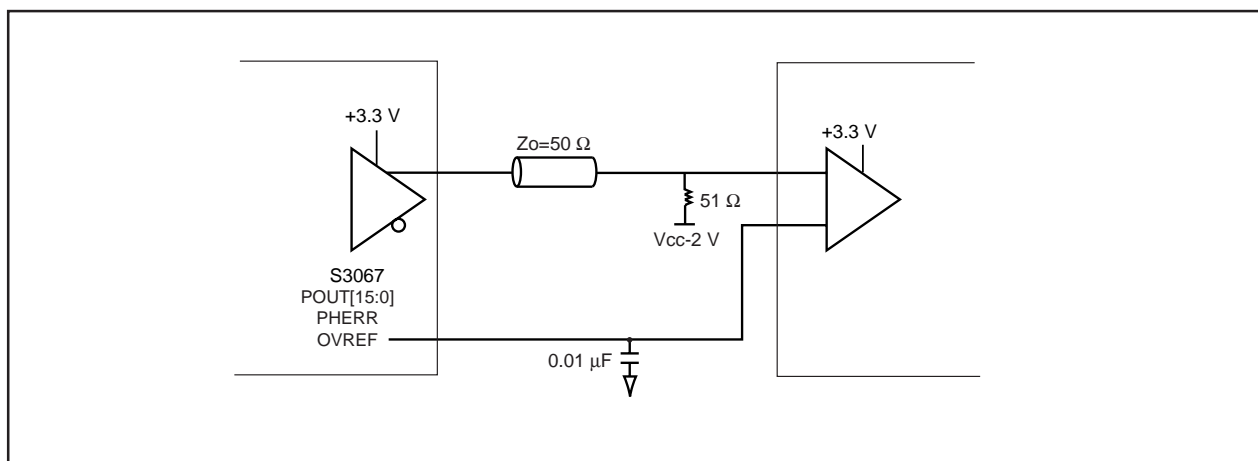


Figure 21. S3067 Single-Ended LVPECL Driver to Differential LVPECL Input Termination

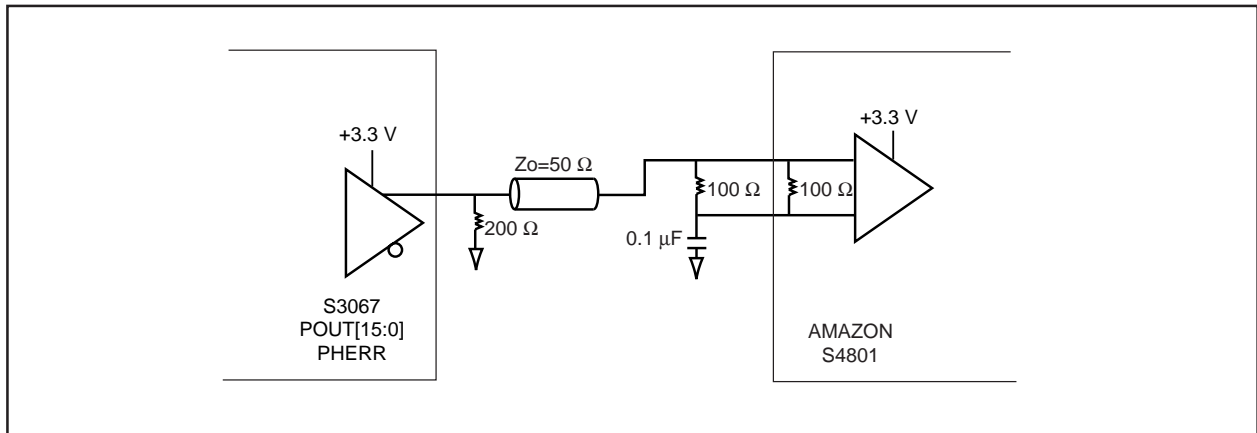


Figure 22. S3067 Differential LVPECL Driver to Differential LVPECL Input Termination

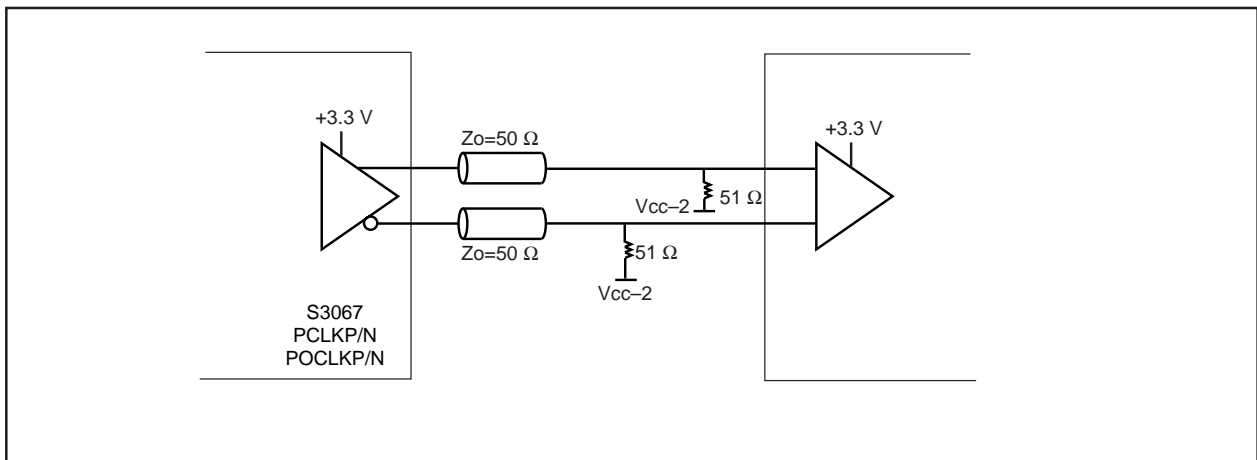


Figure 23. S3067 Differential LVPECL Driver to Differential LVPECL Input Termination

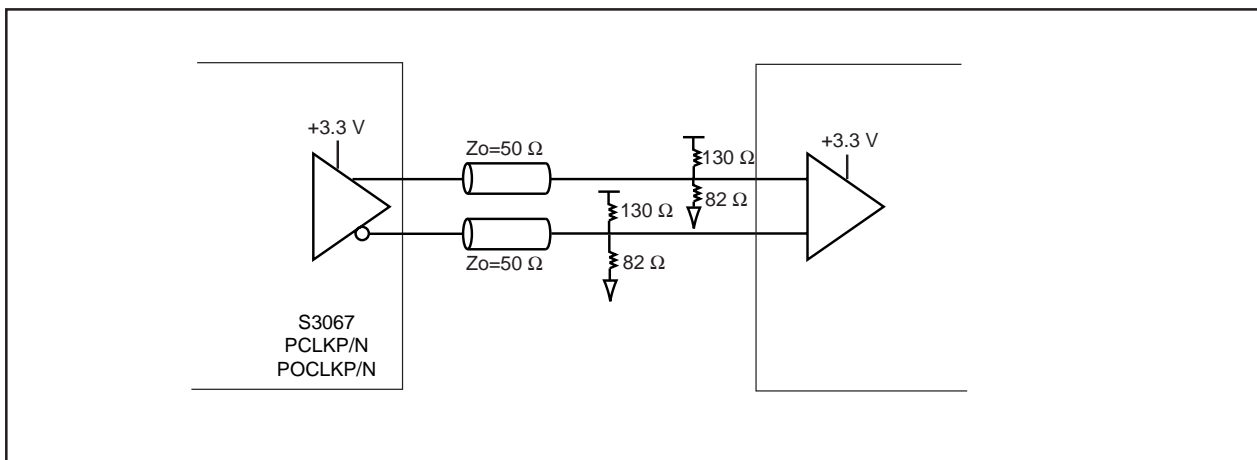
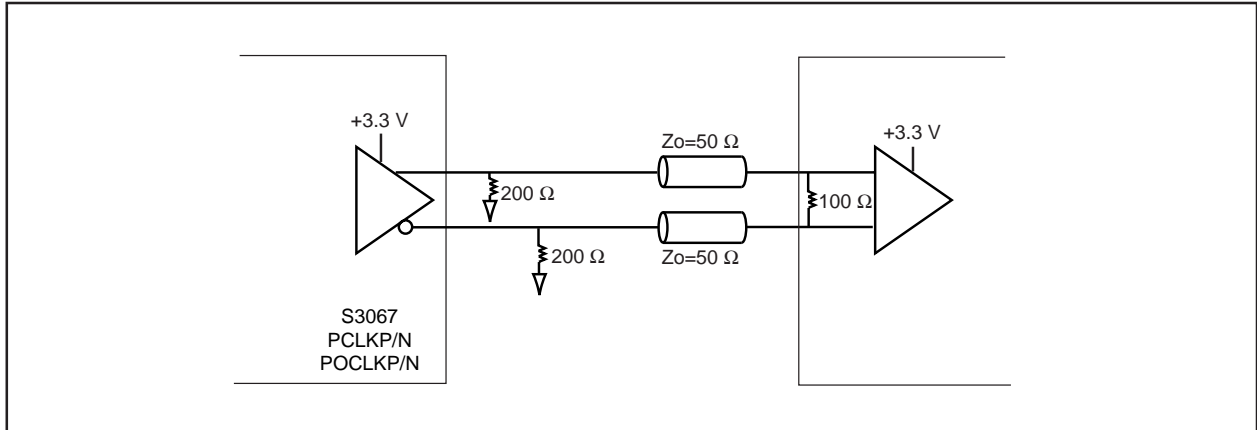


Figure 24. S3067 Differential LVPECL Driver to Differential LVPECL Input Termination¹



1. With 100 Ω line to line, V_{OL} Max increases by 100 mV .

Figure 25. Differential LVPECL Driver to S3067 Internally Biased Differential LVPECL Inputs

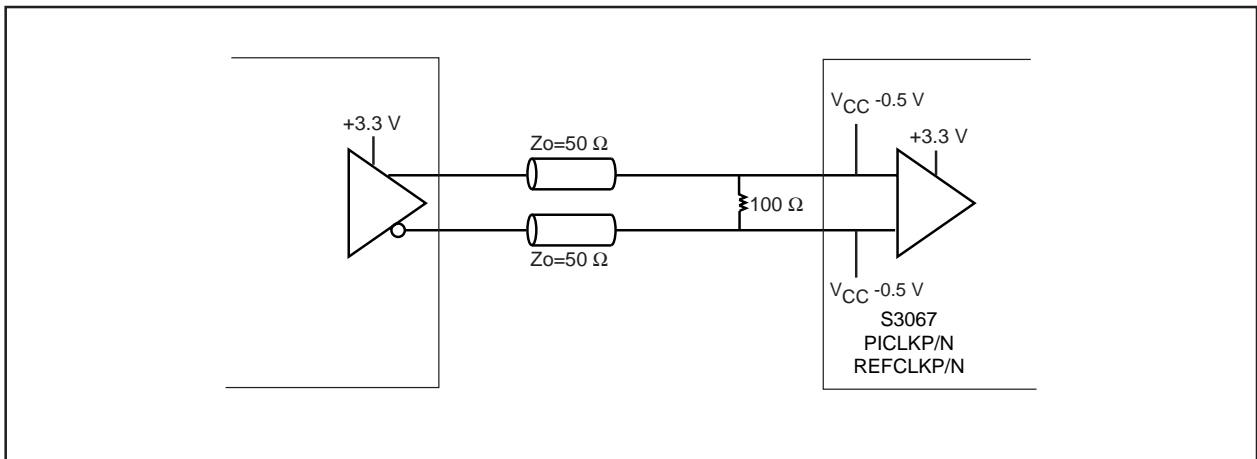
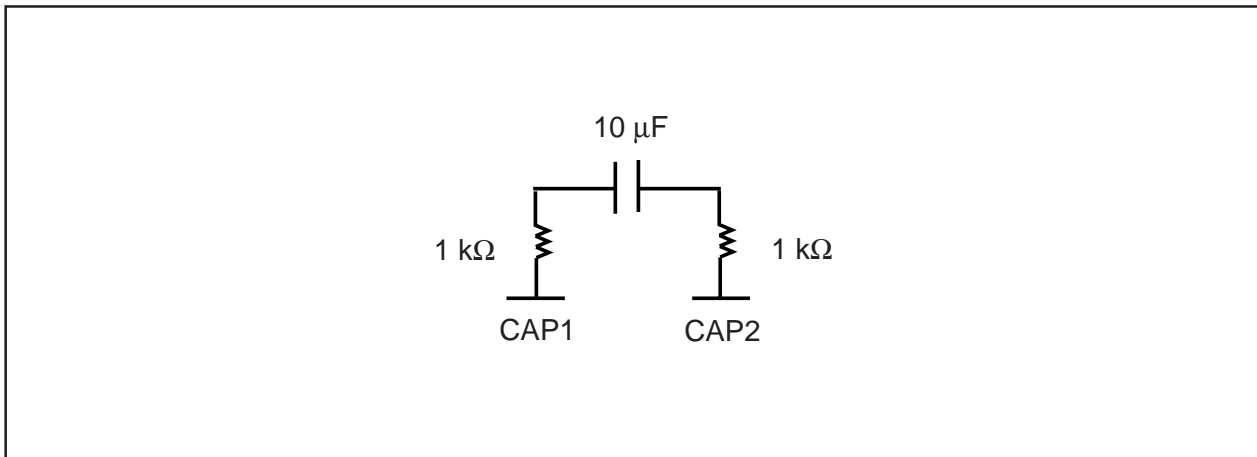


Figure 26. External Loop Filter Components



Ordering Information

| PREFIX | DEVICE | PACKAGE | Revision |
|------------------------|--------|---------------|----------|
| S – Integrated Circuit | 3067 | TB – 156 TBGA | 20 |

X XXXX XX XX
 Prefix Part No. Package Revision (S3067TB20)



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