



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

LV5762LF — Bi-CMOS IC Step-down Switching Regulator

Overview

LV5762LF is a 1ch step-down voltage switching regulator.

Functions

- 1ch step-down switching regulator controller
- Frequency fold back function
- Built-in pulse-by-pulse OCP circuit. It is detected by using ON resistance of an external MOS.
- Load-independent soft start circuit
- ON/OFF function

Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|--------------|------------|------------|------------------|
| Supply voltage | V_{IN} max | | 45 | V |
| Allowable power dissipation | P_d max | *) | 0.65 | W |
| Operating temperature | T_{opr} | | -40 to 85 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to 150 | $^\circ\text{C}$ |

* Specified board: 24.0mm × 15.0mm × 1.6mm, glass epoxy board (2-layer).

Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-------------------------------|----------|------------|----------|------|
| Supply voltage range 1 | V_{IN} | | 8 to 42 | V |
| Error amplifier input voltage | V_{FB} | | 0 to 1.6 | V |

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|----------------------------|-----------|-------------------------|---------|-------|-------|------|
| | | | min | typ | max | |
| Reference voltage block | | | | | | |
| Internal reference voltage | V_{ref} | Including offset of E/A | 0.695 | 0.705 | 0.715 | V |
| 5V power supply | V_{DD} | $I_{OUT}=0$ to 5mA | 4.7 | 5.2 | 5.7 | V |

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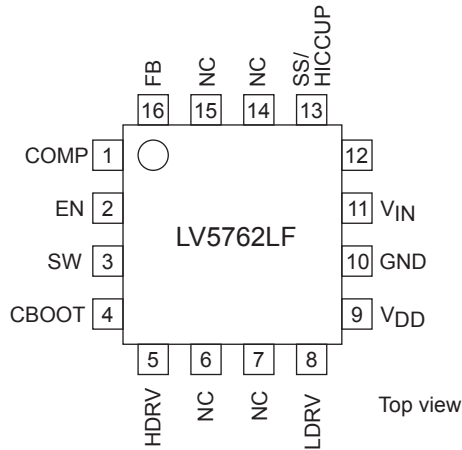
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| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-----------------------------------------------------------|----------------|---------------------------------------|---------------|------|----------|-----------|
| | | | min | typ | max | |
| Triangular waveform oscillator block | | | | | | |
| Oscillation frequency | f_{OSC} | | 870 | 1000 | 1130 | kHz |
| Frequency variation | f_{OSC_DV} | $V_{IN}=8$ to 42V | | 1 | | % |
| Oscillatory frequency fold back detection voltage | V_{OSC_FB} | Detect IN voltage after the end of SS | | 0.5 | | V |
| Oscillatory frequency after fold back | f_{OSC_FB} | | 100 | 150 | 200 | kHz |
| ON/OFF circuit block | | | | | | |
| IC start-up voltage | V_{EN_on} | $V_{IN}=8$ to 42V | | 3.4 | 4.3 | V |
| IC off voltage | V_{EN_off} | $V_{IN}=8$ to 42V | 1.1 | 1.3 | | V |
| Soft start circuit block | | | | | | |
| Soft start source current | I_{SS_SC} | $EN > 5V, SS=0V$ | 3.4 | 4.3 | 5.2 | μA |
| Soft start sink current | I_{SS_SK} | $EN > 1V, V_{DD}=5V, SS=1V$ | | 2 | | mA |
| Voltage to end the soft start function | V_{SS_END} | | 0.7 | 0.9 | 1.1 | V |
| UVLO circuit block | | | | | | |
| UVLO lock release voltage | V_{UVLO} | | 7.0 | 7.4 | 7.8 | V |
| UVLO hysteresis | V_{UVLO_H} | | | 0.6 | | V |
| Error amplifier | | | | | | |
| Input bias current | I_{EA_IN} | | | | 100 | μA |
| Error amplifier transconductance | GEA | | 1000 | 1400 | 1800 | $\mu A/V$ |
| Common mode input voltage range | V_{EA_R} | $V_{IN}=8$ to 42V | 0.0 | | 1.6 | V |
| Sink output current | I_{EA_OSK} | FB=1.0V | | -100 | | μA |
| Source output current | I_{EA_OSC} | FB=0V | | 100 | | μA |
| Current detection amplifier gain | GISNS | | | 1.3 | | |
| Over current limiter circuit block | | | | | | |
| Reference current | I_{LIM} | | -10% | 20 | +10% | μA |
| Over current detection comparator offset voltage | V_{LIM_OFS} | | -5 | | +5 | mV |
| Over current detection comparator common mode input range | | | $V_{IN}-0.45$ | | V_{IN} | V |
| PWM comparator | | | | | | |
| Input threshold voltage | V_{tmax} | Duty cycle=DMAX | 0.95 | 1.1 | 1.25 | V |
| | V_{t0} | Duty cycle=0% | 0.35 | 0.45 | 0.55 | V |
| Maximum ON duty | DMAX | | 75 | 80 | | % |
| Output block | | | | | | |
| Output stage ON resistance(the upper side) | R_{ONH} | | | 5 | | Ω |
| Output stage ON resistance(the under side) | R_{ONL} | | | 5 | | Ω |
| Output stage ON current(the upper side) | I_{ONH} | | 240 | | | mA |
| Output stage ON current(the under side) | I_{ONL} | | 240 | | | mA |
| The whole device | | | | | | |
| Standby current | I_{CCS} | $EN < 1V$ | | | 60 | μA |
| Mean consumption current | I_{CCA} | $EN > 5V$ | | 3.6 | | mA |

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Pin Assignment



Pin Function

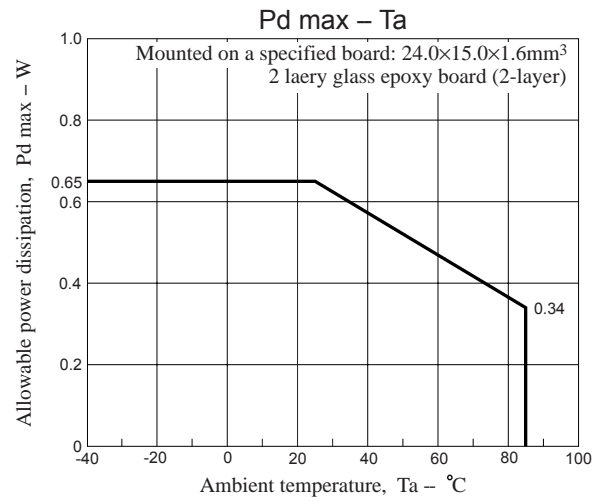
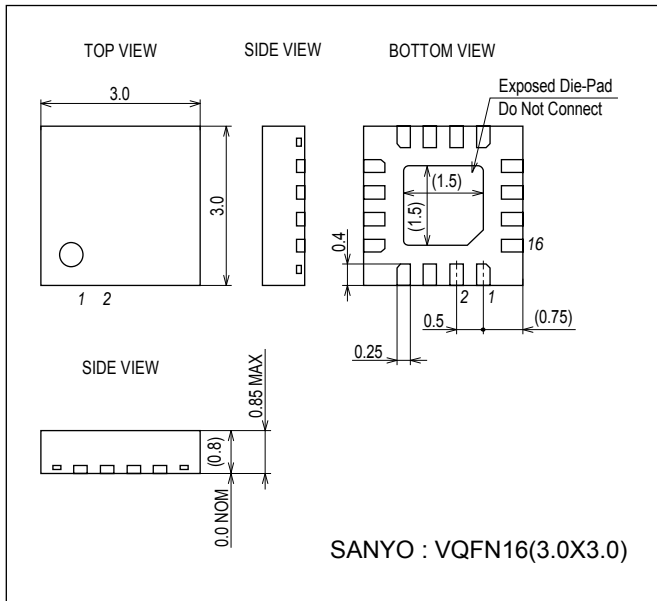
| Pin No. | Pin name | Function |
|----------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | COMP | Error amplifier output pin. Connect a phase compensation circuit between this pin and GND. |
| 2 | EN | ON/OFF pin. |
| 3 | SW | Pin to connect with switching node. The source of Nch MOSFET connects to this pin. |
| 4 | CBOOT | Bootstrap capacity connection pin. This pin becomes a GATE drive power supply of an external Nch MOSFET. Connect a bypass capacitor between CBOOT and SW. |
| 5 | HDRVV | An external the upper MOSFET gate drive pin. |
| 6, 7 14, 15 | NC | No connection |
| 8 | LDRV | An external the lower MOSFET gate drive pin. |
| 9 | V _{DD} | Power supply pin for an external the MOS-FET gate drive. |
| 10 | GND | Ground pin. Each reference voltage is based on the voltage of the ground pin. |
| 11 | V _{IN} | Power supply pin. This pin is monitored by UVLO function. When the voltage of this pin becomes 7.8V or more by UVLO function, The IC starts and the soft start function operates. |
| 12 | I _{LIM} | Reference current pin for current detection. The sink current of about 20μA flows to this pin. When a resistance is connected between this pin and V _{IN} outside and the voltage applied to the SW pin is lower than the voltage of the terminal side of the resistance, the upper Nch MOSFET is off by operating the current limiter comparator. This operation is reset with respect to each PWN pulse. |
| 13 | SS/HICCUP | Pin to connect a capacitor for soft start. A capacitor for soft start is charged by using the voltage of about 4.3μA. This pin ends the soft start period by using the voltage of about 0.9V and the frequency fold back function becomes active. |
| 16 | FB | Error amplifier reverse input pin. By operating the converter, the voltage of this pin becomes 0.7V. The voltage in which the output voltage is divided by an external resistance is applied to this pin. Also, the oscillation frequency become one-eighth when the voltage of this pin becomes 0.4V or less after soft start function. |

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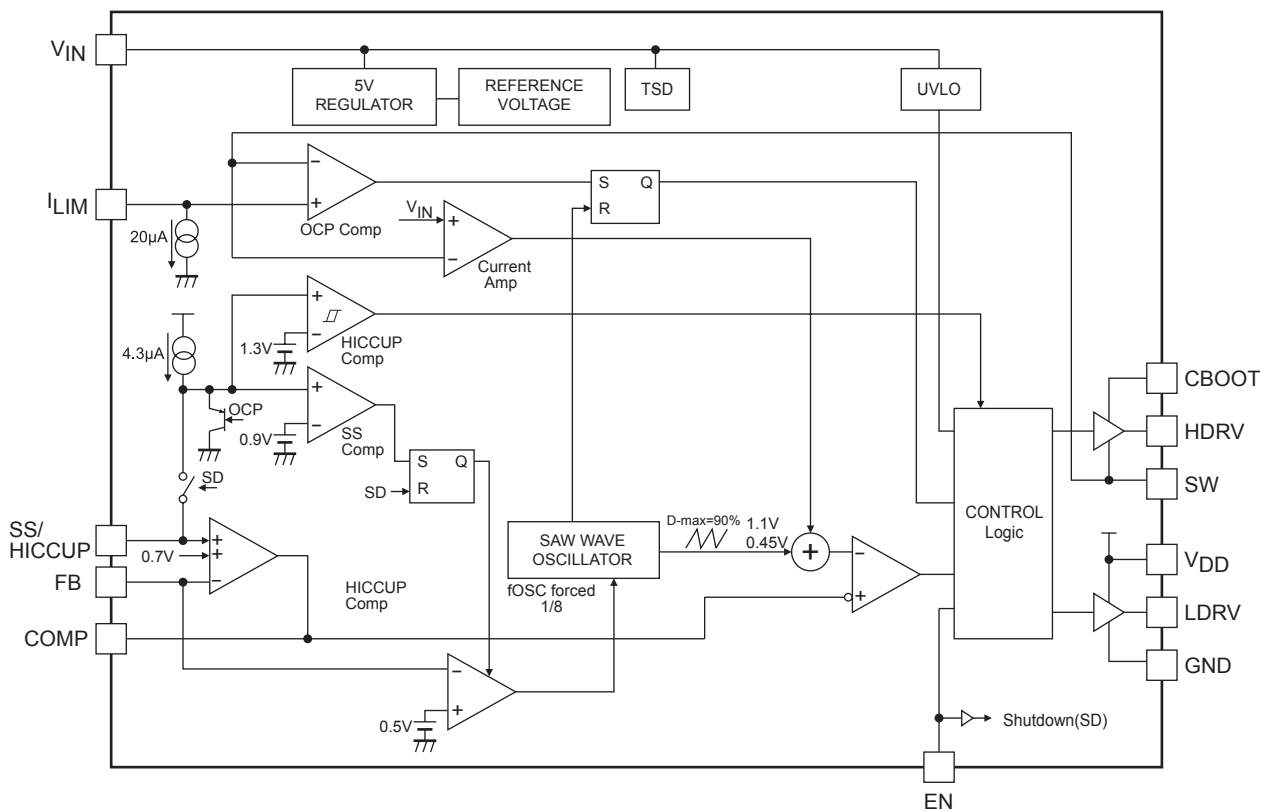
Package Dimensions

unit : mm (typ)

3394

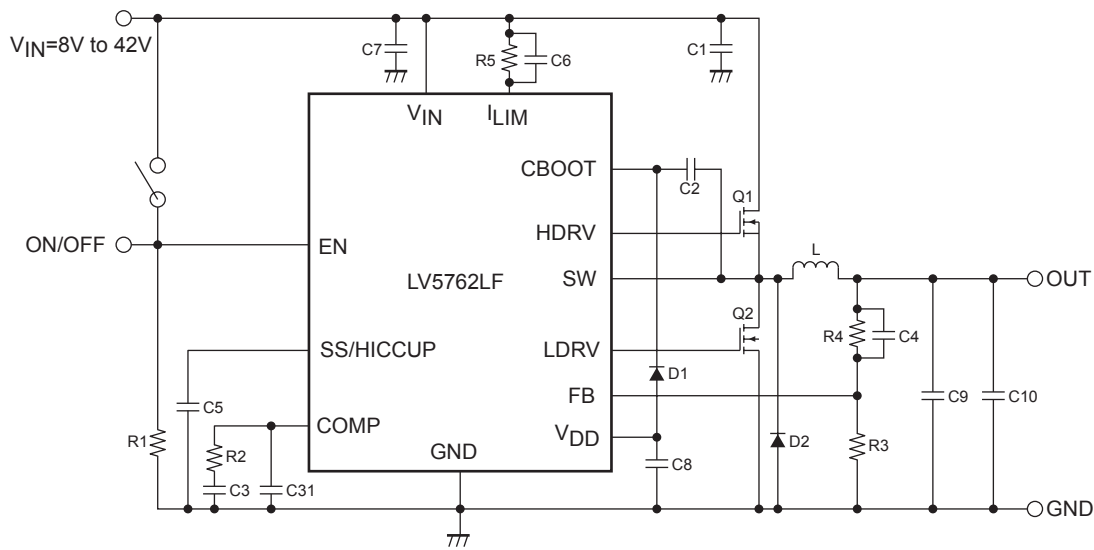


Block Diagram



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Sample Application Circuit



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