

Dual N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
30	0.0355 at V _{GS} = 10 V	6.5	3.7 nC
	0.044 at V _{GS} = 4.5 V	5.8	

FEATURES

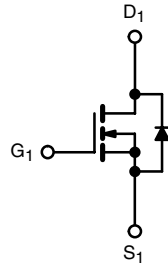
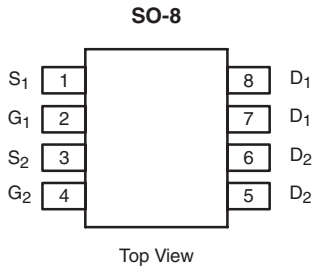
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % UIS Tested
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



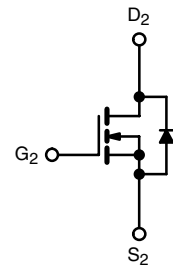
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Set Top Box
- Low Current DC/DC



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	30	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	6.5 ^a	A
		T _C = 70 °C	5.2	
		T _A = 25 °C	5.2 ^{b, c}	
		T _A = 70 °C	4.2 ^{b, c}	
Pulsed Drain Current	I _{DM}	24		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	2.25	
		T _A = 25 °C	1.48 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	5		
Single Pulse Avalanche Energy	E _{AS}	1.25	mJ	
Maximum Power Dissipation	P _D	T _C = 25 °C	2.7	W
		T _C = 70 °C	1.77	
		T _A = 25 °C	1.78 ^{b, c}	
		T _A = 70 °C	1.14 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, c, d}	R _{thJA}	58	70	°C/W	
Maximum Junction-to-Foot (Drain)	R _{thJF}	38	45		

Notes:

- Package limited, T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 110 °C/W.

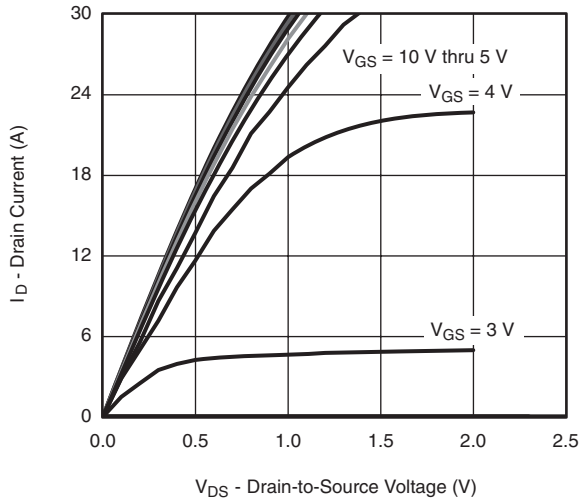
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		32		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.0		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.2		2.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	10			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		0.0295	0.0355	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 4\text{ A}$		0.036	0.044	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 5\text{ A}$		16		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		445		pF
Output Capacitance	C_{oss}			75		
Reverse Transfer Capacitance	C_{rss}			37		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		8	12	nC
				3.7	5.6	
Gate-Source Charge	Q_{gs}	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$		1.4		
Gate-Drain Charge	Q_{gd}			1.05		
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.8	4.3	8.6	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		12	24	ns
Rise Time	t_r			55	100	
Turn-Off Delay Time	$t_{d(off)}$			11	22	
Fall Time	t_f			8	16	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		4	8	
Rise Time	t_r			9	18	
Turn-Off Delay Time	$t_{d(off)}$			10	20	
Fall Time	t_f			6	12	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			2.25	A
Pulse Diode Forward Current	I_{SM}				24	
Body Diode Voltage	V_{SD}	$I_S = 2\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		11	20	ns
Body Diode Reverse Recovery Charge	Q_{rr}			4	8	nC
Reverse Recovery Fall Time	t_a			7		ns
Reverse Recovery Rise Time	t_b			4		

Notes:

- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

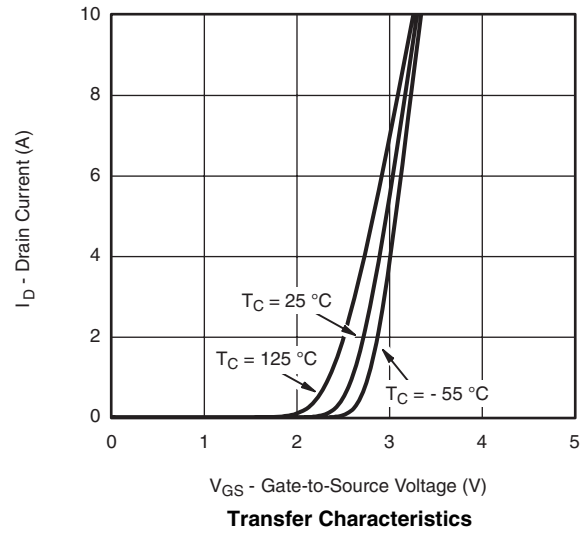


$V_{GS} = 10\text{ V thru } 5\text{ V}$
 $V_{GS} = 4\text{ V}$
 $V_{GS} = 3\text{ V}$

I_D - Drain Current (A)

V_{DS} - Drain-to-Source Voltage (V)

Output Characteristics

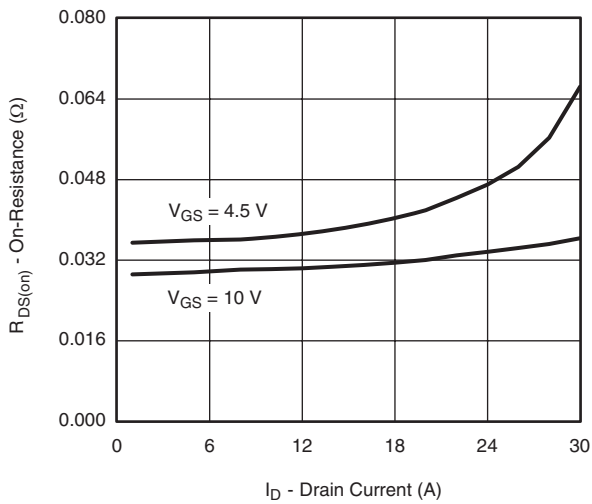


$T_C = 25\text{ }^\circ\text{C}$
 $T_C = 125\text{ }^\circ\text{C}$
 $T_C = -55\text{ }^\circ\text{C}$

I_D - Drain Current (A)

V_{GS} - Gate-to-Source Voltage (V)

Transfer Characteristics

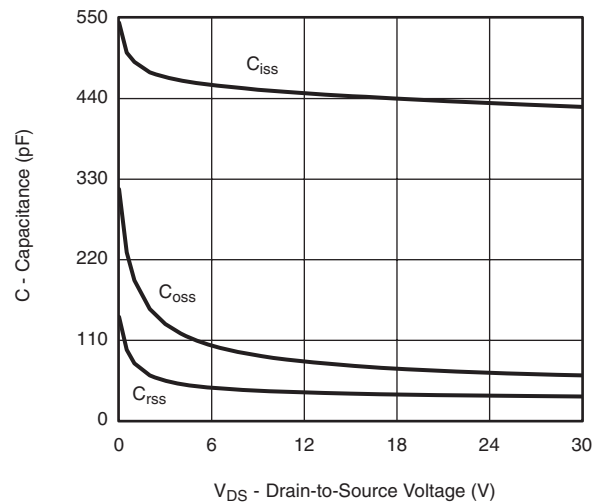


$V_{GS} = 4.5\text{ V}$
 $V_{GS} = 10\text{ V}$

$R_{DS(on)}$ - On-Resistance (Ω)

I_D - Drain Current (A)

On-Resistance vs. Drain Current

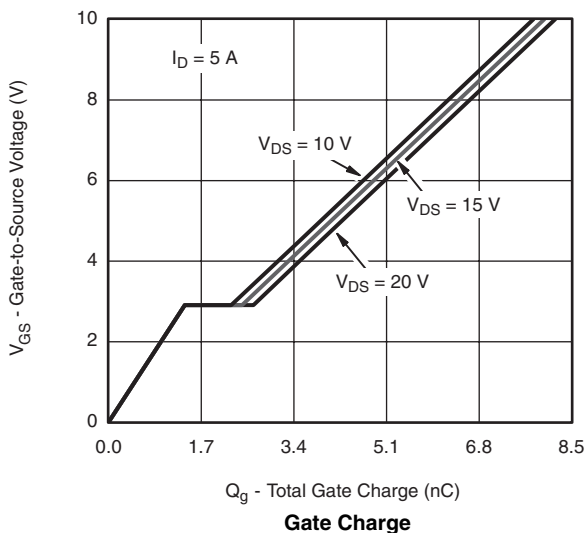


C_{iss}
 C_{oss}
 C_{rss}

C - Capacitance (pF)

V_{DS} - Drain-to-Source Voltage (V)

Capacitance

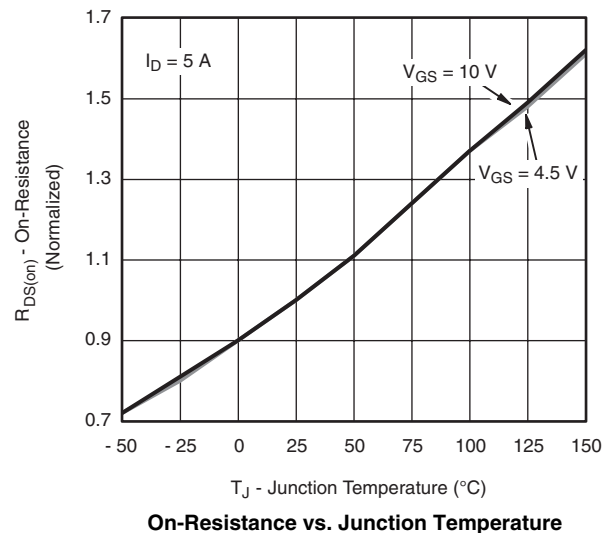


$I_D = 5\text{ A}$
 $V_{DS} = 10\text{ V}$
 $V_{DS} = 15\text{ V}$
 $V_{DS} = 20\text{ V}$

V_{GS} - Gate-to-Source Voltage (V)

Q_g - Total Gate Charge (nC)

Gate Charge



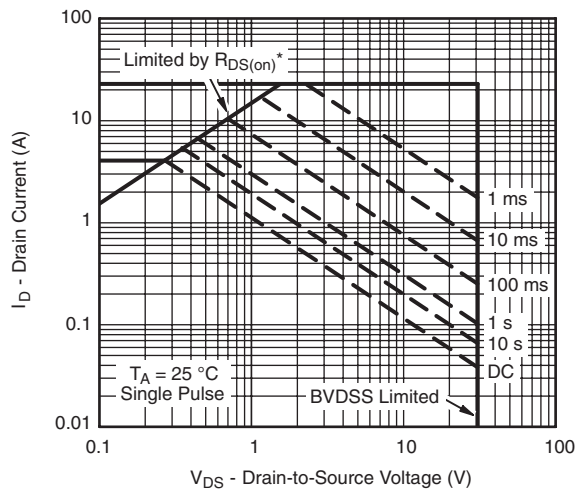
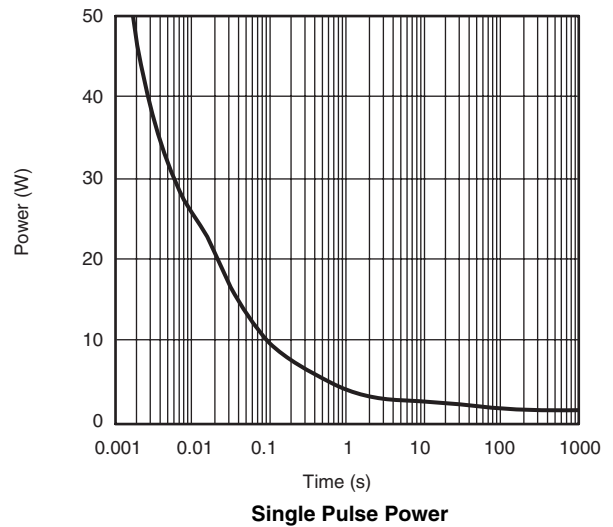
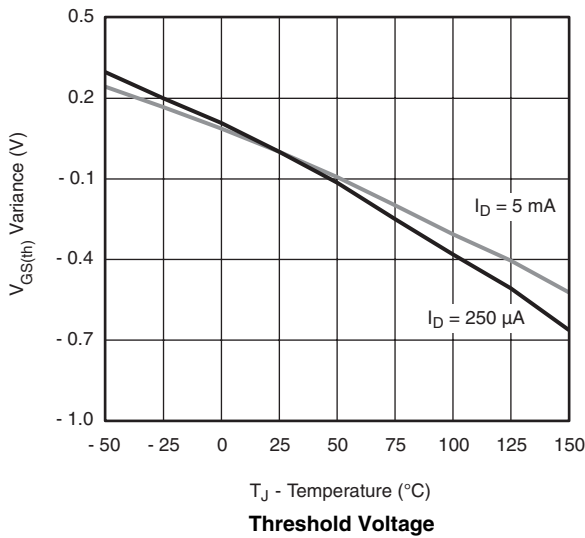
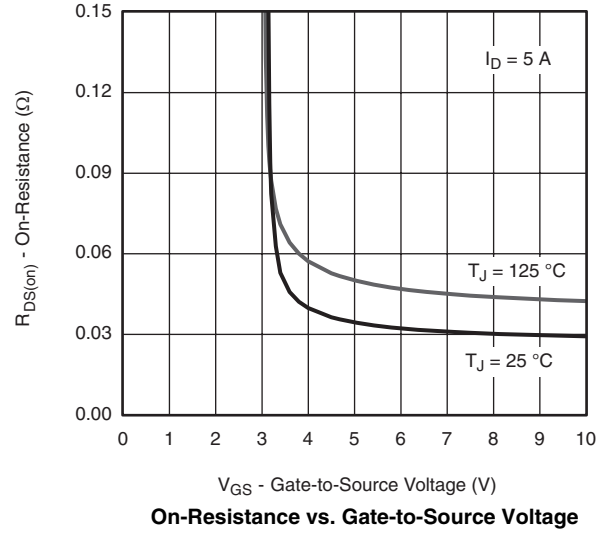
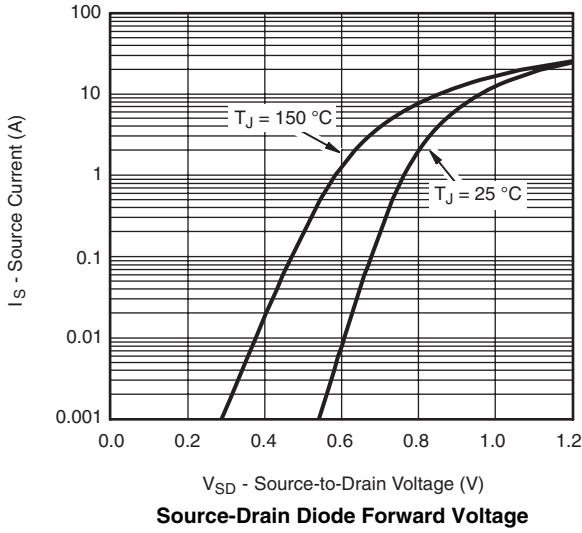
$I_D = 5\text{ A}$
 $V_{GS} = 10\text{ V}$
 $V_{GS} = 4.5\text{ V}$

$R_{DS(on)}$ - On-Resistance (Normalized)

T_J - Junction Temperature ($^\circ\text{C}$)

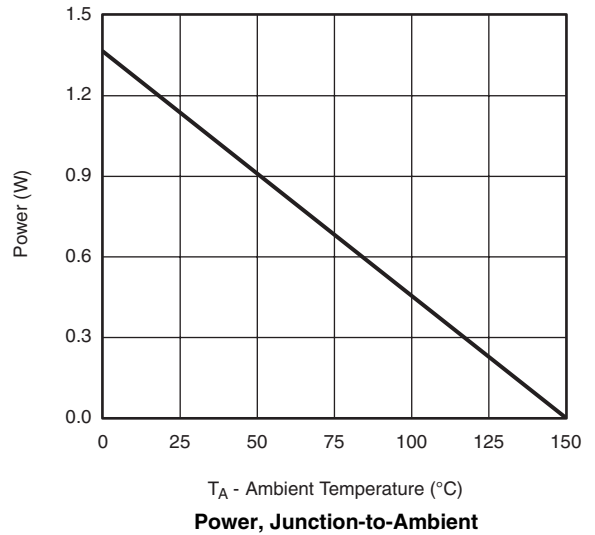
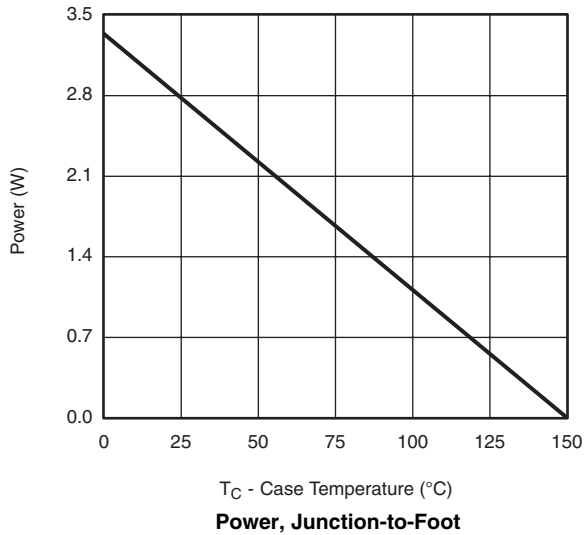
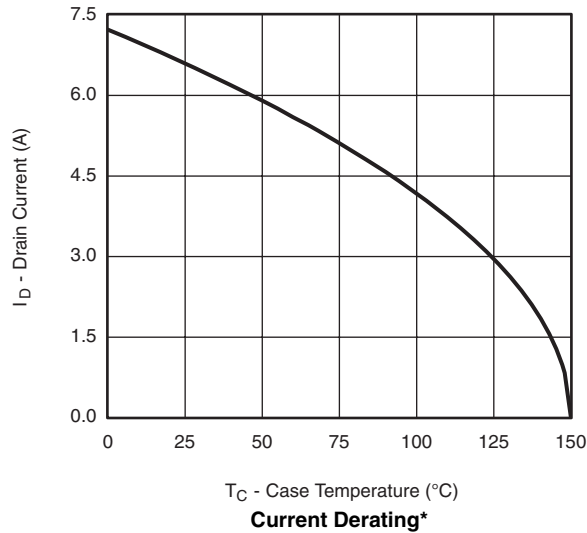
On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

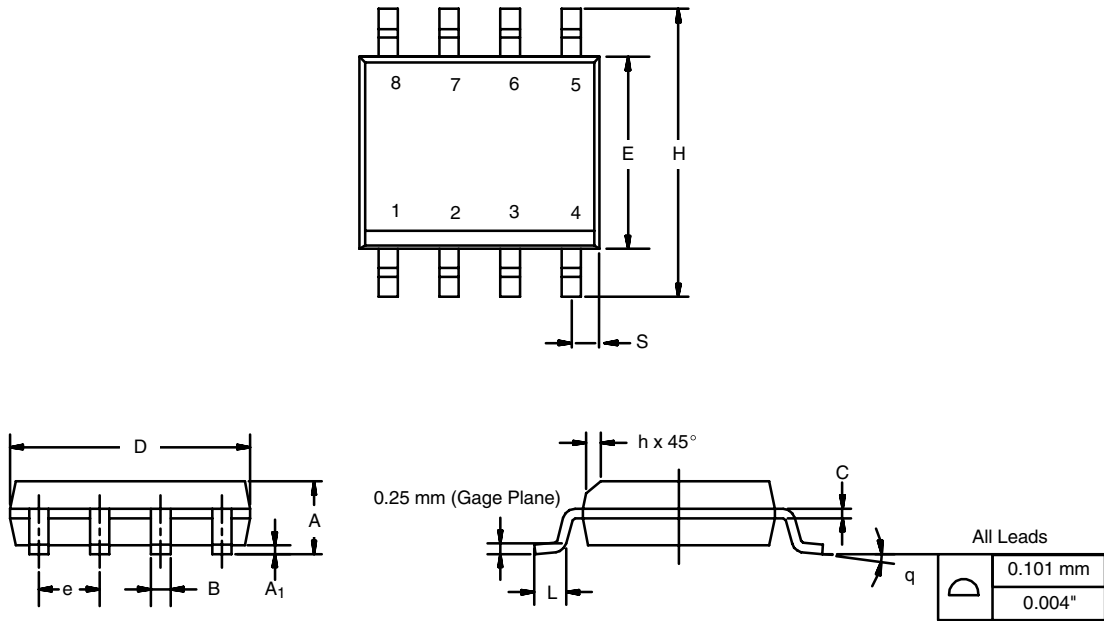
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

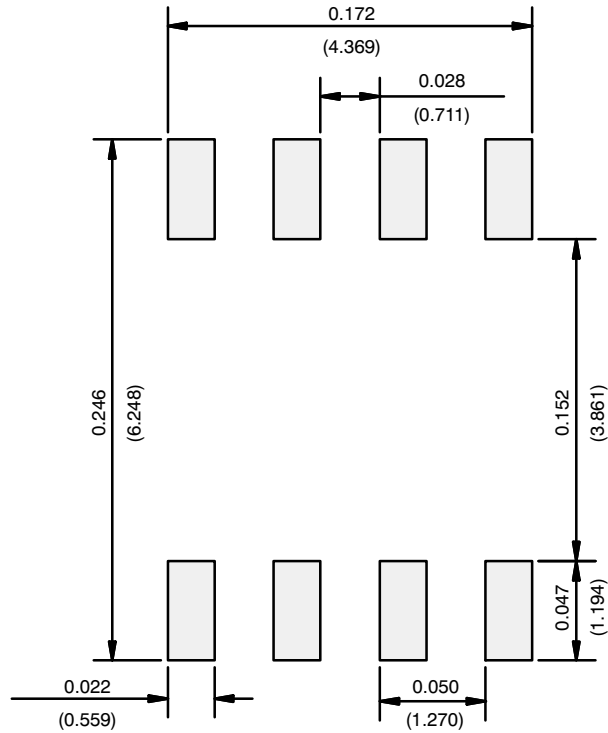
SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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