

AD8538/AD8539

FEATURES

Low offset voltage: 13 μ V maximum
Input offset drift: 0.03 μ V/ $^{\circ}$ C
Single-supply operation: 2.7 V to 5.5 V
High gain, CMRR, and PSRR
Low input bias current: 25 pA
Low supply current: 180 μ A

APPLICATIONS

Mobile communications
Portable instrumentation
Battery-powered devices
Sensor interfaces
Temperature measurement
Electronic scales

GENERAL DESCRIPTION

The AD8538/AD8539 are very high precision amplifiers featuring extremely low offset voltage, low input bias current, and low power consumption. The supply current is less than 215 μ A maximum per amplifier at 5.0 V. Operation is fully specified from 2.7 V to 5.0 V single supply (± 1.35 V to ± 2.5 V dual supply).

The AD8538/AD8539 operate at very low power making these amplifiers ideal for battery-powered devices and portable equipment.

The AD8538/AD8539 are specified over the extended industrial temperature range (-40° C to $+125^{\circ}$ C). The AD8538 amplifier is available in 5-lead TSOT-23, and 8-lead, narrow body SOIC packages, and the AD8539 amplifier is available in 8-lead, narrow body SOIC and 8-lead MSOP.

PIN CONFIGURATIONS

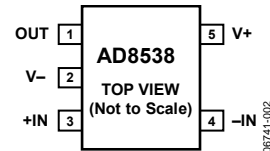


Figure 1. 5-Lead TSOT-23 (UJ-5)



Figure 2. 8-Lead SOIC_N (R-8)

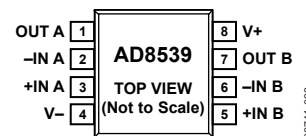


Figure 3. 8-Lead SOIC_N (R-8)



Figure 4. 8-Lead MSOP (RM-8)

Rev. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

TABLE OF CONTENTS

Features	1	Absolute Maximum Ratings	7
Applications	1	Thermal Resistance	7
General Description	1	ESD Caution	7
Pin Configurations	1	Typical Performance Characteristics	8
Revision History	2	AD8538 Characteristics	8
Specifications	3	AD8539 Characteristics	14
AD8538 Electrical Specifications	3	Outline Dimensions	20
AD8539 Electrical Specifications	5	Ordering Guide	21

REVISION HISTORY

5/07—Rev. 0 to Rev. A

Added AD8539	Universal
Changes to Specifications Section	3
Added Table 3, Renumbered Tables Sequentially	5
Added Table 4, Renumbered Tables Sequentially	6
Changes to Thermal Resistance Section	7
Added Figure 32 and Figure 33	13
Added AD8539 Characteristics Section, Renumbered Figures Sequentially	14

Updated Outline Dimensions	20
Changes to Ordering Guide	21

10/05—Revision 0: Initial Version

SPECIFICATIONS

AD8538 ELECTRICAL SPECIFICATIONS

@ $V_S = 5.0\text{ V}$, $V_{CM} = 2.5\text{ V}$, $V_O = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	13	μV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			30	μV
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		15	25	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.7	1.0	nA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	50	pA
Input Voltage Range					150	pA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $V_{CM} = 0.2\text{ V to } 4.8\text{ V}$	0	115	150	V dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $V_O = 0.1\text{ V to } 4.9\text{ V}$	100	115	135	dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110	135		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.03	0.1	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 100\text{ k}\Omega$ to ground	4.99	4.998		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 100\text{ k}\Omega$ to ground	4.98			V
		$R_L = 10\text{ k}\Omega$ to ground	4.95	4.970		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to ground	4.94			V
Output Voltage Low	V_{OL}	$R_L = 100\text{ k}\Omega$ to $V+$		1.9	5	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 100\text{ k}\Omega$ to $V+$		2.8	7	mV
		$R_L = 10\text{ k}\Omega$ to $V+$		17	20	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to $V+$		20	30	mV
Short-Circuit Limit	I_{SC}			± 25		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to } 5.0\text{ V}$	105	125		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100	125		dB
Supply Current/Amplifier	I_{SY}	$I_O = 0$		150	180	μA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		190	215	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.4		$\text{V}/\mu\text{s}$
Settling Time 0.01%	t_s	$G = \pm 1$, 2 V step , $C_L = 20\text{ pF}$, $R_L = 1\text{ k}\Omega$		10		μs
Overload Recovery Time				0.05		ms
Gain Bandwidth Product	GBP			430		kHz
Phase Margin	ϕ_M	$R_L = 10\text{ k}\Omega$, $R_L = 100\text{ k}\Omega$, $C_L = 20\text{ pF}$		65		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\text{ p-p}}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		2.0		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		50		$\text{nV}/\sqrt{\text{Hz}}$

AD8538/AD8539

@ $V_S = 2.7\text{ V}$, $V_{CM} = 1.35\text{ V}$, $V_O = 1.35\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	13	μV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		15	25	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.7	1.0	nA
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	50	pA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 2.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	0	110	140	dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $V_O = 0.1\text{ V to } 1.7\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100	110	140	dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		105	135	dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 100\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 100\text{ k}\Omega$ to ground	2.68	2.698		V
		$R_L = 10\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to ground	2.68			V
		$R_L = 10\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to ground	2.67	2.68		V
Output Voltage Low	V_{OL}	$R_L = 100\text{ k}\Omega$ to $V+$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 100\text{ k}\Omega$ to $V+$		1.7	5	mV
		$R_L = 10\text{ k}\Omega$ to $V+$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to $V+$		2.4	5	mV
		$R_L = 10\text{ k}\Omega$ to $V+$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to $V+$		14	20	mV
Short-Circuit Limit	I_{SC}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to $V+$		20	25	mV
				± 8		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to } 5.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	105	125		dB
Supply Current/Amplifier	I_{SY}	$I_O = 0$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		100	125	dB
				150	180	μA
				190	215	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.35		$\text{V}/\mu\text{s}$
Settling Time 0.01%	t_S	$G = \pm 1$, 1 V step , $C_L = 20\text{ pF}$, $R_L = 1\text{ k}\Omega$		5		μs
Overload Recovery Time				0.05		ms
Gain Bandwidth Product	GBP			430		kHz
Phase Margin	ϕ_M	$R_L = 10\text{ k}\Omega$, $R_L = 100\text{ k}\Omega$, $C_L = 20\text{ pF}$		65		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\text{ p-p}}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		2.0		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		50		$\text{nV}/\sqrt{\text{Hz}}$

AD8539 ELECTRICAL SPECIFICATIONS

@ $V_S = 5.0\text{ V}$, $V_{CM} = 2.5\text{ V}$, $V_O = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	15	μV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			30	μV
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		15	60	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.7	1.0	nA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	70	pA
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	0		5	V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	0.2		4.8	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 5\text{ V}$	115	135		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $V_{CM} = 0.2\text{ V to } 4.8\text{ V}$	100	130		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $V_O = 0.1\text{ V to } 4.9\text{ V}$	110	130		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110	125		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.03	0.1	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 100\text{ k}\Omega$ to ground	4.99	4.994		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 100\text{ k}\Omega$ to ground	4.98			V
		$R_L = 10\text{ k}\Omega$ to ground	4.95	4.97		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to ground	4.94			V
Output Voltage Low	V_{OL}	$R_L = 100\text{ k}\Omega$ to V_+		5	7	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 100\text{ k}\Omega$ to V_+		6	8	mV
		$R_L = 10\text{ k}\Omega$ to V_+		20	25	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to V_+		24	30	mV
Short-Circuit Limit	I_{SC}			± 25		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to } 5.0\text{ V}$	105	125		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100	125		dB
Supply Current/Amplifier	I_{SY}	$I_O = 0$		170	210	μA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			225	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.4		$\text{V}/\mu\text{s}$
Settling Time 0.01%	t_s	$G = \pm 1$, 2 V step , $C_L = 20\text{ pF}$, $R_L = 1\text{ k}\Omega$		10		μs
Overload Recovery Time				0.05		ms
Gain Bandwidth Product	GBP			430		kHz
Phase Margin	ϕ_M	$R_L = 10\text{ k}\Omega$, $R_L = 100\text{ k}\Omega$, $C_L = 20\text{ pF}$		65		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\text{ p-p}}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		1.2		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		52		$\text{nV}/\sqrt{\text{Hz}}$

AD8538/AD8539

@ $V_S = 2.7\text{ V}$, $V_{CM} = 1.35\text{ V}$, $V_O = 1.35\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 4.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5	16	μV
Input Bias Current	I_B	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		15	25	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.7	1.0	nA
Input Voltage Range		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	0		2.7	V
Common-Mode Rejection Ratio	CMRR	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $V_{CM} = 0\text{ V to } 2.7\text{ V}$	110	130	2.5	dB
Large Signal Voltage Gain	A_{VO}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $V_{CM} = 0.2\text{ V to } 2.5\text{ V}$ $R_L = 10\text{ k}\Omega$, $V_O = 0.1\text{ V to } 2.6\text{ V}$	100	125		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	105	125		dB
				0.03	0.1	$\mu\text{V}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 100\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 100\text{ k}\Omega$ to ground	2.68	2.693		V
		$R_L = 10\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to ground	2.68			V
		$R_L = 10\text{ k}\Omega$ to ground $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to ground	2.67	2.68		V
Output Voltage Low	V_{OL}	$R_L = 100\text{ k}\Omega$ to $V+$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 100\text{ k}\Omega$ to $V+$	2.66			V
		$R_L = 10\text{ k}\Omega$ to $V+$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to $V+$		5	7	mV
		$R_L = 10\text{ k}\Omega$ to $V+$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to $V+$		6	8	mV
		$R_L = 10\text{ k}\Omega$ to $V+$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to $V+$		14	20	mV
Short-Circuit Limit	I_{SC}	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ to $V+$		20	25	mV
				± 8		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to } 5.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	105	125		dB
Supply Current/Amplifier	I_{SY}	$I_O = 0$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	100	125		dB
					210	μA
					225	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.35		$\text{V}/\mu\text{s}$
Settling Time 0.01%	t_s	$G = \pm 1$, 1 V step , $C_L = 20\text{ pF}$, $R_L = \infty$		8		μs
Overload Recovery Time				0.05		ms
Gain Bandwidth Product	GBP			430		kHz
Phase Margin	ϕ_M	$R_L = 10\text{ k}\Omega$, $R_L = 100\text{ k}\Omega$, $C_L = 20\text{ pF}$		65		Degrees
NOISE PERFORMANCE						
Voltage Noise	$e_{n\text{ p-p}}$	$f = 0.1\text{ Hz to } 10\text{ Hz}$		2.0		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		55		$\text{nV}/\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 5.

Parameter	Rating
Supply Voltage	+6 V
Input Voltage	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$
Differential Input Voltage	$\pm 6\text{ V}$
Output Short-Circuit Duration to GND	Observe derating curve
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C
Operating Temperature Range	-40°C to $+125^\circ\text{C}$
Junction Temperature Range	-65°C to $+150^\circ\text{C}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply at 25°C , unless otherwise noted.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead TSOT-23 (UJ-5)	207	61	$^\circ\text{C}/\text{W}$
8-Lead SOIC_N (R-8)	125	43	$^\circ\text{C}/\text{W}$
8-Lead MSOP (RM-8)	145	45	$^\circ\text{C}/\text{W}$

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

AD8538 CHARACTERISTICS

AD8538 only, $V_{SY} = 5\text{ V}$ or $\pm 2.5\text{ V}$, unless otherwise noted.

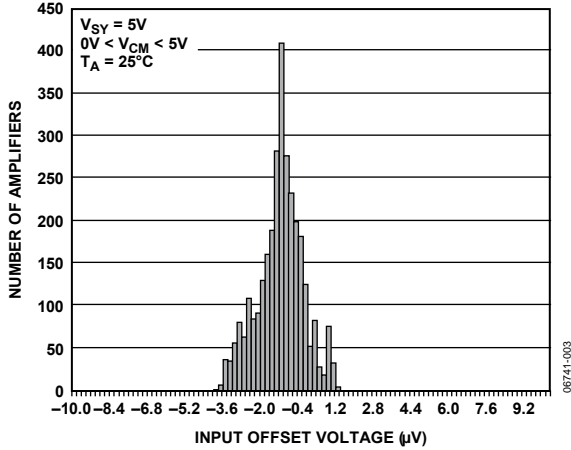


Figure 5. AD8538 Input Offset Voltage Distribution

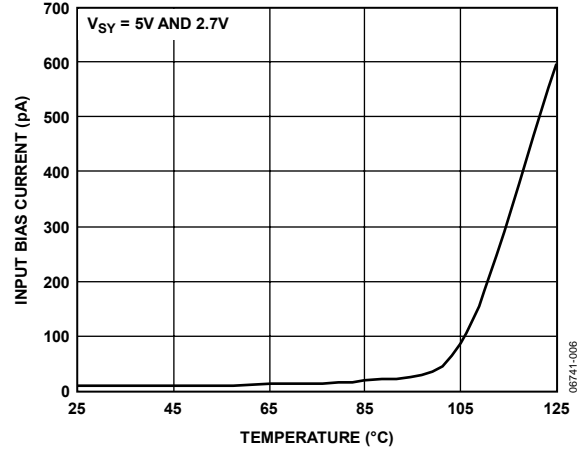


Figure 8. AD8538 Input Bias Current vs. Temperature

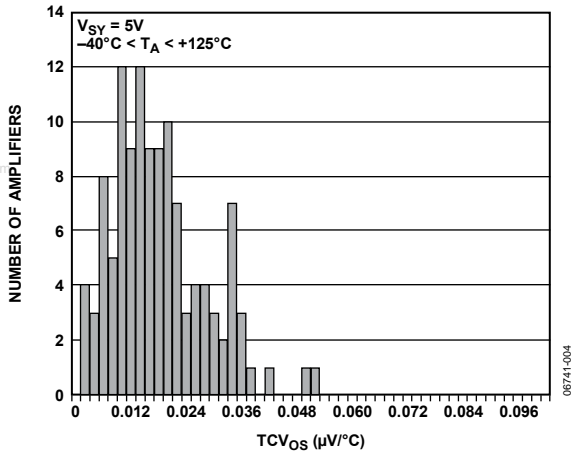


Figure 6. AD8538 Input Offset Voltage Drift Distribution

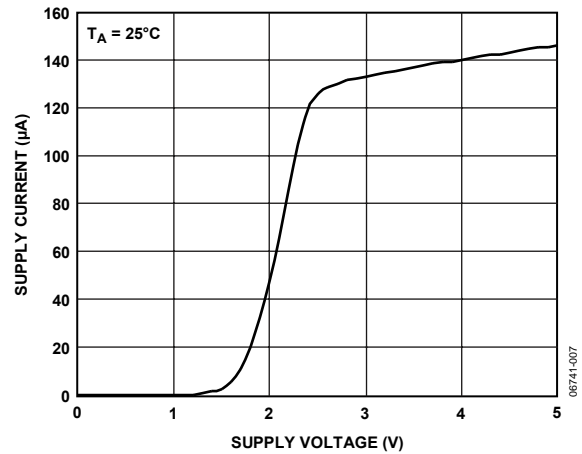


Figure 9. AD8538 Supply Current vs. Supply Voltage

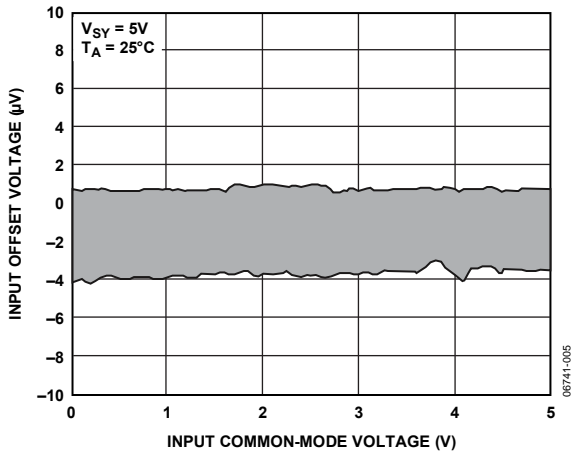


Figure 7. AD8538 Input Offset Voltage vs. Input Common-Mode Voltage

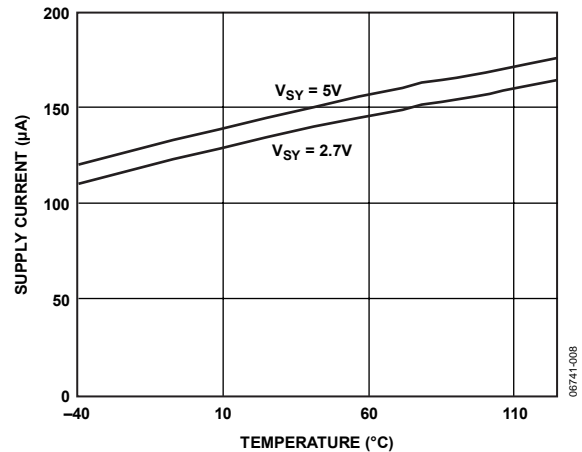


Figure 10. AD8538 Supply Current vs. Temperature

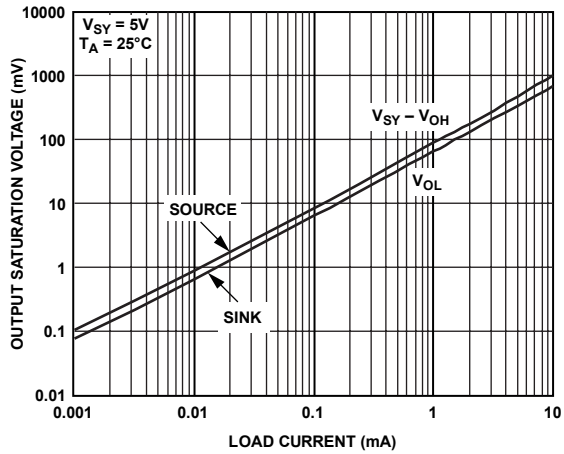


Figure 11. AD8538 Output Saturation Voltage vs. Load Current

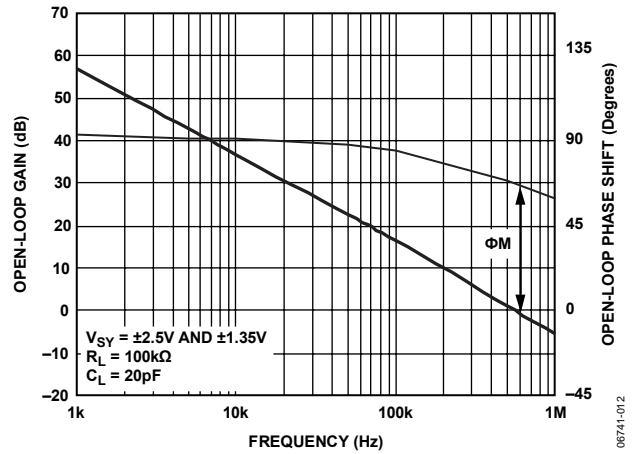


Figure 14. AD8538 Open-Loop Gain and Phase vs. Frequency

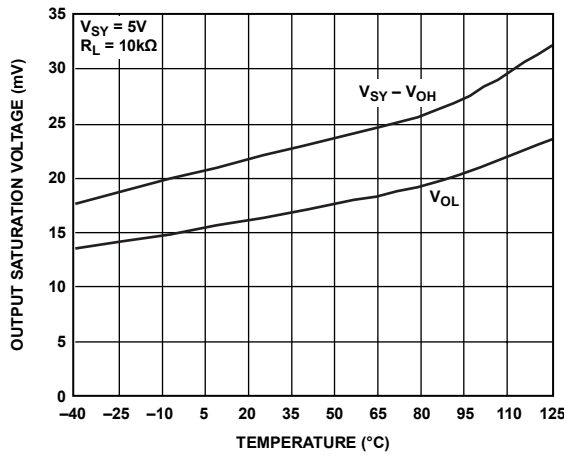


Figure 12. AD8538 Output Saturation Voltage vs. Temperature

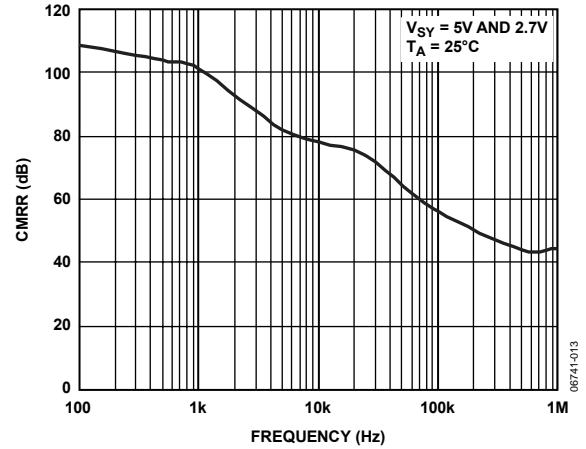


Figure 15. AD8538 CMRR vs. Frequency

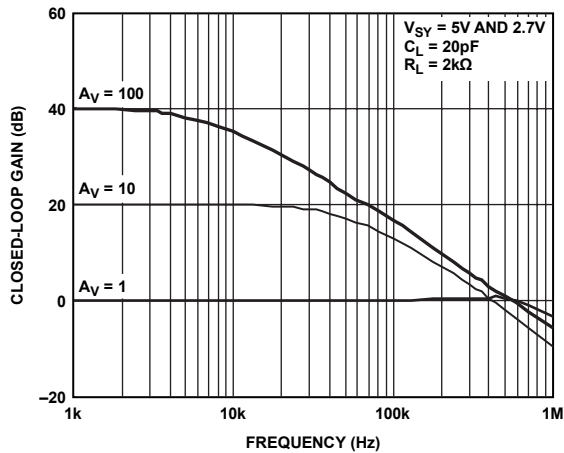


Figure 13. AD8538 Closed-Loop Gain vs. Frequency

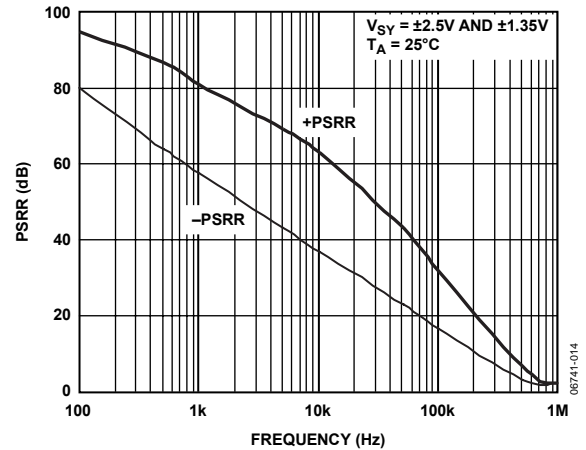


Figure 16. AD8538 PSRR vs. Frequency

AD8538/AD8539

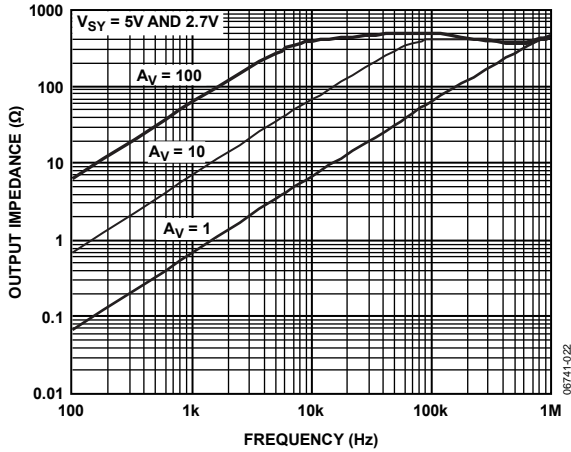


Figure 17. AD8538 Closed-Loop Output Impedance vs. Frequency

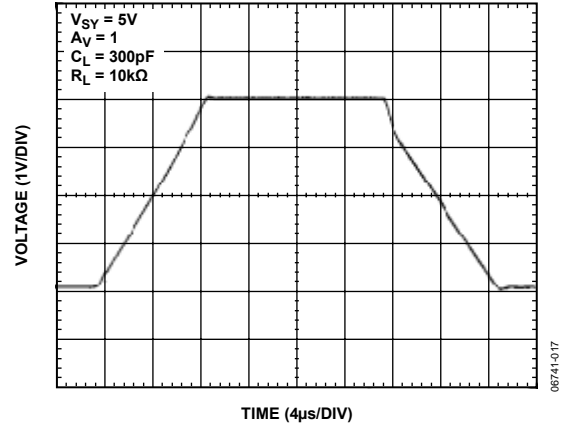


Figure 20. AD8538 Large Signal Transient Response

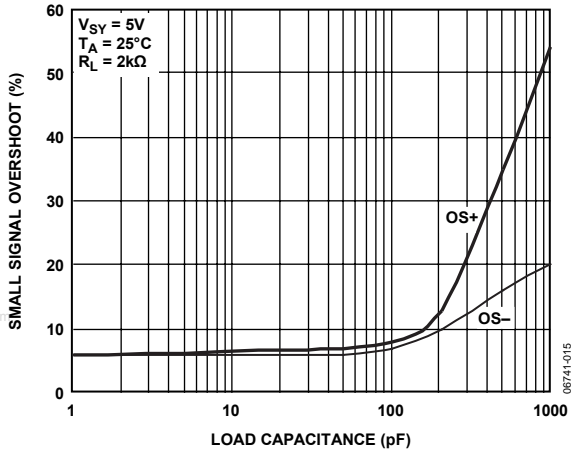


Figure 18. AD8538 Small Signal Overshoot vs. Load Capacitance

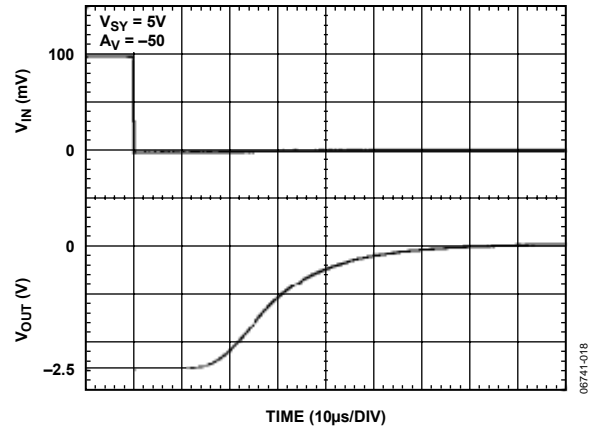


Figure 21. AD8538 Positive Overload Recovery

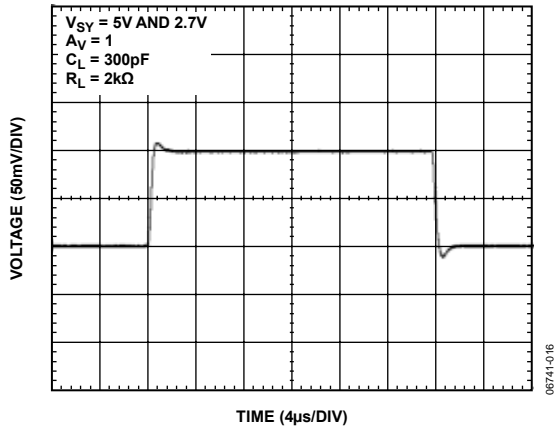


Figure 19. AD8538 Small Signal Transient Response

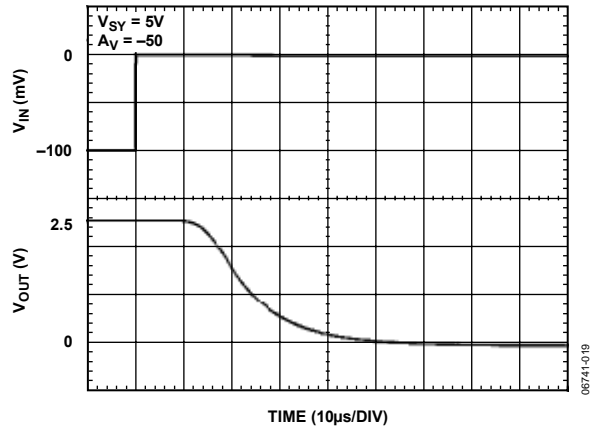


Figure 22. AD8538 Negative Overload Recovery

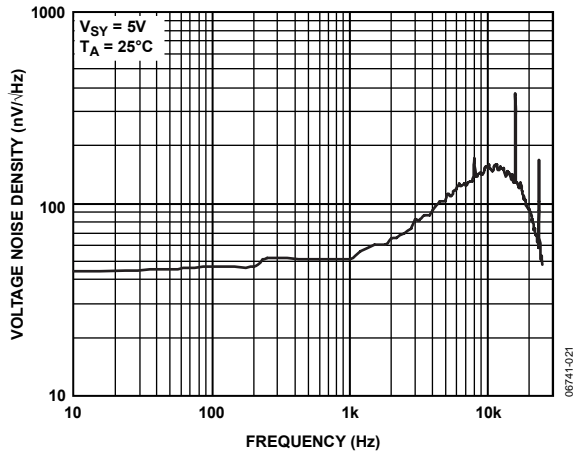


Figure 23. AD8538 Voltage Noise Density

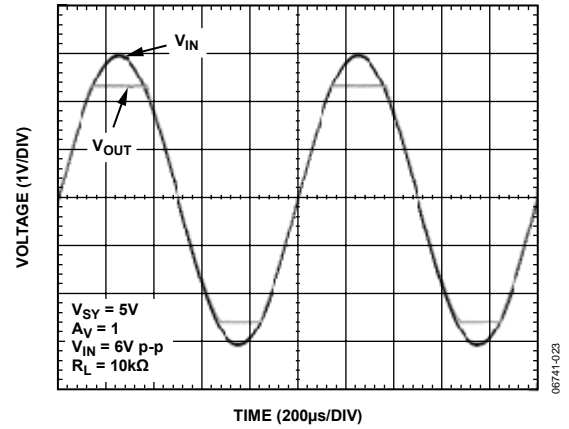


Figure 25. AD8538 No Phase Reversal

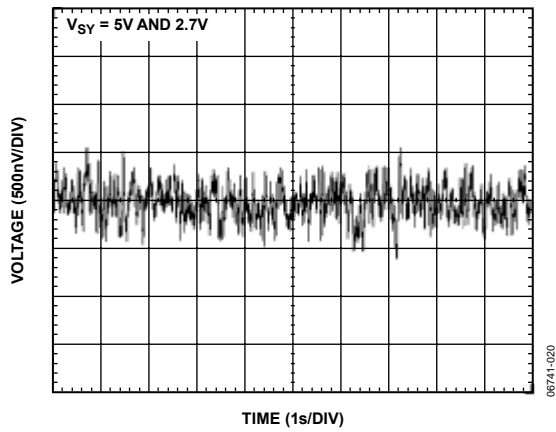


Figure 24. AD8538 0.1 Hz to 10 Hz Input Voltage Noise

AD8538/AD8539

$V_{SY} = 2.7\text{ V}$ or $\pm 1.35\text{ V}$, AD8538 only, unless otherwise noted.

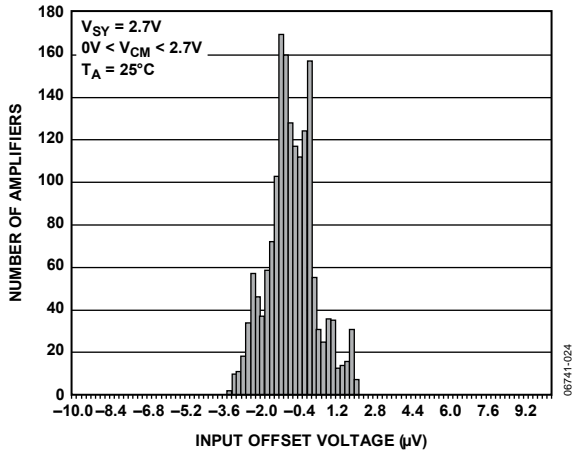


Figure 26. AD8538 Input Offset Voltage Distribution

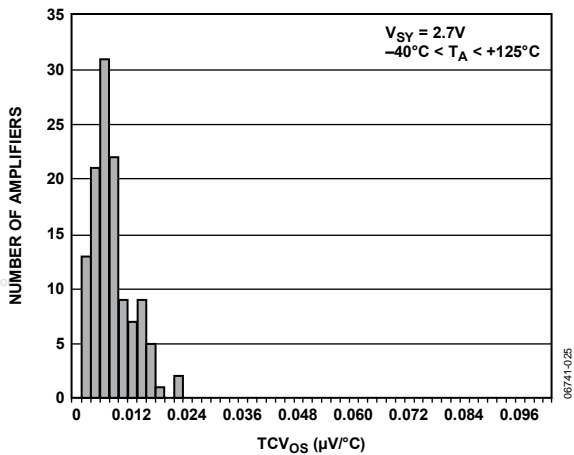


Figure 27. AD8538 Input Offset Voltage Drift Distribution

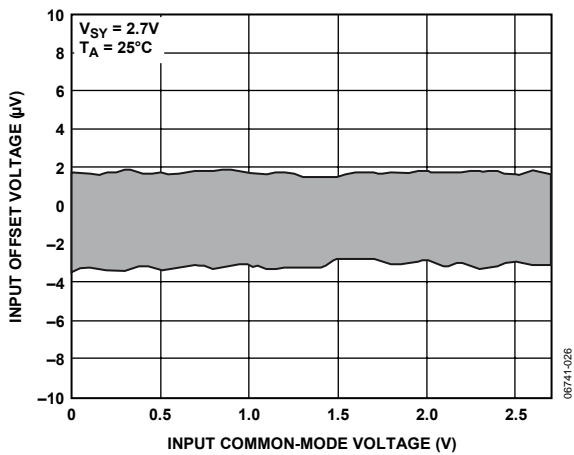


Figure 28. AD8538 Input Offset Voltage vs. Input Common-Mode Voltage

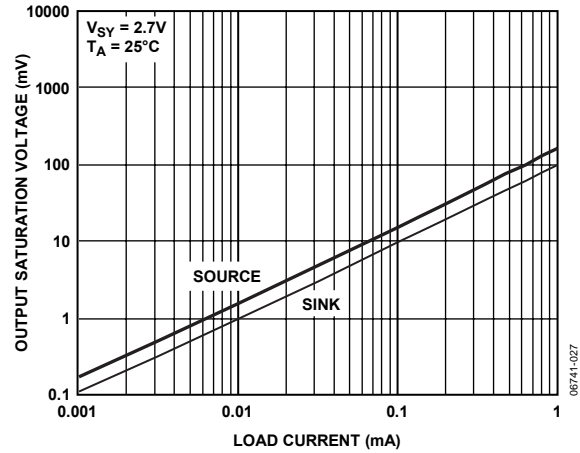


Figure 29. AD8538 Output Saturation Voltage vs. Load Current

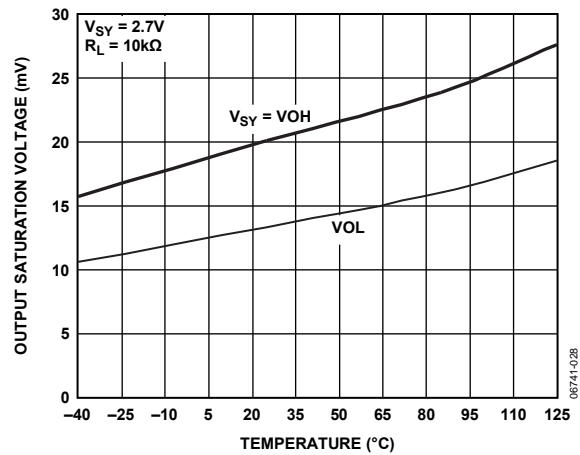


Figure 30. AD8538 Output Saturation Voltage vs. Temperature

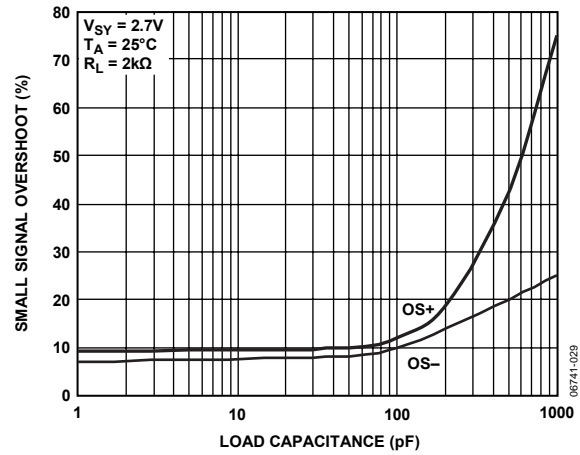


Figure 31. AD8538 Small Signal Overshoot vs. Load Capacitance

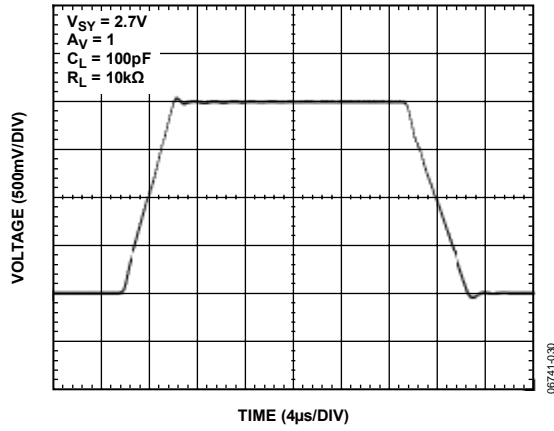


Figure 32. AD8538 Large Signal Transient Response

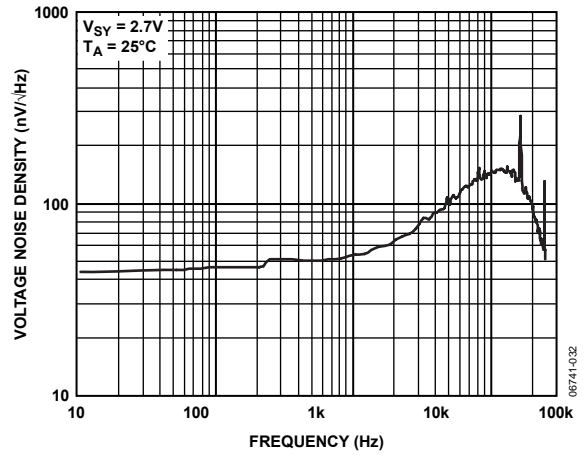


Figure 33. AD8538 Voltage Noise Density

AD8538/AD8539

AD8539 CHARACTERISTICS

AD8539 only, $V_S = 5\text{ V}$ or $\pm 2.5\text{ V}$, unless otherwise noted.

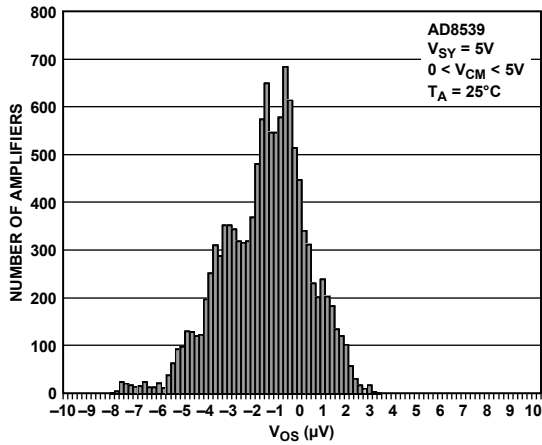


Figure 34. AD8539 Input Offset Voltage Distribution

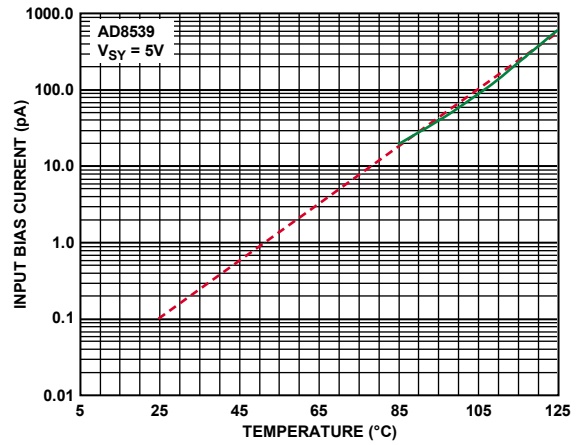


Figure 37. AD8539 Input Bias Current vs. Temperature

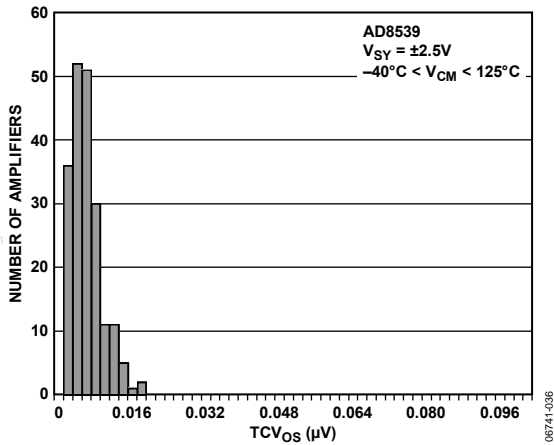


Figure 35. AD8539 Input Offset Voltage Drift Distribution

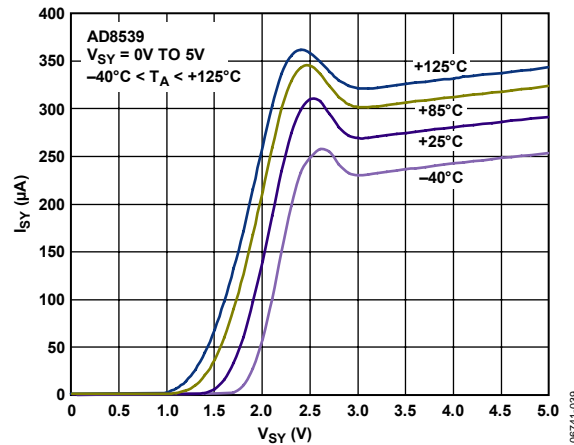


Figure 38. AD8539 Supply Current vs. Supply Voltage

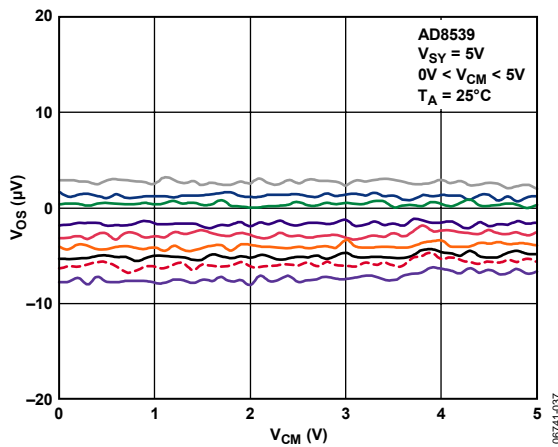


Figure 36. AD8539 Input Offset Voltage vs. Input Common-Mode Voltage

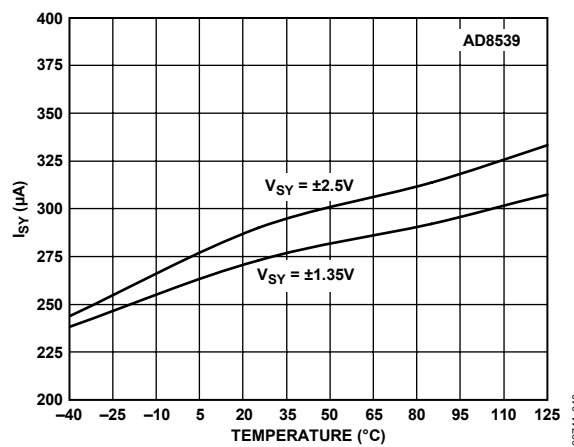


Figure 39. AD8539 Supply Current vs. Temperature

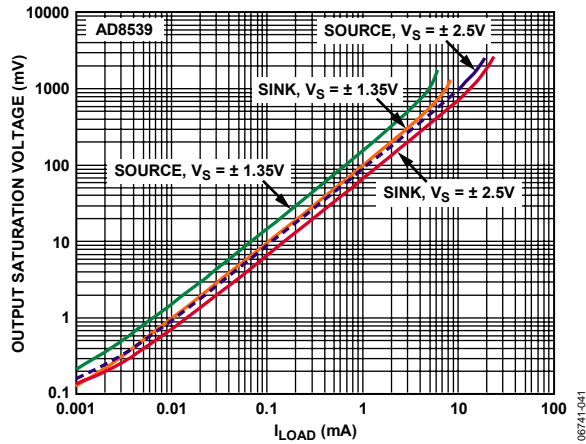


Figure 40. AD8539 Output Saturation Voltage vs. Load Current

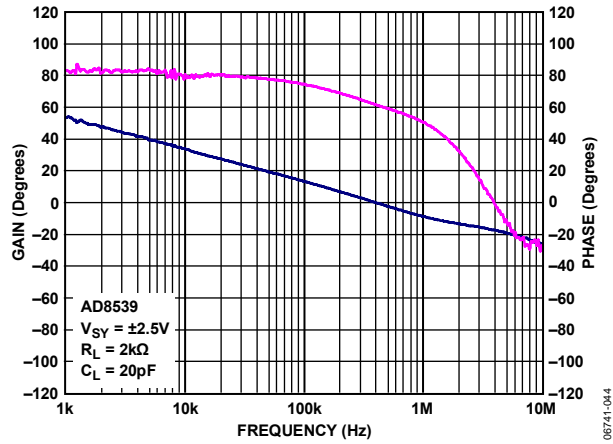


Figure 43. AD8539 Open-Loop Gain and Phase vs. Frequency

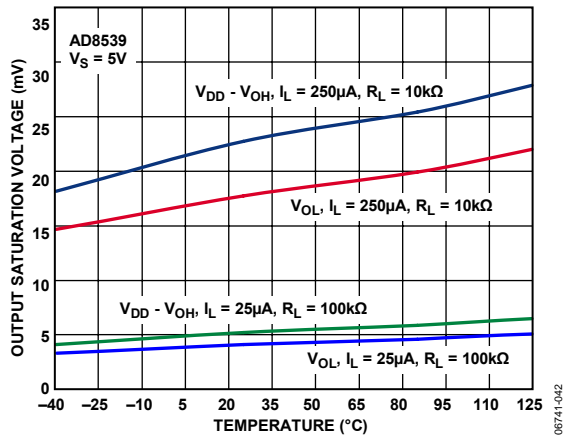


Figure 41. AD8539 Output Saturation Voltage vs. Temperature

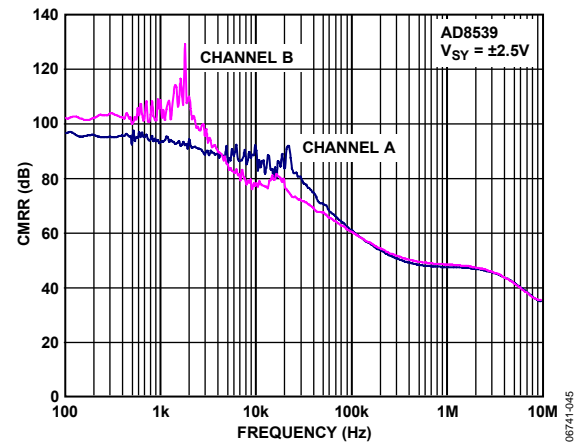


Figure 44. AD8539 CMRR vs. Frequency

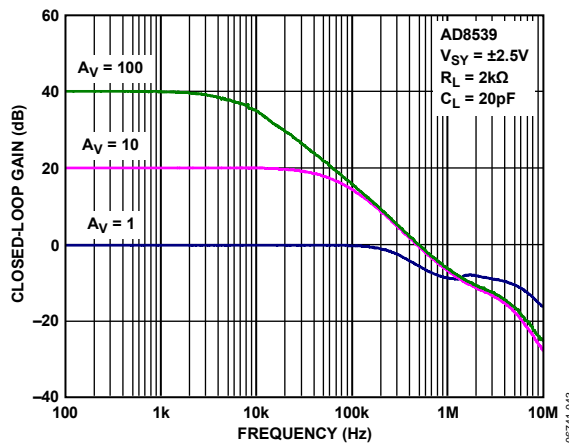


Figure 42. AD8539 Closed-Loop Gain vs. Frequency

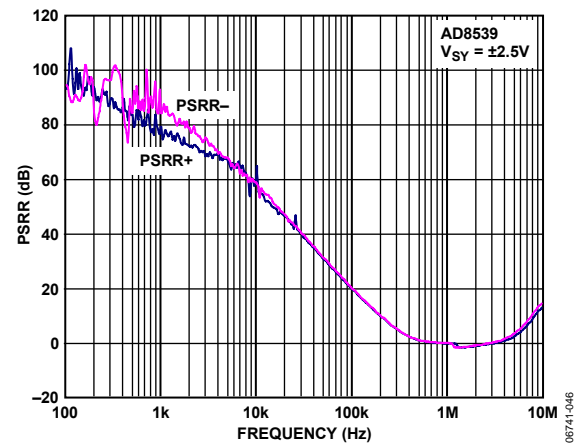


Figure 45. AD8539 PSRR vs. Frequency

AD8538/AD8539

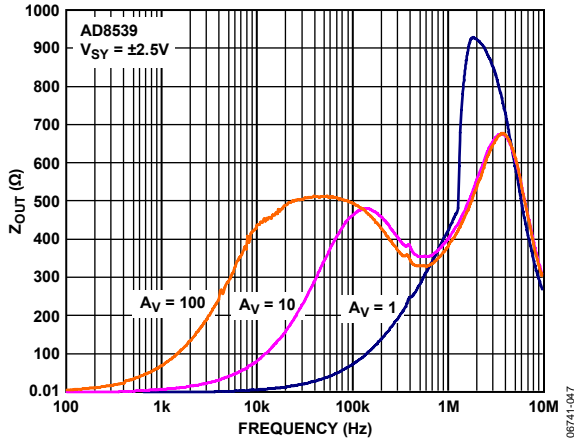


Figure 46. AD8539 Closed-Loop Output Impedance vs. Frequency

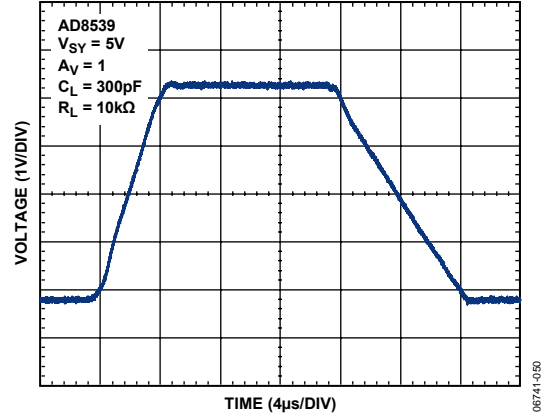


Figure 49. AD8539 Large Signal Transient Response

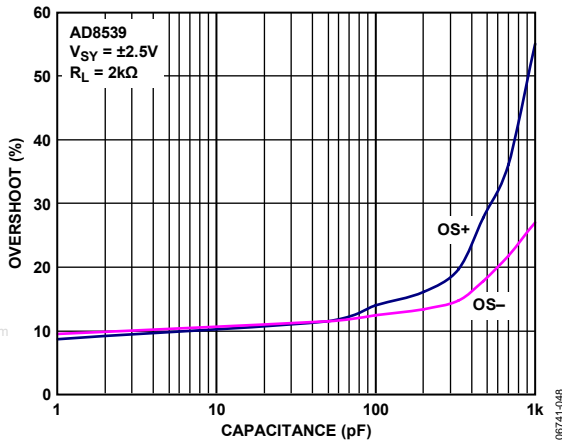


Figure 47. AD8539 Small Signal Overshoot vs. Load Capacitance

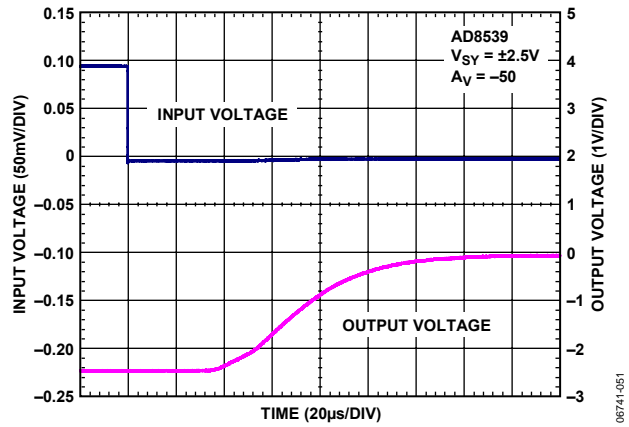


Figure 50. AD8539 Positive Overload Recovery

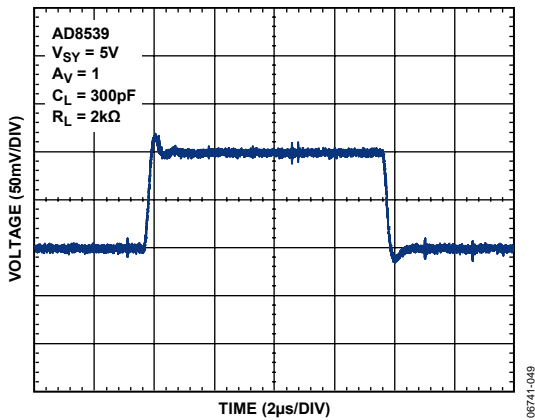


Figure 48. AD8539 Small Signal Transient Response

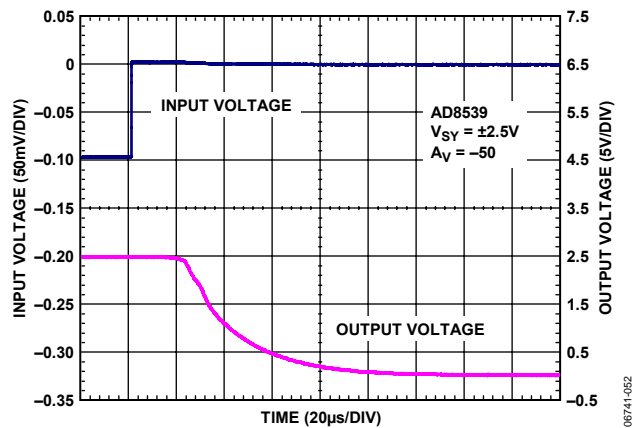


Figure 51. AD8539 Negative Overload Recovery

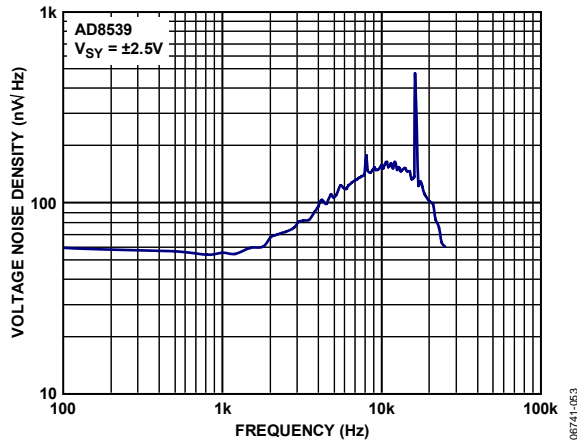


Figure 52. AD8539 Voltage Noise Density

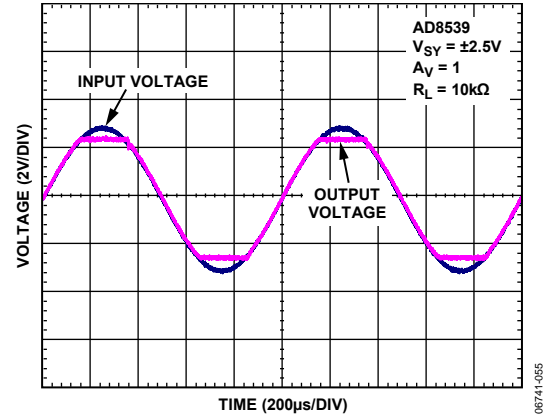


Figure 54. AD8539 No Phase Reversal

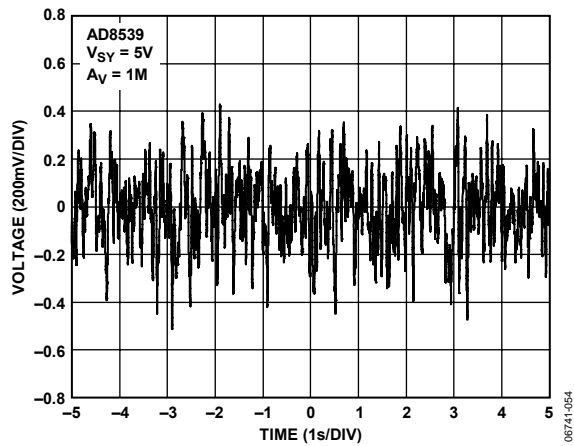


Figure 53. AD8539 0.1 Hz to 10 Hz Input Voltage Noise

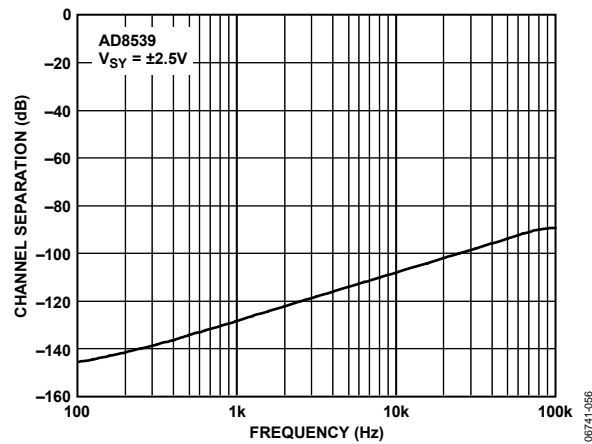


Figure 55. AD8539 Channel Separation vs. Frequency

AD8538/AD8539

$V_S = 2.7\text{ V}$ or $\pm 1.35\text{ V}$, $T_A = 25^\circ\text{C}$, AD8539 only, unless otherwise noted.

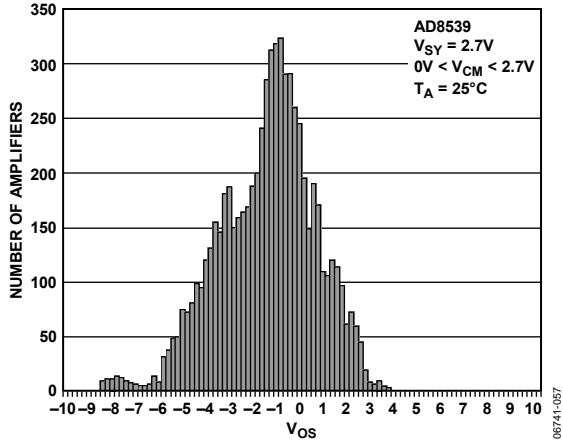


Figure 56. AD8539 Input Offset Voltage Distribution

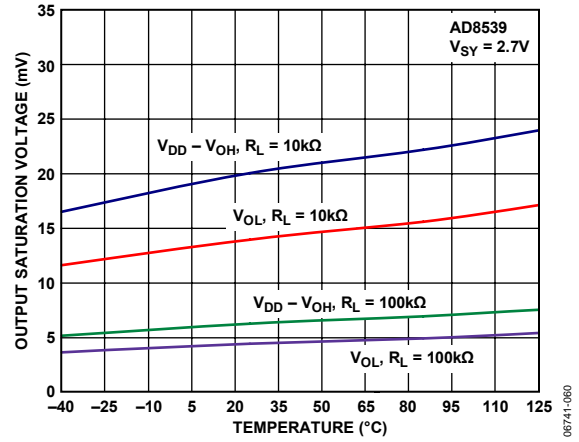


Figure 59. AD8539 Output Saturation Voltage vs. Temperature

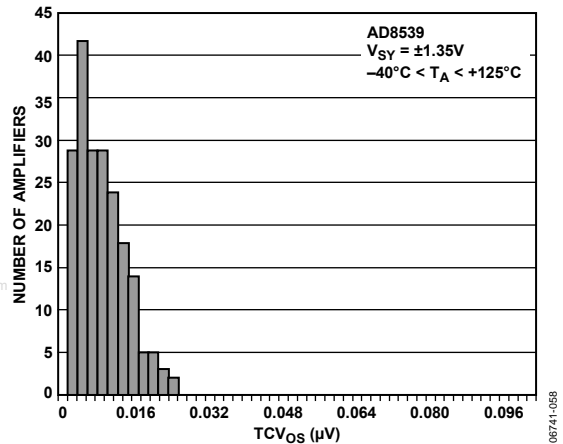


Figure 57. AD8539 Input Offset Voltage Drift Distribution

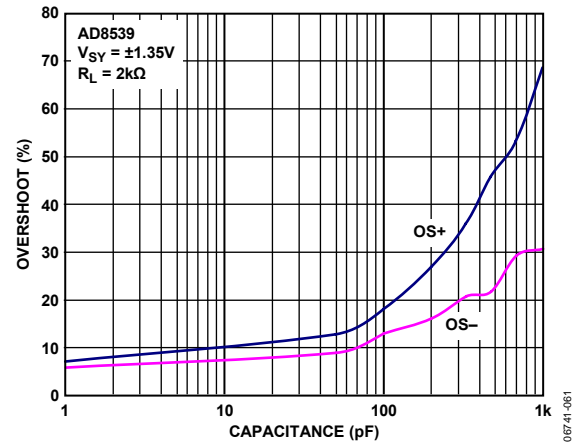


Figure 60. AD8539 Small Signal Overshoot vs. Load Capacitance

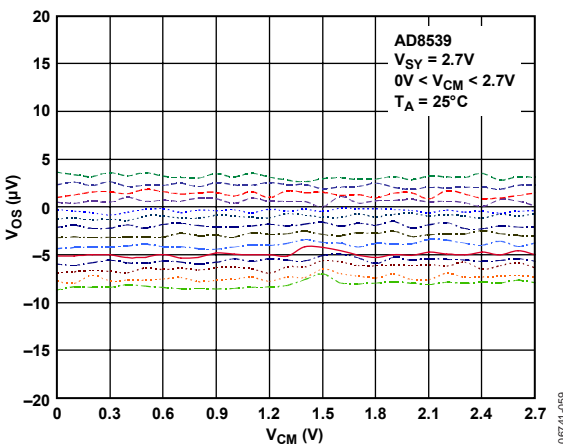


Figure 58. AD8539 Input Offset Voltage vs. Input Common-Mode Voltage

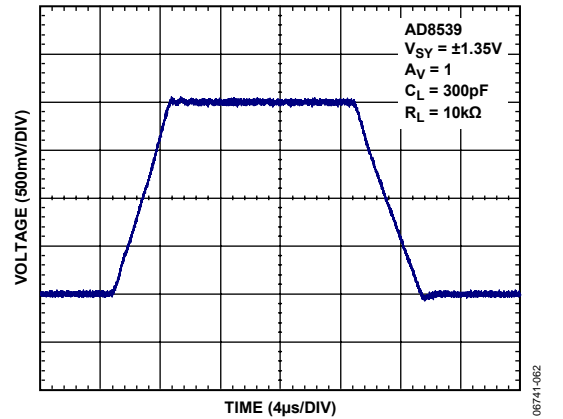


Figure 61. AD8539 Large Signal Transient Response

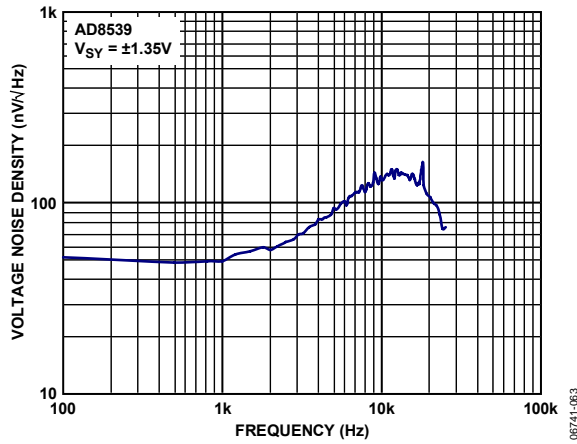


Figure 62. AD8539 Voltage Noise Density

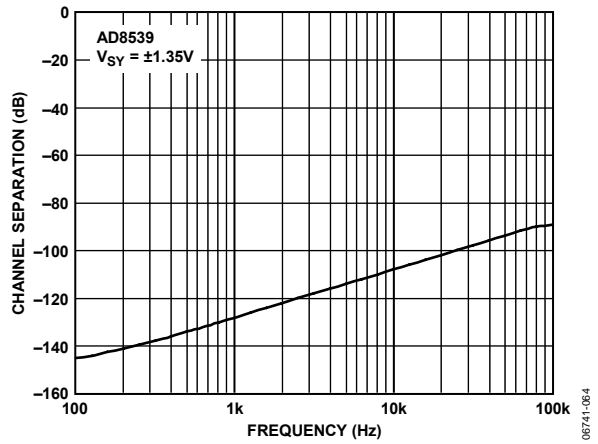
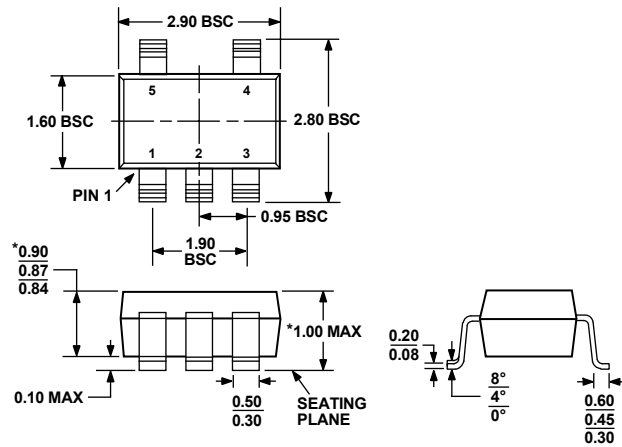


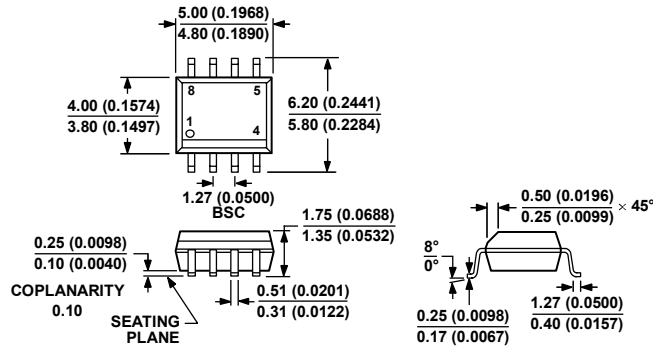
Figure 63. AD8539 Channel Separation vs. Frequency

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-193-AB WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 64. 5-Lead Thin Small Outline Transistor Package [TSOT-23] (UJ-5)
Dimensions shown in millimeters

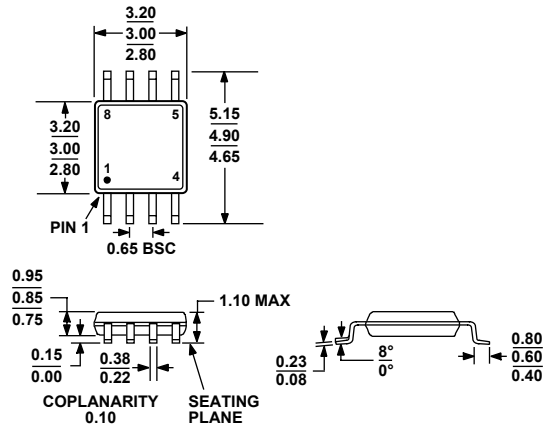


COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 65. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

012407A



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 66. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8538AUJZ-R2 ¹	-40°C to +125°C	5-Lead TSOT-23	UJ-5	A0C
AD8538AUJZ-REEL ¹	-40°C to +125°C	5-Lead TSOT-23	UJ-5	A0C
AD8538AUJZ-REEL7 ¹	-40°C to +125°C	5-Lead TSOT-23	UJ-5	A0C
AD8538ARZ ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8538ARZ-REEL ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8538ARZ-REEL7 ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8539ARMZ-R2 ¹	-40°C to +125°C	8-Lead MSOP	RM-8	A1S
AD8539ARMZ-REEL ¹	-40°C to +125°C	8-Lead MSOP	RM-8	A1S
AD8539ARZ ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8539ARZ-REEL ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
AD8539ARZ-REEL7 ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	

¹ Z = RoHS Compliant Part.

AD8538/AD8539

NOTES

NOTES

AD8538/AD8539

NOTES

www.DataSheet4U.com

©2005–2007 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D06741-0-5/07(A)



Rev. A | Page 24 of 24

www.analog.com

www.DataSheet4U.com