DATA SHEET

74LVC257A

Quad 2-input multiplexer with 5 Volt tolerant inputs/outputs; 3-state

Product specification
Supersedes data of 1998 Jul 29
File under Integrated Circuits, IC24

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Philips
Semiconductors

PHILIPS

Quad 2-input multiplexer with 5 Volt tolerant inputs/outputs; 3-state

74LVC257A

FEATURES

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range of 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no. 8-1A
- Specified from –40 to +85 and +125 °C.

DESCRIPTION

The 74LVC257A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V environment.

The 74LVC257A is a quad 2-input multiplexer with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common select input (S). The data inputs from source 0 ($1I_0$ to $4I_0$) are selected when input S is LOW and the data inputs from source 1 ($1I_1$ to $4I_1$) are selected when input S is HIGH. Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the selected inputs.

The 74LVC157A is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S. The outputs are forced to a high impedance OFF-state when $\overline{OE}$ is HIGH.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay			
	nI_0, nI_1 to nY	C_L = 50 pF; V_{CC} = 3.3 V	2.6	ns
	S to nY	C_L = 50 pF; V_{CC} = 3.3 V	2.9	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V; notes 1 and 2	17	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz; f_o = output frequency in MHz;

   a) C_L = output load capacitance in pF; V_{CC} = supply voltage in V;

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC257AD	–40 to +125 °C	16	SO	plastic	SOT109-1
74LVC257ADB		16	SSOP	plastic	SOT338-1
74LVC257APW		16	TSSOP	plastic	SOT403-1
74LVC257ABQ		16	HVQFN16	plastic	SOT763-1

FUNCTION TABLE

See note 1.

INPUTS				OUTPUTS
$\overline{OE}$	**S**	**nI_0**	**nI_1**	**nY**
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don’t care:
   Z = high impedance OFF-state.

PINNING FOR SO, SSOP AND TSSOP

PIN	SYMBOL	DESCRIPTION
1	S	common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	data inputs from sources 0
3, 6, 10, 13	$1I_1$ to $4I_1$	data inputs from sources 1
4, 7, 9, 12	1Y to 4Y	3-state multiplexer outputs
8	GND	ground (0 V)
15	$\overline{OE}$	3-state output enable input (active LOW)
16	V_{CC}	DC supply voltage

PINNING FOR HVQFN16

PIN	SYMBOL	DESCRIPTION
16	S	common data select input
1, 4, 10, 13	$1I_0$ to $4I_0$	data inputs from sources 0
2, 5, 9, 12	$1I_1$ to $4I_1$	data inputs from sources 1
3, 6, 8, 11	1Y to 4Y	3-state multiplexer outputs
7	GND	ground (0 V)
14	$\overline{OE}$	3-state output enable input (active LOW)
15	V_{CC}	DC supply voltage

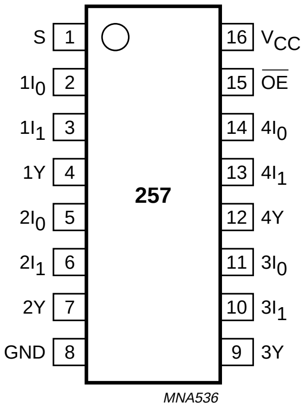


Fig.1 Pin configuration SO, SSOP and TSSOP.

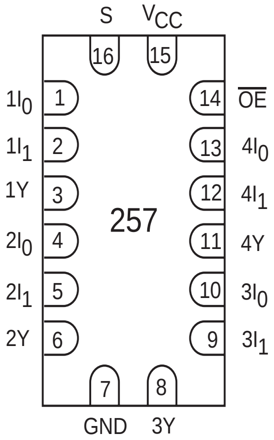


Fig.2 Pin configuration HVQFN16.

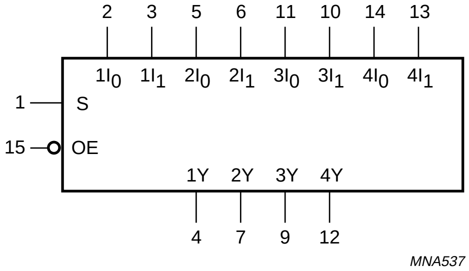


Fig.3 Logic symbol.

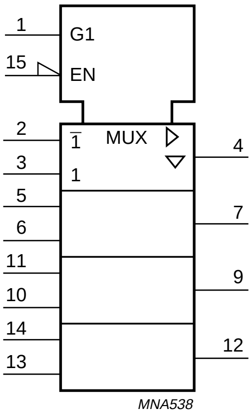


Fig.4 Logic symbol (IEEE/IEC).

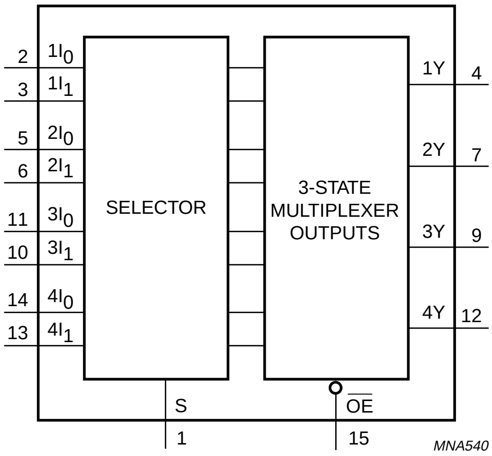


Fig.5 Functional diagram.

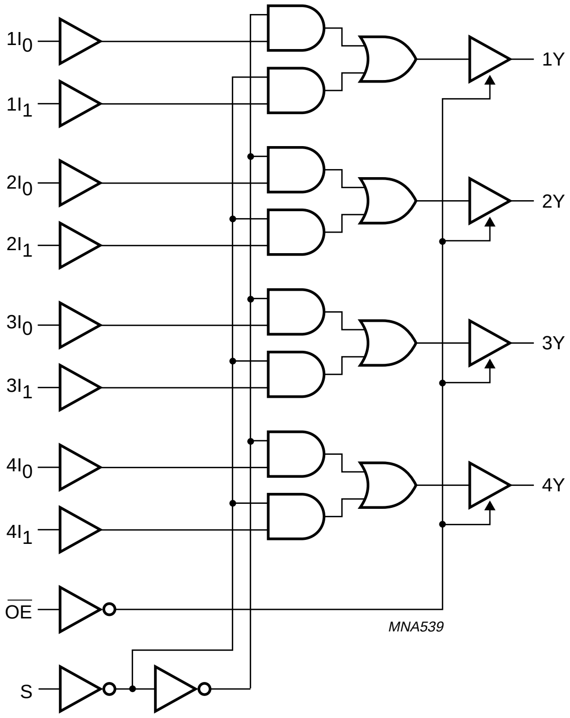


Fig.6 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		CONDITIONS	LIMITS		UNIT
				MIN.	MAX.	
V_{CC}	DC supply voltage (for max. speed performance)			2.7	3.6	V
	DC supply voltage (for low-voltage applications)			1.2	3.6	V
V_I	DC input voltage range			0	5.5	V
V_O	DC output voltage range	output HIGH or LOW state		0	V_{CC}	V
		output 3-state		0	5.5	V
T_{amb}	operating ambient temperature range			–40	+125	°C
t_r,t_f	input rise and fall times		V_{CC} = 1.2 to 2.7 V	0	20	ns/V
			V_{CC} = 2.7 to 3.6 V	0	10	

LIMITING VALUES

In accordance with the absolute maximum rating system (IEC 60134). Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER		CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC supply voltage			–0.5	+6.5	V
I_{IK}	DC input diode current		$V_I < 0$	–	–50	mA
V_I	DC input voltage		note 1	–0.5	+6.5	V
I_{OK}	DC output diode current		$V_O > V_{CC}$ or $V_O < 0$	–	±50	mA
V_O	DC output voltage	output HIGH or LOW state	note 1	–0.5	V_{CC} + 0.5	V
V_O	DC output voltage	output 3-state	note 1	–0.5	+ 6.5	V
I_O	DC output source or sink current		V_O = 0 to V_{CC}	–	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current			–	±100	mA
T_{stg}	storage temperature range			–65	+150	°C
P_{tot}	power dissipation per package					
	plastic mini-pack (SO)		above +70 °C derate linearly with 8 mW/K	–	500	mW
	plastic shrink mini-pack (SSOP and TSSOP)		above +60 °C derate linearly with 5.5 mW/K	–	500	mW
	plastic quad flat pack no lead (HVQFN16)		above +60 °C derate linearly with 4.5 mW/K	–	500	mW

Note

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)			T_{amb} (°C)		UNIT
		OTHER	V_{CC} (V)	–40 to +85			–40 to +125		
				MIN.	TYP.$^{(1)}$	MAX.	MIN.	MAX.	
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V_{CC}	–	V
			2.7 to 3.6	2.0	–	–	2.0	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	–	GND	V
			2.7 to 3.6	–	–	0.8	–	0.8	V
V_{OH}	HIGH-level output voltage; $V_I = V_{IH}$ or V_{IL}	$I_O = –100\ \mu A$	2.7 to 3.6	$V_{CC} – 0.2$	V_{CC}	–	$V_{CC} – 0.3$	–	V
		$I_O = –12$ mA	2.7	$V_{CC} – 0.5$	–	–	$V_{CC} – 0.65$	–	V
		$I_O = –18$ mA	3.0	$V_{CC} – 0.6$	–	–	$V_{CC} – 0.75$	–	V
		$I_O = –24$ mA	3.0	$V_{CC} – 0.8$	–	–	$V_{CC} – 1$	–	V
V_{OL}	LOW-level output voltage; $V_I = V_{IH}$ or V_{IL}	$I_O = 100\ \mu A$	2.7 to 3.6	–	GND	0.2	–	0.3	V
		$I_O = 12$ mA	2.7	–	–	0.4	–	0.6	V
		$I_O = 24$ mA	3.0	–	–	0.55	–	0.8	V
I_I	input leakage current	$V_I = 5.5$ V or GND	3.6	–	±0.1	±5	–	±20	μA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = 5.5$ V or GND note 2	3.6	–	±0.1	±5	–	±20	μA
I_{off}	power off leakage supply	V_I or $V_O = 5.5$ V	0.0	–	±0.1	±10	–	±20	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$	3.6	–	0.1	10	–	40	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC} – 0.6V$ $I_O = 0$	2.7 to 3.6	–	5	500	–	5000	μA

Notes

1. All typical values are at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.
2. For I/O ports the parameter I_{OZ} includes the input leakage current.

AC CHARACTERISTICS

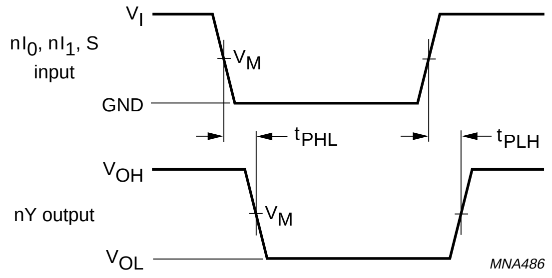
GND = 0 V; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	WAVEFORMS	T_{amb} (°C)					UNIT
			–40 to +85			–40 to +125		
			MIN.	TYP.(1)	MAX.	MIN.	MAX.	
V_{CC} = 1.2 V								
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY, nI_1 to nY	see Figs 6 and 8	–	13	–	–	–	ns
t_{PHL}/t_{PLH}	propagation delay S to nY	see Figs 6 and 8	–	15	–	–	–	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY	see Figs 7 and 8	–	18	–	–	–	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY	see Figs 7 and 8	–	10	–	–	–	ns
V_{CC} = 2.7 V								
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY, nI_1 to nY	see Figs 6 and 8	1.5	3.0	5.4	1.5	7.0	ns
t_{PHL}/t_{PLH}	propagation delay S to nY	see Figs 6 and 8	1.5	3.4	7.5	1.5	9.5	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY	see Figs 7 and 8	1.5	4.1	6.7	1.5	8.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY	see Figs 7 and 8	1.5	3.1	4.7	1.5	6.0	ns
V_{CC} = 3.0 to 3.6 V								
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY, nI_1 to nY	see Figs 6 and 8	1.0	2.6	4.6	1.0	6.0	ns
t_{PHL}/t_{PLH}	propagation delay S to nY	see Figs 6 and 8	1.0	2.9	6.4	1.0	8.0	ns
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY	see Figs 7 and 8	1.0	3.3	5.6	1.0	7.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY	see Figs 7 and 8	1.0	2.8	4.3	1.0	5.5	ns
$t_{sk(0)}$	skew	note 2			1.0		1.5	ns

Notes

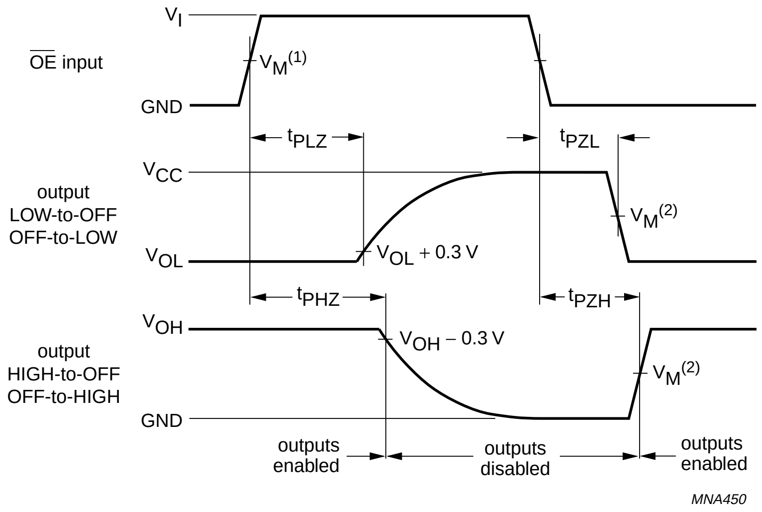
1. Typical values at V_{CC} = 3.3 V.
2. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

AC WAVEFORMS



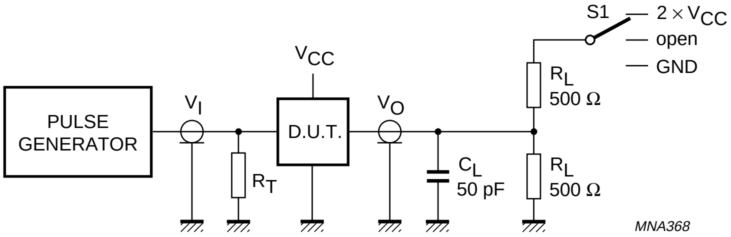
$V_M^{(1)}$ = 1.5 V at $V_{CC} \geq 2.7$ V;
$V_M^{(1)}$ = 0.5 V_{CC} at $V_{CC} < 2.7$ V;
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 Data inputs (nI_0, nI_1) and common data select input (S) to output (nY) propagation delays.



$V_M^{(1)}$ = 1.5 V at $V_{CC} \geq 2.7$ V;
$V_M^{(1)}$ = 0.5 V_{CC} at $V_{CC} < 2.7$ V;
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 3-state enable and disable times.



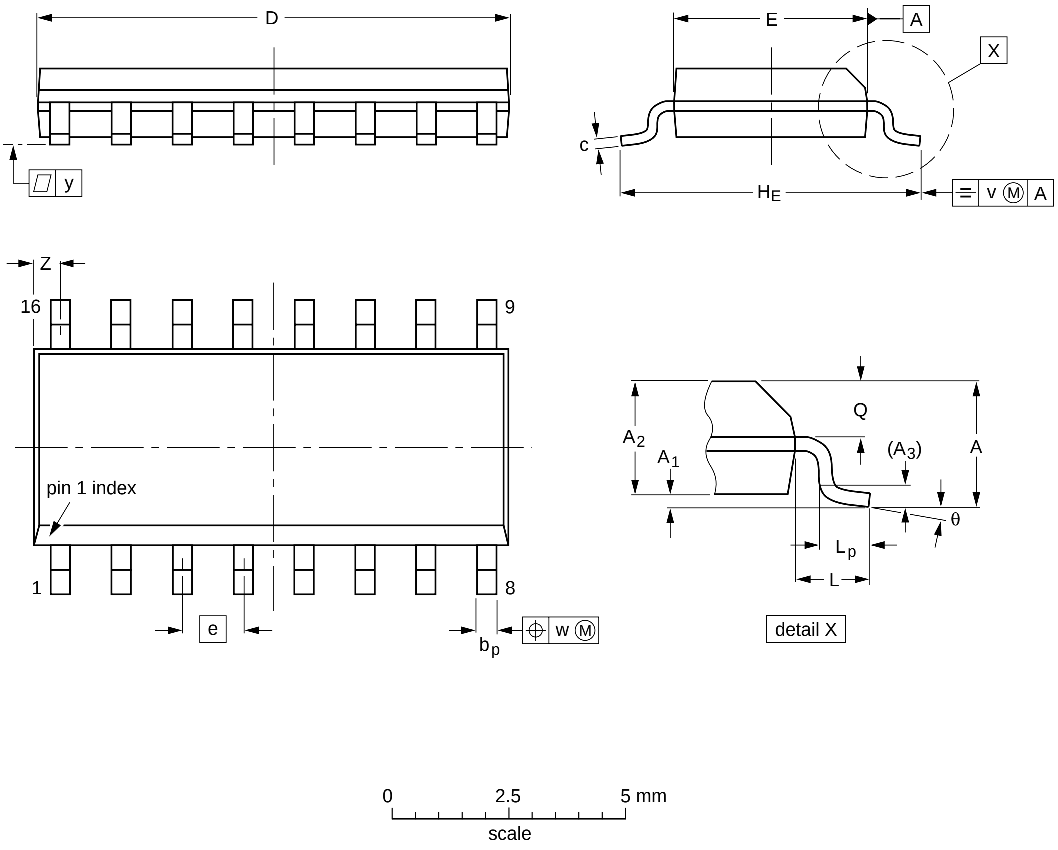
V_{CC}	V_I	t_{PLH}/t_{PHL}
1.2 V	V_{CC}	open
2.7 V	2.7 V	open
3.0 to 3.6 V	2.7 V	open

Definitions for test circuits:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance (see Chapter “AC characteristics”).
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.8 Load circuitry for switching times.

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

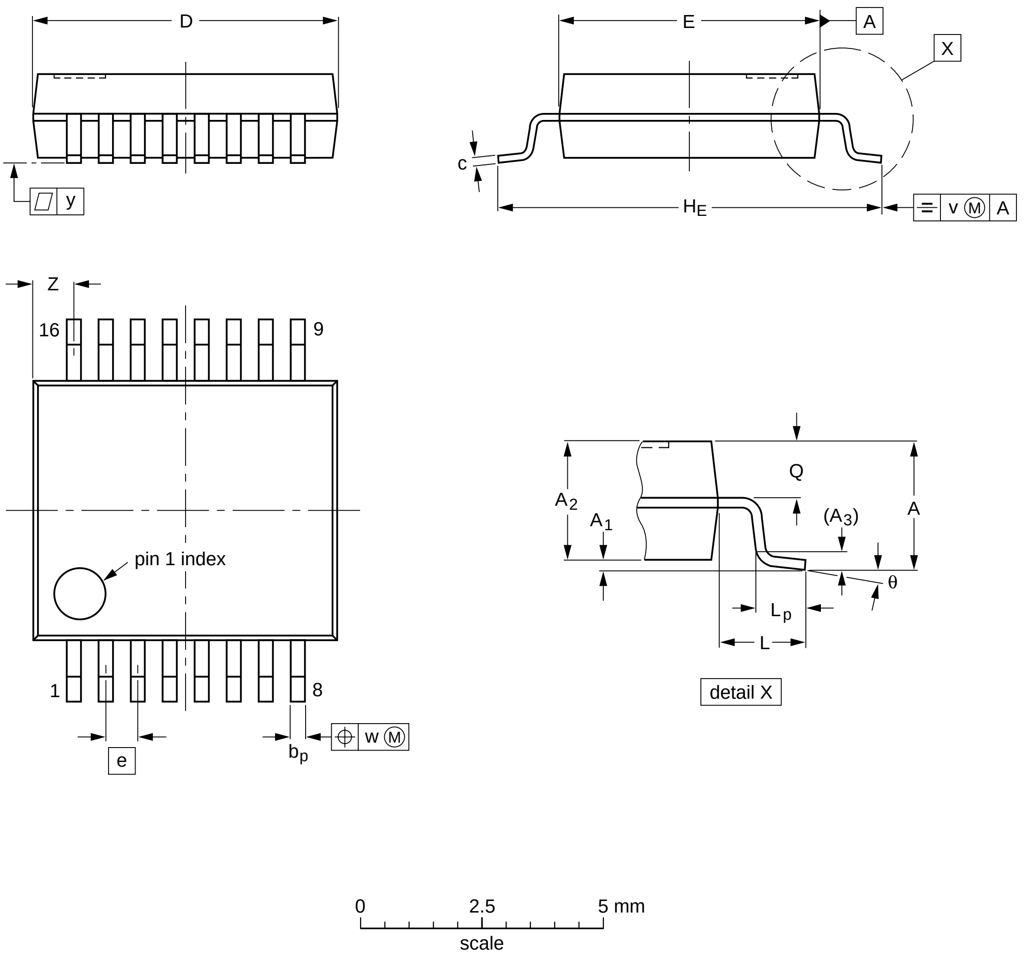
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				~~97-05-22~~ 99-12-27

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

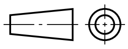


DIMENSIONS (mm are the original dimensions)

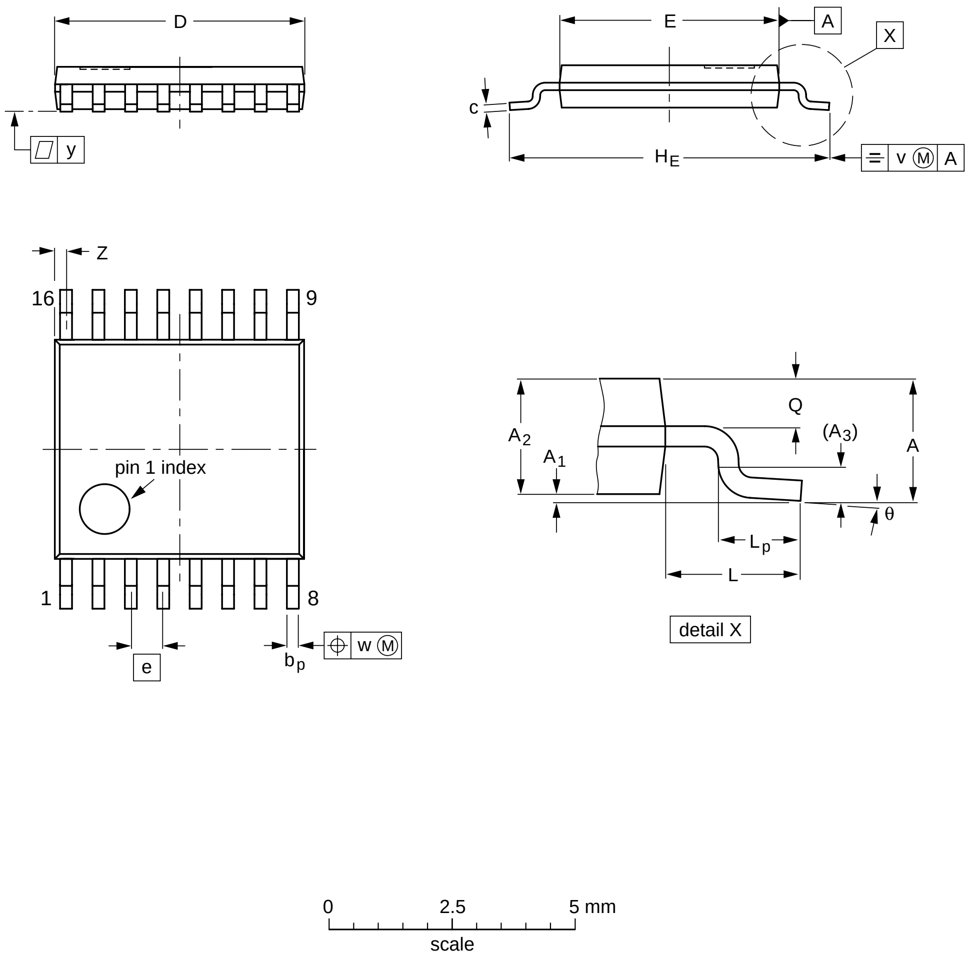
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^{o} 0^{o}

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150				~~95-02-04~~ 99-12-27

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm SOT403-1

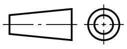


DIMENSIONS (mm are the original dimensions)

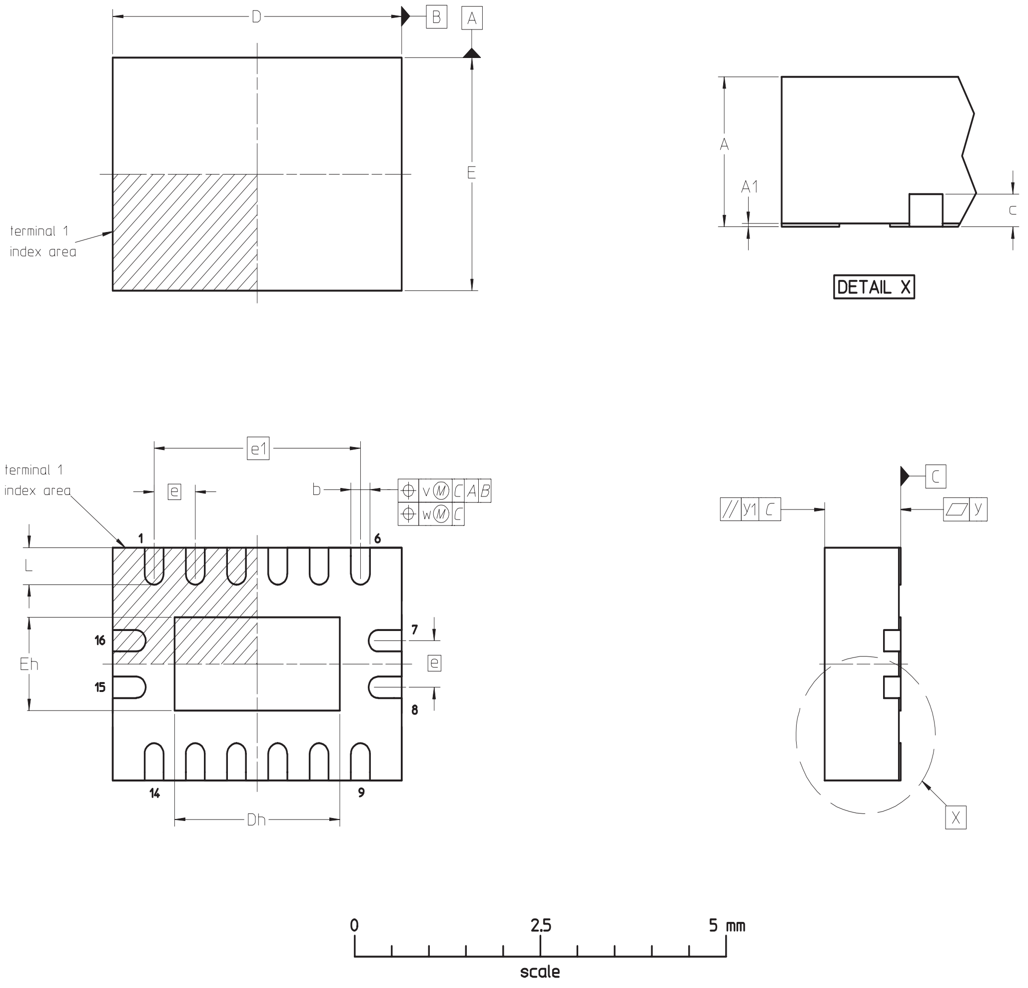
UNIT	A max.	A_1	A_2	A_3	b_p	c	D [1]	E [2]	e	H_E	L	L_p	Q	v	w	y	Z [1]	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~95-04-04~~ 99-12-27

HVQFN16 : plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.50 x 3.50 x 0.85 mm. SOT763-1



DIMENSIONS (mm are the controlling dimensions)

UNIT	A (1) max.	A_1	b	c	D (1)	D_h	E (1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Notes

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	-------	MO-220	-------			

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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