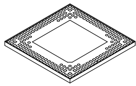
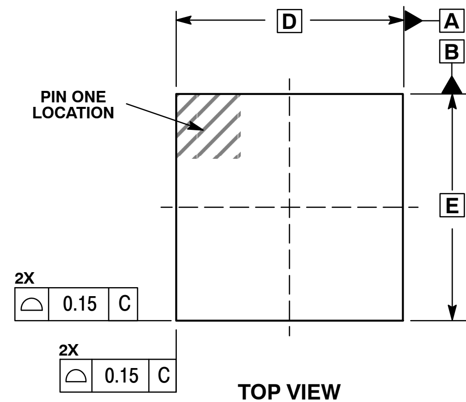


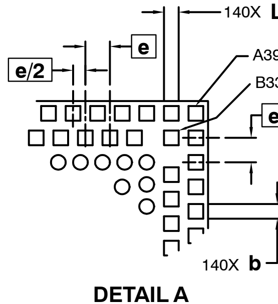
SCALE 1:1

TLLGA140 10x10, 0.5P, Dual−Row, Staggered−Pad
CASE 513AL−01
ISSUE O

DATE 20 OCT 2009



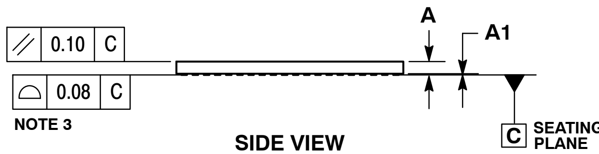
TOP VIEW



DETAIL A

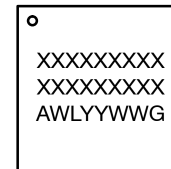
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MAX
A	0.50	0.60
A1	---	0.05
b	0.25	0.35
D	10.00 BSC	
D2	5.70	5.90
E	10.00 BSC	
E2	5.70	5.90
e	0.50 BSC	
L	0.25	0.35

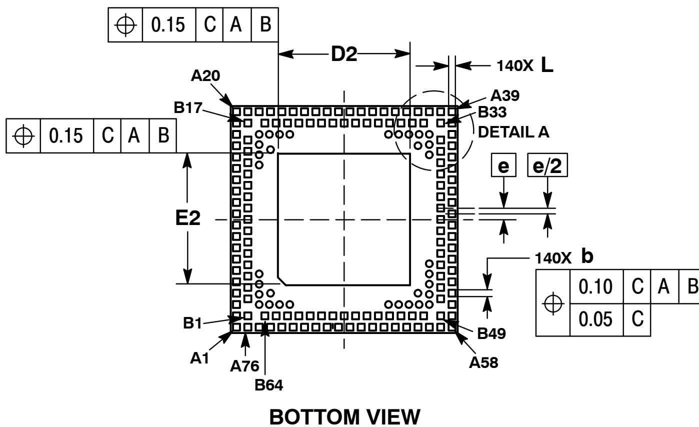


SIDE VIEW

GENERIC MARKING DIAGRAM

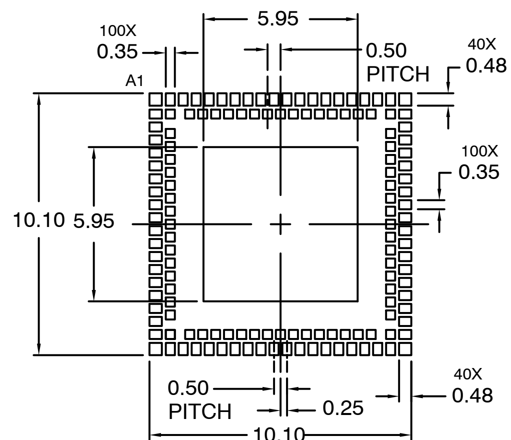


XXXXX = Device Code
A = Assembly Site
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package



BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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