

Wide Frequency range Timing-Safe™ Peak EMI reduction IC

General Features

- 1x , LVCMOS Timing-Safe™ Peak EMI Reduction
- Input frequency:
 - 2MHz - 16MHz @ 2.5V
 - 2MHz - 20MHz @ 3.3V
- Output frequency (Timing-Safe™):
 - 2MHz - 16MHz @ 2.5V
 - 2MHz - 20MHz @ 3.3V
- Analog Spread Selection up to ±1.5%
- External Input-Output Delay Control option
- Power Down option for Power Save mode
- Supply Voltage: 2.5V±0.2V
3.3V ± 0.3V
- Commercial temperature range
- 8 pin, TSSOP, and TDFN(2X2) COL packages
- The First True Drop-in Solution

input from an external reference, and locks on to it delivering a 1x Timing-Safe™ clock. PCS3P73Z01AW has a Frequency Selection (FS) control that facilitates selecting one of the two frequency ranges within the operating frequency range. Refer to the frequency Selection table for details. The device has an SSEXTR pin to select different deviation and associated Input-Output Skew (T_{skew}), depending upon the value of an external resistor connected between SSEXTR and GND. PCS3P73Z01AW has a DLY_CTRL for adjusting the Input-Output clock delay, depending upon the value of capacitor connected at this pin to GND. PD#/OE provides the Power Down option. Outputs will be tri-stated when power down is active.

PCS3P73Z01AW operates from a 2.5V/3.3V supply and is available in an 8 Pin TSSOP, and TDFN (2X2) COL Packages, over Commercial temperature range.

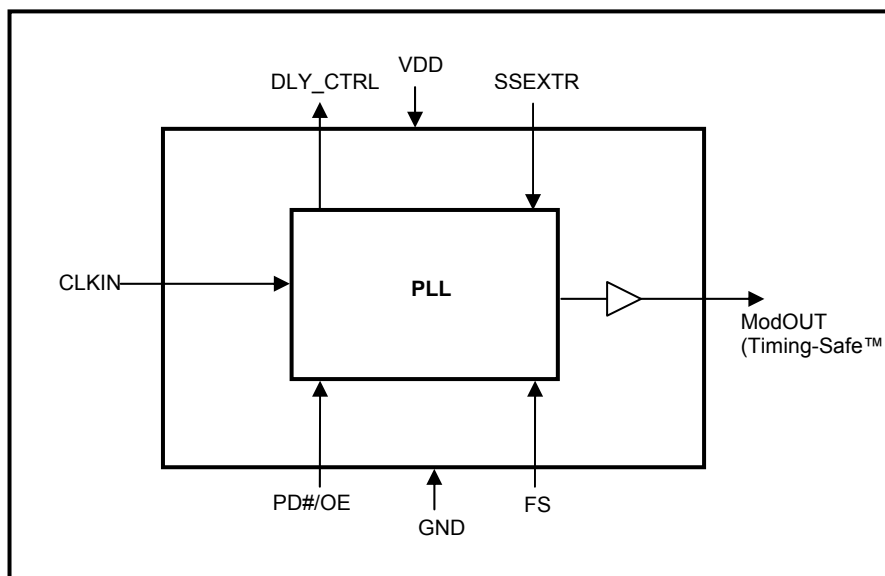
Functional Description

PCS3P73Z01AW is a 2.5V/3.3V versatile EMI reduction IC based on PulseCore Semiconductor's patent pending Timing-Safe™ technology. PCS3P73Z01AW accepts one

Application

PCS3P73Z01AW is targeted for use in Displays, Camera modules and SDRAM memory interface systems.

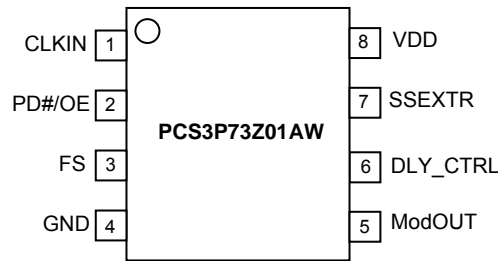
Block Diagram



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Pin Configuration



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Pin Description

| Pin # | Type | Pin Name | Description |
|-------|------|----------|--|
| 1 | I | CLKIN | External reference Clock input. |
| 2 | I | PD#/OE | Power Down. Pull LOW to enable Power Down. Outputs will be tri-stated when power down is enabled. Pull HIGH to disable power down and enable output. |
| 3 | I | FS | Frequency Select (see Frequency Selection table for details). |
| 4 | P | GND | Ground |
| 5 | O | ModOUT | Buffered modulated Timing-Safe™ clock output |
| 6 | O | DLY_CTRL | External Input-Output Delay control |
| 7 | I | SSEXTR | Analog Spread Selection through external resistor to GND. |
| 8 | P | VDD | 2.5V / 3.3V supply Voltage |

Frequency Selection Table

| VDD | FS | Frequency(MHz) |
|------|----|----------------|
| 2.5V | 0 | 2-6 |
| | 1 | 6-16 |
| 3.3V | 0 | 2-6 |
| | 1 | 6-20 |

Absolute Maximum Rating

| Symbol | Parameter | Rating | Unit |
|------------------|---|--------------|------|
| V _{DD} | Voltage on any pin with respect to Ground | -0.5 to +4.6 | V |
| T _{STG} | Storage temperature | -65 to +125 | °C |
| T _s | Max. Soldering Temperature (10 sec) | 260 | °C |
| T _J | Junction Temperature | 150 | °C |
| T _{DV} | Static Discharge Voltage (As per JEDEC STD22- A114-B) | 2 | KV |

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions

| Parameter | Description | Min | Max | Unit |
|-----------------------|---|-----|-----|------|
| V _{DD(3.3V)} | Supply Voltage | 3.0 | 3.6 | V |
| V _{DD(2.5V)} | Supply Voltage | 2.3 | 2.7 | V |
| T _A | Operating Temperature (Ambient Temperature) | 0 | +70 | °C |
| C _L | Load Capacitance | | 10 | pF |
| C _{IN} | Input Capacitance | | 7 | pF |

Electrical Characteristics for 2.5V Supply

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|-----------------|------------------------|-----------------------------------|-------|-----|-----|------|
| V _{DD} | Supply Voltage | | 2.3 | 2.5 | 2.7 | V |
| V _{IL} | Input LOW Voltage | | | | 0.7 | V |
| V _{IH} | Input HIGH Voltage | | 1.7 | | | V |
| I _{IL} | Input LOW Current | V _{IN} = 0V | | | 50 | μA |
| I _{IH} | Input HIGH Current | V _{IN} = V _{DD} | | | 50 | μA |
| V _{OL} | Output LOW Voltage | I _{OL} = 8mA | | | 0.6 | V |
| V _{OH} | Output HIGH Voltage | I _{OH} = -8mA | 1.8 | | | V |
| I _{CC} | Static Supply Current | CLKIN & PD#/OE pins pulled to GND | | | 2 | μA |
| I _{DD} | Dynamic Supply Current | Unloaded Output | 2MHz | 2 | | mA |
| | | | 6MHz | 5 | | |
| | | | 16MHz | 6 | | |
| Z _o | Output Impedance | | | 36 | | Ω |

Electrical Characteristics for 3.3V Supply

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|-----------------|------------------------|-------------------------------------|-------|-----|-----|------|
| V _{DD} | Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| V _{IH} | Input HIGH Voltage | | 2.0 | | | V |
| V _{IL} | Input LOW Voltage | | | | 0.8 | V |
| I _{IH} | Input HIGH Current | V _{IN} = V _{DD} | | | 50 | μA |
| I _{IL} | Input LOW Current | V _{IN} = 0V | | | 50 | μA |
| V _{OH} | Output HIGH Voltage | I _{OH} = -8mA | 2.4 | | | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 8mA | | | 0.4 | V |
| I _{CC} | Static Supply Current | CLKIN pulled Low, PD#/OE pulled Low | | | 2 | μA |
| I _{DD} | Dynamic Supply Current | Unloaded outputs | 2MHz | 4 | | mA |
| | | | 6MHz | 7 | | |
| | | | 20MHz | 9 | | |
| Z _o | Output Impedance | | | 27 | | Ω |

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Switching Characteristics for 2.5V

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|--|--|----------------|-----|------|------|
| Input Frequency | FS=0 | 2 | | 6 | MHz |
| | FS=1 | 6 | | 16 | |
| ModOUT | FS=0 | 2 | | 6 | MHz |
| | FS=1 | 6 | | 16 | |
| Duty Cycle ^{1,2} | Measured at $V_{DD}/2$ | 45 | 50 | 55 | % |
| Rise Time ^{1,2} | Measured between 20% to 80% | | 1.7 | | nS |
| Fall Time ^{1,2} | Measured between 80% to 20% | | 0.9 | | nS |
| Cycle-to-Cycle Jitter ² | Unloaded outputs | FS=0; @ 5 MHz | | ±225 | pS |
| | | FS=1; @ 15 MHz | | ±150 | |
| Input-to-Output propagation Delay ² | Unloaded outputs with SSEXTR pin OPEN, No load on DLY_CTRL | FS=0; @ 6 MHz | | 175 | pS |
| | | FS=1; @ 12 MHz | | 75 | |
| PLL Lock Time ² | Stable power supply, valid clock presented on CLKIN pin | | | 3 | mS |

Notes: 1. All parameters are specified with 10 pF loaded outputs
 2. Parameter is guaranteed by design and characterization. Not 100% tested in production

Switching Characteristics for 3.3V

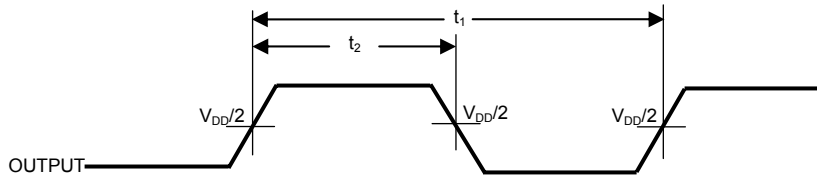
| Parameter | Test Conditions | Min | Typ | Max | Unit |
|--|--|----------------|-----|------|------|
| Input Frequency | FS=0 | 2 | | 6 | MHz |
| | FS=1 | 6 | | 20 | |
| ModOUT | FS=0 | 2 | | 6 | MHz |
| | FS=1 | 6 | | 20 | |
| Duty Cycle ^{3,4} | Measured at $V_{DD}/2$ | 45 | 50 | 55 | % |
| Rise Time ^{3,4} | Measured between 20% to 80% | | 1.2 | | nS |
| Fall Time ^{3,4} | Measured between 80% to 20% | | 0.8 | | nS |
| Cycle-to-Cycle Jitter ⁴ | Unloaded outputs | FS=0; @ 5 MHz | | ±200 | pS |
| | | FS=1; @ 15 MHz | | ±125 | |
| Input-to-Output propagation Delay ⁴ | Unloaded outputs with SSEXTR pin OPEN, No load on DLY_CTRL | FS=0; @ 6 MHz | | -75 | pS |
| | | FS=1; @ 12 MHz | | 125 | |
| PLL Lock Time ⁴ | Stable power supply, valid clock presented on CLKIN pin | | | 3 | mS |

Notes: 3. All parameters are specified with 10 pF loaded outputs
 4. Parameter is guaranteed by design and characterization. Not 100% tested in production

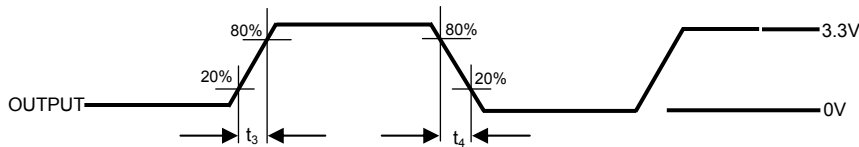
Switching Waveforms

Duty Cycle Timing

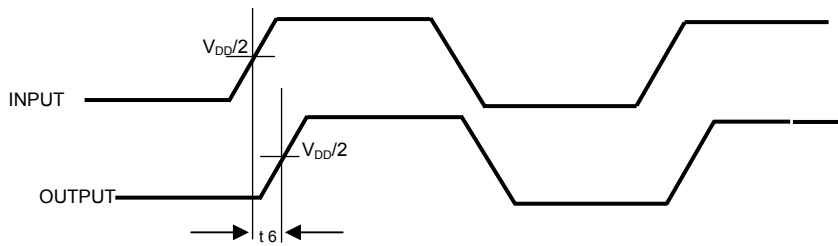
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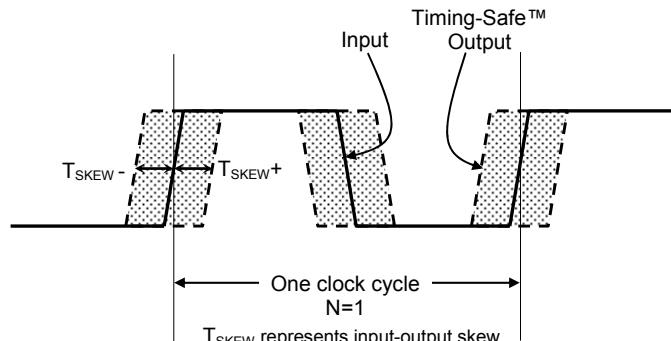
All Outputs Rise/Fall Time



Input - Output Propagation Delay



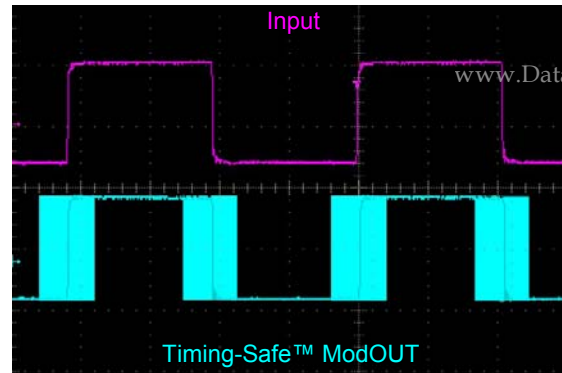
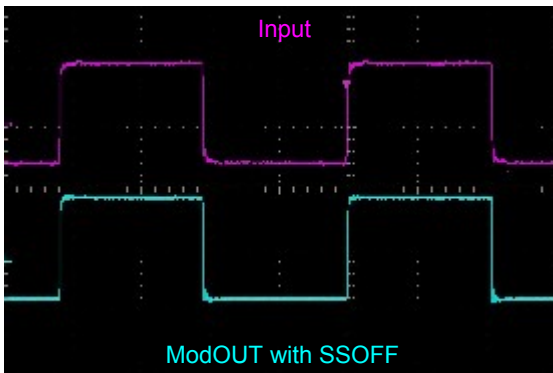
Input-Output Skew



T_{SKEW} represents input-output skew when spread spectrum is ON
 For example, $T_{SKEW} = \pm 0.20$ for an Input clock of 12MHz, translates in to $(1/12MHz) * 0.20 = 16.66nS$

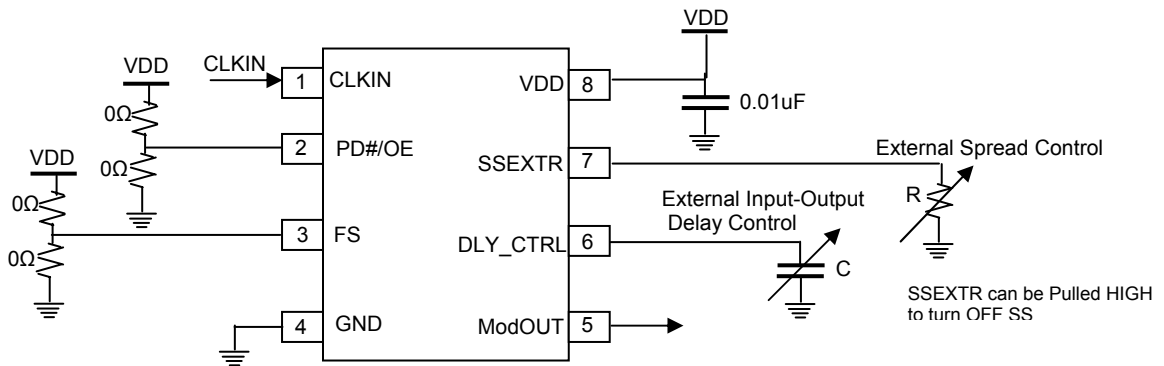
Note: Tskew is measured in units of Clock Period

Typical example of Timing-Safe™ waveform



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Typical Application Schematic



Note: Refer to Pin Description table for Functionality details

Charts (for VDD=2.5V±0.2V and 3.3V±0.3V)

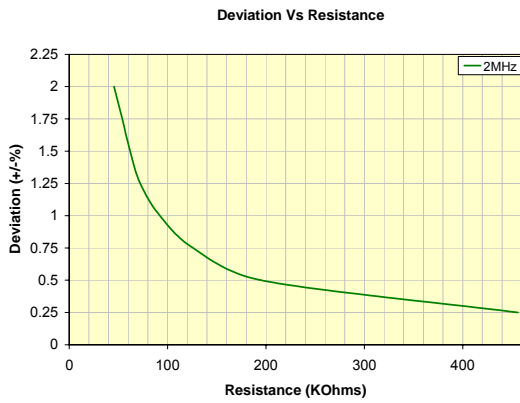


Fig1: Deviation Vs Resistance (2MHz, FS=0)

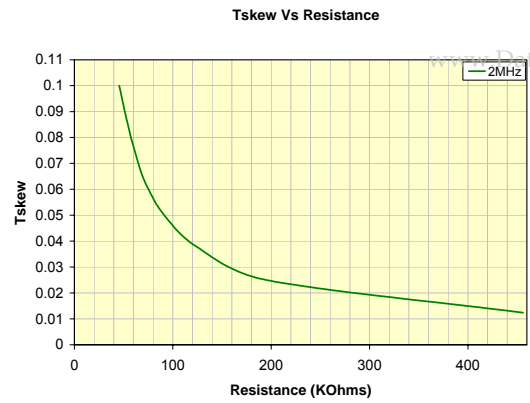


Fig2: Tskew Vs Resistance (2MHz, FS=0)

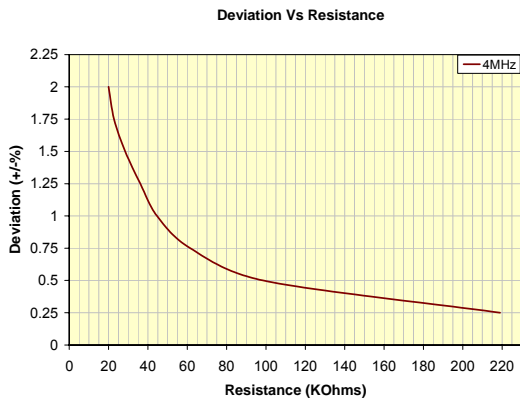


Fig3: Deviation Vs Resistance (4MHz, FS=0)

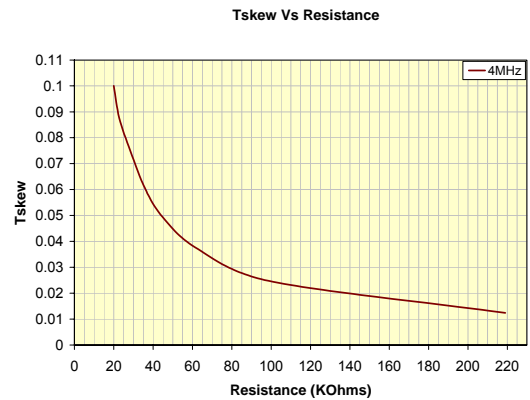


Fig4: Tskew Vs Resistance (4MHz, FS=0)

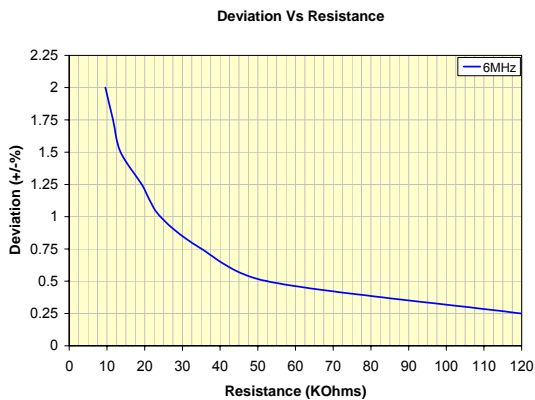


Fig5: Deviation Vs Resistance (6MHz, FS=0)

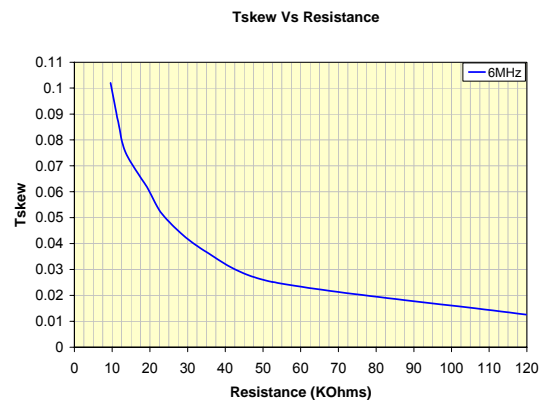


Fig6: Tskew Vs Resistance (6MHz, FS=0)

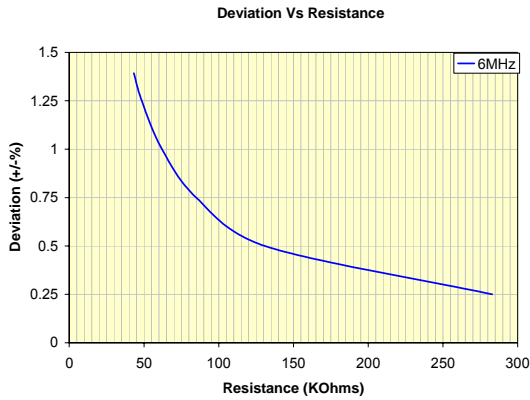


Fig7: Deviation Vs Resistance (6MHz, FS=1)

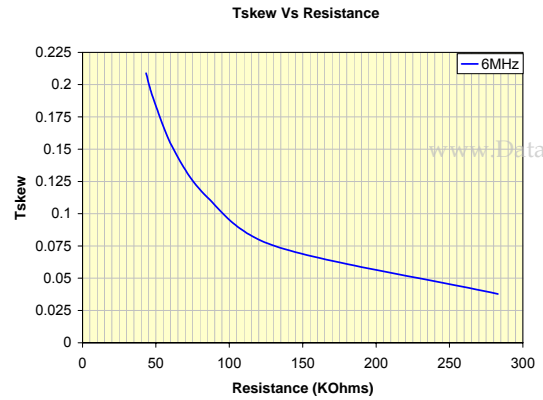


Fig8: Tskew Vs Resistance (6MHz, FS=1)

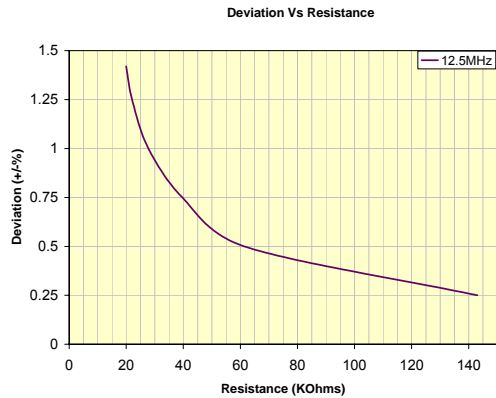


Fig9: Deviation Vs Resistance (12.5MHz, FS=1)

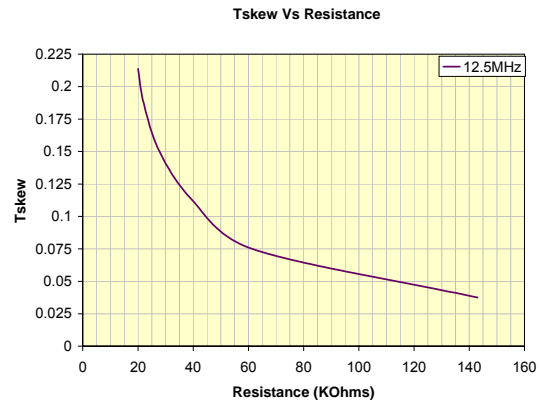


Fig10: Tskew Vs Resistance (12.5MHz, FS=1)

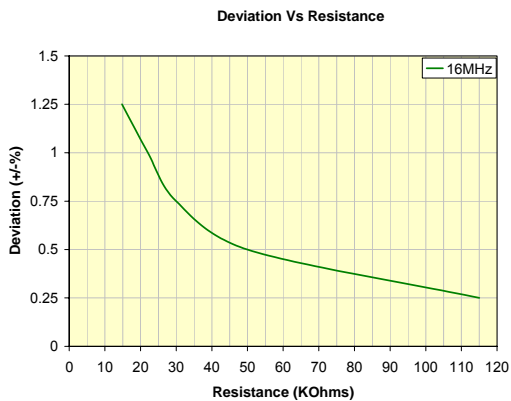
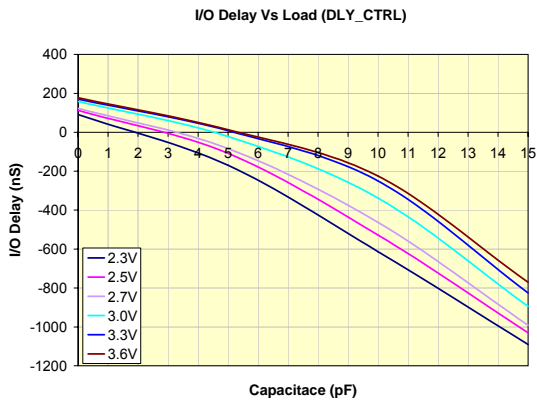


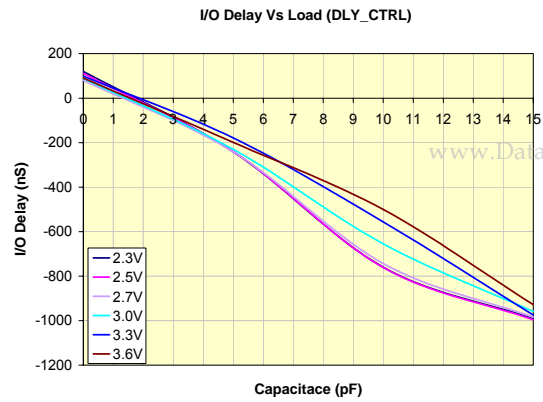
Fig11: Deviation Vs Resistance (16MHz, FS=1)



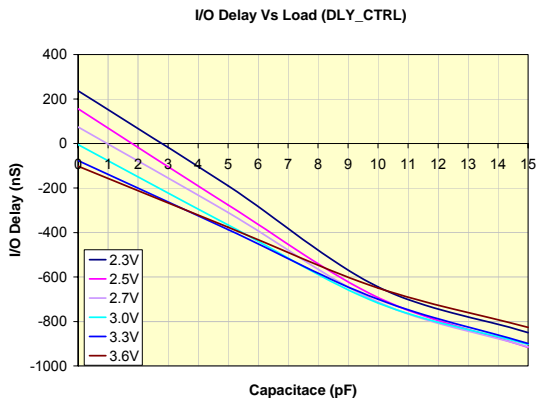
Fig12: Tskew Vs Resistance (16MHz, FS=1)



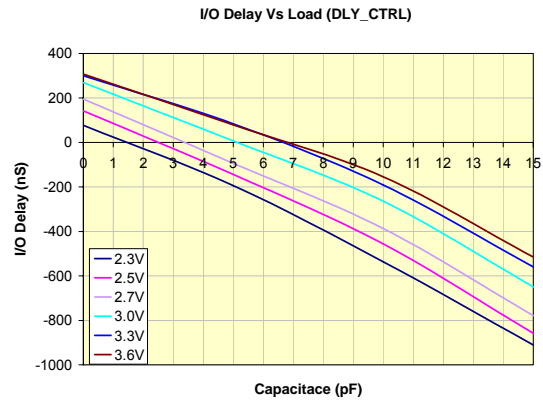
**Fig13: I/O Delay Vs Load (DLY_CTRL)
(For 2MHz, FS=0)**



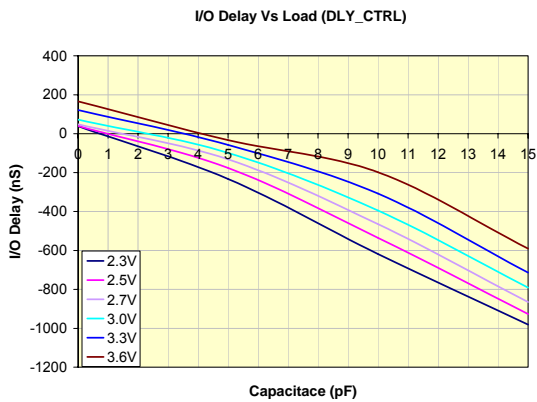
**Fig14: I/O Delay Vs Load (DLY_CTRL)
(For 4MHz, FS=0)**



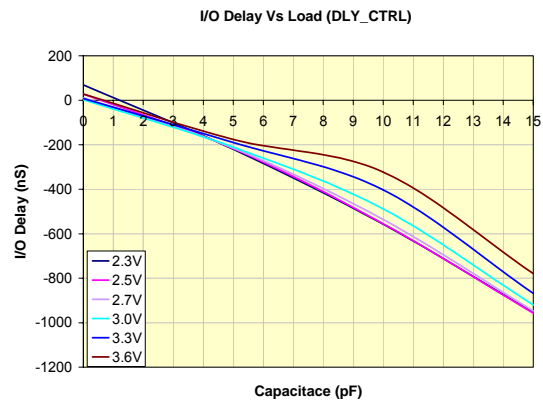
**Fig15: I/O Delay Vs Load (DLY_CTRL)
(For 6MHz, FS=0)**



**Fig16: I/O Delay Vs Load (DLY_CTRL)
(For 6MHz, FS=1)**



**Fig17: I/O Delay Vs Load (DLY_CTRL)
(For 12.5MHz, FS=1)**



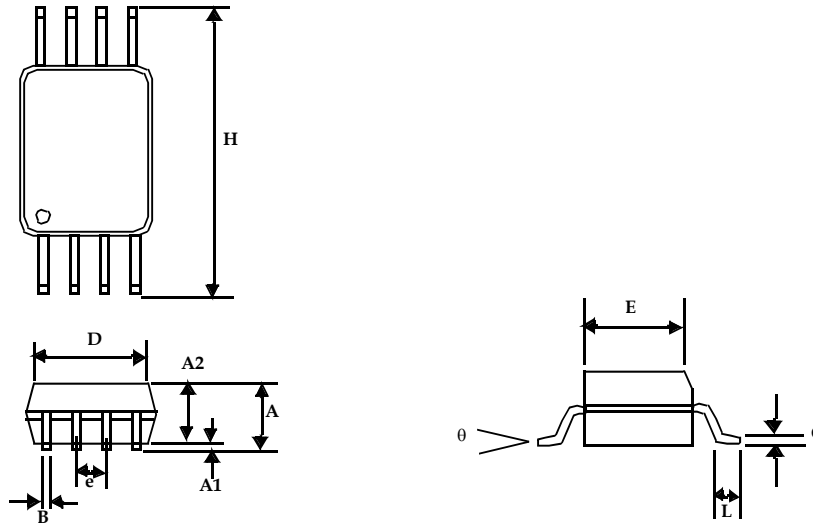
**Fig18: I/O Delay Vs Load (DLY_CTRL)
(For 16MHz, FS=1)**

Note: Device to Device variation of Deviation and I/O delay is $\pm 10\%$

Package Information

8-lead TSSOP Package (4.40-MM Body)

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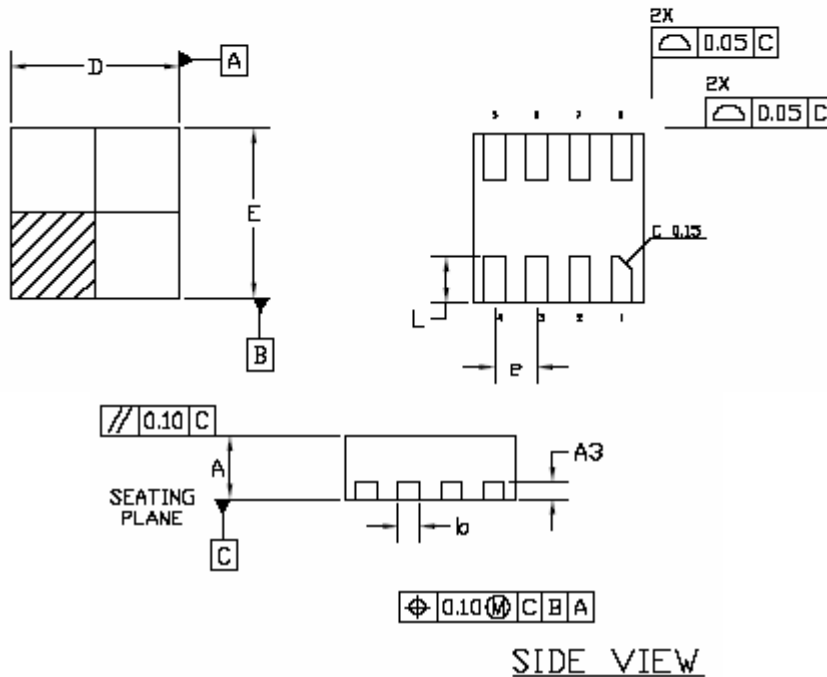
| Symbol | Dimensions | | | |
|--------|------------|-------|-------------|------|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | | 0.043 | | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 |
| A2 | 0.033 | 0.037 | 0.85 | 0.95 |
| B | 0.008 | 0.012 | 0.19 | 0.30 |
| c | 0.004 | 0.008 | 0.09 | 0.20 |
| D | 0.114 | 0.122 | 2.90 | 3.10 |
| E | 0.169 | 0.177 | 4.30 | 4.50 |
| e | 0.026 BSC | | 0.65 BSC | |
| H | 0.252 BSC | | 6.40 BSC | |
| L | 0.020 | 0.028 | 0.50 | 0.70 |
| θ | 0° | 8° | 0° | 8° |

TDFN COL 2x2 8L package Outline drawing

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TOP VIEW

BOTTOM VIEW



| Symbol | Dimensions | | | |
|--------|------------|--------|-------------|------|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | 0.027 | 0.0315 | 0.70 | 0.80 |
| A3 | 0.008 BSC | | 0.203 BSC | |
| b | 0.008 | 0.012 | 0.20 | 0.30 |
| D | 0.079 BSC | | 2.00 BSC | |
| E | 0.078 BSC | | 2.00 BSC | |
| e | 0.020 BSC | | 0.50 BSC | |
| L | 0.020 | 0.024 | 0.50 | 0.60 |

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Ordering Codes

| Ordering Code | Marking | Package Type | Temperature |
|---------------------|------------|---|-------------|
| PCS3P73Z01AWG-08-TT | 3P73Z01AWG | 8-pin 4.4-mm TSSOP - TUBE, Green | Commercial |
| PCS3P73Z01AWG-08-TR | 3P73Z01AWG | 8- pin 4.4-mm TSSOP - TAPE & REEL, Green | Commercial |
| PCS3P73Z01AWG-08-CR | AE1LL | 8- pin 2-mm TDFN COL - TAPE & REEL, Green | Commercial |

LL = 2 Character LOT #

Device Ordering Information

PCS3P73Z01AWG-08-TR

| | | | | | | | | | | | | | | | | | | | | | |
|---|-------------------------------|------------------------------------|------------------------------------|----------------------|-------------------|----------------------|--------------------------|--------------------|---------------------------|--------------|----------|--|-----------|----------|--|---------|----------|--|---------|-----------|--|
| R = Tape & Reel, T = Tube or Tray | | | | | | | | | | | | | | | | | | | | | |
| <table border="0"> <tr> <td>O = TSOT23</td> <td>U = MSOP</td> <td>J=TSOT26</td> </tr> <tr> <td>S = SOIC</td> <td>E = TQFP</td> <td>C=TDFN (2X2) COL</td> </tr> <tr> <td>T = TSSOP</td> <td>L = LQFP</td> <td></td> </tr> <tr> <td>A = SSOP</td> <td>U = MSOP</td> <td></td> </tr> <tr> <td>V = TVSOP</td> <td>P = PDIP</td> <td></td> </tr> <tr> <td>B = BGA</td> <td>D = QSOP</td> <td></td> </tr> <tr> <td>O = OFN</td> <td>X = SC-70</td> <td></td> </tr> </table> | O = TSOT23 | U = MSOP | J=TSOT26 | S = SOIC | E = TQFP | C=TDFN (2X2) COL | T = TSSOP | L = LQFP | | A = SSOP | U = MSOP | | V = TVSOP | P = PDIP | | B = BGA | D = QSOP | | O = OFN | X = SC-70 | |
| O = TSOT23 | U = MSOP | J=TSOT26 | | | | | | | | | | | | | | | | | | | |
| S = SOIC | E = TQFP | C=TDFN (2X2) COL | | | | | | | | | | | | | | | | | | | |
| T = TSSOP | L = LQFP | | | | | | | | | | | | | | | | | | | | |
| A = SSOP | U = MSOP | | | | | | | | | | | | | | | | | | | | |
| V = TVSOP | P = PDIP | | | | | | | | | | | | | | | | | | | | |
| B = BGA | D = QSOP | | | | | | | | | | | | | | | | | | | | |
| O = OFN | X = SC-70 | | | | | | | | | | | | | | | | | | | | |
| DEVICE PIN COUNT | | | | | | | | | | | | | | | | | | | | | |
| F = LEAD FREE AND RoHS COMPLIANT PART G = GREEN PACKAGE, LEAD FREE, and RoHS | | | | | | | | | | | | | | | | | | | | | |
| PART NUMBER | | | | | | | | | | | | | | | | | | | | | |
| <table border="0"> <tr> <td>X= Automotive (-40C to +125C)</td> <td>I= Industrial (-40C to +85C)</td> <td>P or n/c = Commercial (0C to +70C)</td> </tr> </table> | X= Automotive (-40C to +125C) | I= Industrial (-40C to +85C) | P or n/c = Commercial (0C to +70C) | | | | | | | | | | | | | | | | | | |
| X= Automotive (-40C to +125C) | I= Industrial (-40C to +85C) | P or n/c = Commercial (0C to +70C) | | | | | | | | | | | | | | | | | | | |
| <table border="0"> <tr> <td>1 = Reserved</td> <td>6 = Power Management</td> </tr> <tr> <td>2 = Non PLL based</td> <td>7 = Power Management</td> </tr> <tr> <td>3 = EMI Reduction</td> <td>8 = Power Management</td> </tr> <tr> <td>4 = DDR support products</td> <td>9 = Hi Performance</td> </tr> <tr> <td>5 = STD Zero Delay Buffer</td> <td>0 = Reserved</td> </tr> </table> | 1 = Reserved | 6 = Power Management | 2 = Non PLL based | 7 = Power Management | 3 = EMI Reduction | 8 = Power Management | 4 = DDR support products | 9 = Hi Performance | 5 = STD Zero Delay Buffer | 0 = Reserved | | | | | | | | | | | |
| 1 = Reserved | 6 = Power Management | | | | | | | | | | | | | | | | | | | | |
| 2 = Non PLL based | 7 = Power Management | | | | | | | | | | | | | | | | | | | | |
| 3 = EMI Reduction | 8 = Power Management | | | | | | | | | | | | | | | | | | | | |
| 4 = DDR support products | 9 = Hi Performance | | | | | | | | | | | | | | | | | | | | |
| 5 = STD Zero Delay Buffer | 0 = Reserved | | | | | | | | | | | | | | | | | | | | |
| PulseCore Semiconductor Mixed Signal Product | | | | | | | | | | | | | | | | | | | | | |



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Document Version: 0.3

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003
Many PulseCore Semiconductor products are protected by issued patents or by applications for patent

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