Agilent Technologies

Surface Mount RF PIN Switch Diode

Technical Data

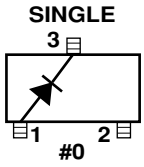
HSMP-3880

Features

- **Diodes Optimized for: Ultra-Low Distortion Switching**
- **Surface Mount SOT-23 Package**
  Tape and Reel Options Available
- **Low Failure in Time (FIT) Rate[1]**
- **Lead-free Option Available**

Note:
1. For more information see the Surface Mount PIN Reliability Data Sheet.

Package Lead Code Identification (Top View)



Description/Applications

The HSMP-3880 switching diode is an ultra low distortion device optimized for higher power applications to 1.5 GHz.

A SPICE model is not available for PIN diodes as SPICE does not provide for a key PIN diode characteristic, carrier lifetime.

Absolute Maximum Ratings[1] T_C = 25°C

Symbol	Parameter	Units	Absolute Maximum
I_f	Forward Current (1 ms Pulse)	Amp	1
P_t	Total Device Dissipation	mW[2]	250
P_{iv}	Peak Inverse Voltage	—	Same as V_{BR}
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. CW Power Dissipation at T_{LEAD} = 25°C. Derate to zero at maximum rated temperature.

Typical Parameters at T_C = 25°C

Part Number HSMP-	Series Resistance R_S (Ω)	Carrier Lifetime τ (ns)	Reverse Recovery Time T_{rr} (ns)	Total Capacitance C_T (pF)
3880	3.8	2500	550	0.30 @ 50 V
Test Conditions	I_F = 1 mA f = 100 MHz	I_F = 50 mA I_R = 250 mA	V_R = 10 V I_F = 20 mA 90% Recovery	

Electrical Specifications T_C = 25°C

Part Number HSMP-	Package Marking Code[1]	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Maximum Total Capacitance C_T (pF)	Maximum Shunt Mode Harmonic Distortion Hmd (dBc)
3880	S0	0	Single	100	6.5	0.40	-55
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10$ µA	I_F = 5 mA f = 100 MHz	V_R = 50 V f = 1 MHz	$2f_o$, Z_o = 50 W f_o = 400 MHz P_{in} = +30 dBm 0 V bias

Note:
1. Package marking code is white.

Typical Parameters at T_C = 25°C (unless otherwise noted), Single Diode

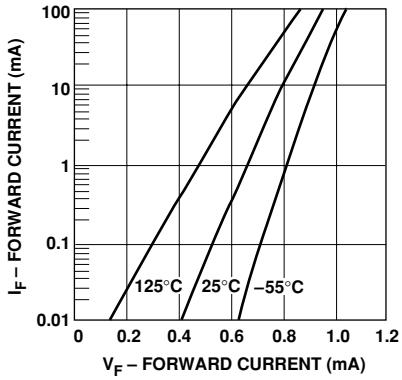


Figure 1. Forward Current vs. Forward Voltage.

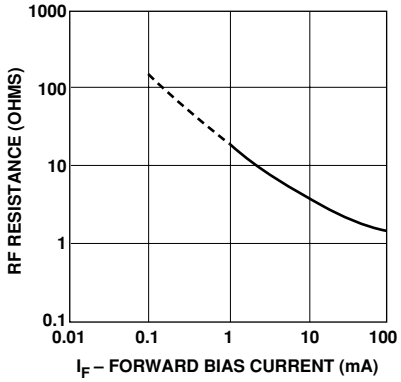


Figure 2. RF Resistance at 25°C vs. Forward Bias Current.

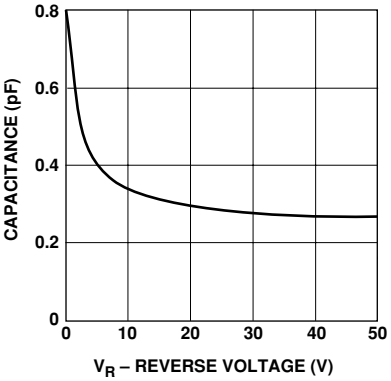


Figure 3. Capacitance vs. Reverse Voltage.

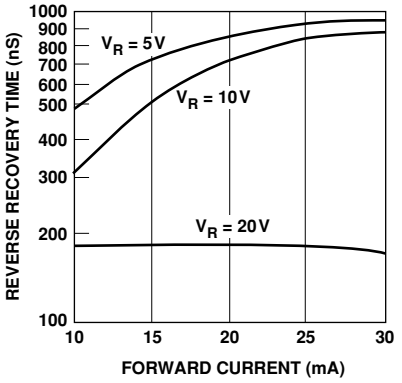


Figure 4. Typical Reverse Recovery Time vs. Reverse Voltage.

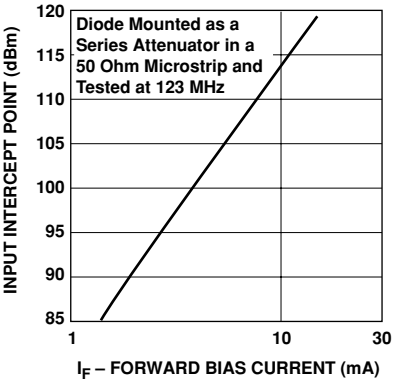
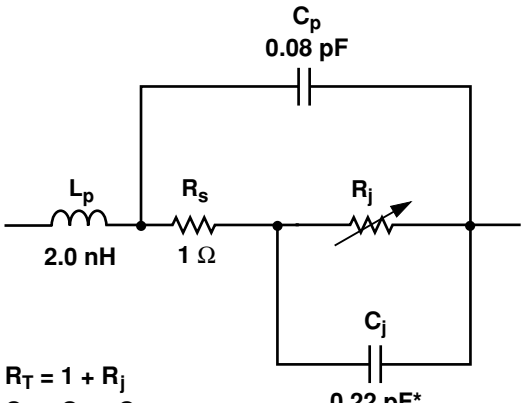


Figure 5. 2nd Harmonic Input Intercept Point vs. Forward Bias Current.

Equivalent Circuit Model

HSMP-3880



$R_T = 1 + R_j$

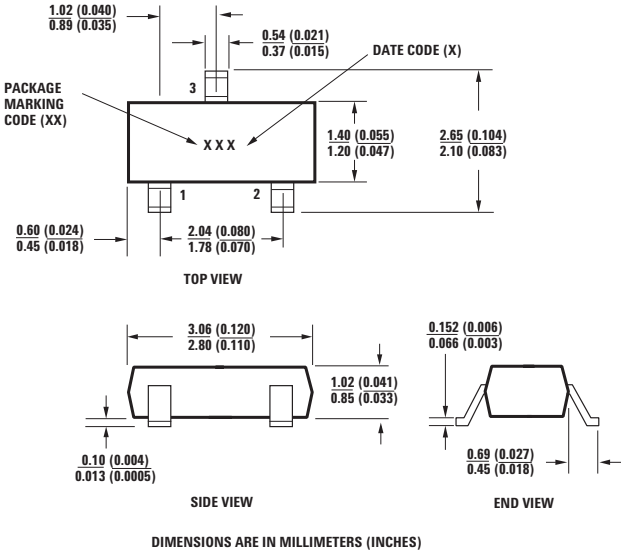
$C_T = C_P + C_j$

$R_j = \frac{49}{I^{0.9}}\ \Omega$

I = Forward Bias Current in mA

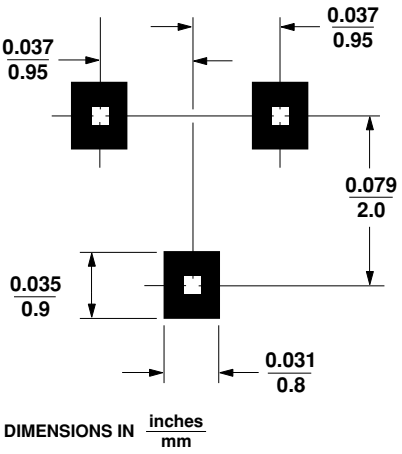
Package Dimensions

Outline 23 (SOT-23)



PC Board Footprints

SOT-23



Package Characteristics

Lead Material ..... Alloy 42
Lead Finish ..... Tin-Lead 85-15%
Maximum Soldering Temperature ..... 260°C for 5 seconds
Minimum Lead Strength ..... 2 pounds pull
Typical Package Inductance ..... 2 nH
Typical Package Capacitance ..... 0.08 pF (opposite leads)

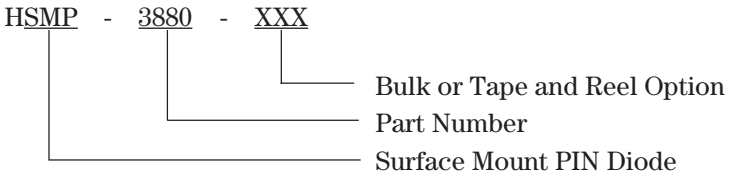
Profile Option Descriptions

-BLK = Bulk
-TR1 = 3K pc. Tape and Reel, Device Orientation; See Figure 6
-TR2 = 10K pc. Tape and Reel, Device Orientation; See Figure 6

Tape and Reeling conforms to Electronic Industries RS-481, “Taping of Surface Mounted Components for Automated Placement.”
For lead-free option, the part number will have the character "G" at the end, e.g., TR2G for a 10K pc lead-free reel.

Ordering Information

Specify part number followed by option under. For example:



Device Orientation
For Outline SOT-23

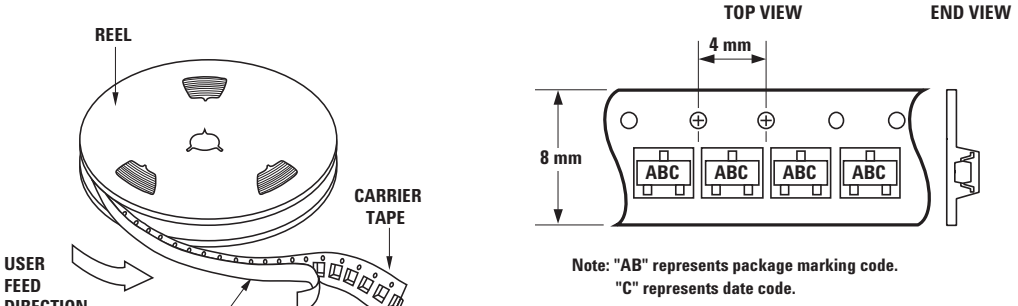
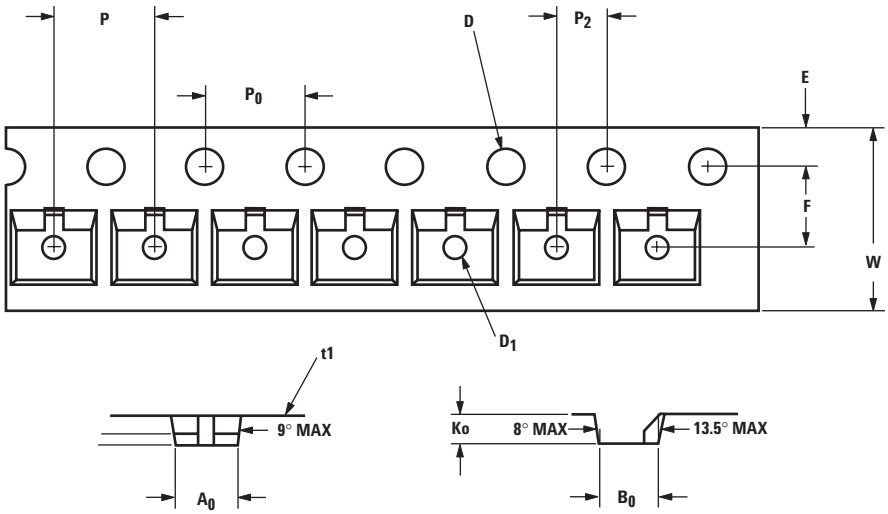


Figure 6. Options -TR1, -TR2 for SOT-23 Package.

Tape Dimensions and Product Orientation
For Outline SOT-23



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.15 ± 0.10	0.124 ± 0.004
	WIDTH	B_0	2.77 ± 0.10	0.109 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.05	0.039 ± 0.002
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 +0.30 –0.10	0.315 +0.012 –0.004
	THICKNESS	t1	0.229 ± 0.013	0.009 ± 0.0005
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

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Data subject to change.

Obsoletes 5968-7702E
March 24, 2004
5988-9924EN