

# AN5192K

Single chip IC with I<sup>2</sup>C bus Interface for PAL/NTSC color TV system

## ■ Overview

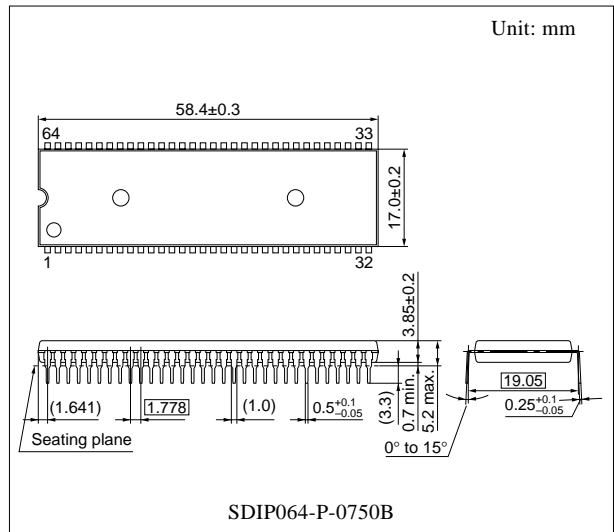
The AN5192K is a single chip IC for PAL/NTSC system color TV. TV for multiple systems can be easily designed by the use of this IC in combination with SECAM demodulation IC (The AN 5637).

## ■ Features

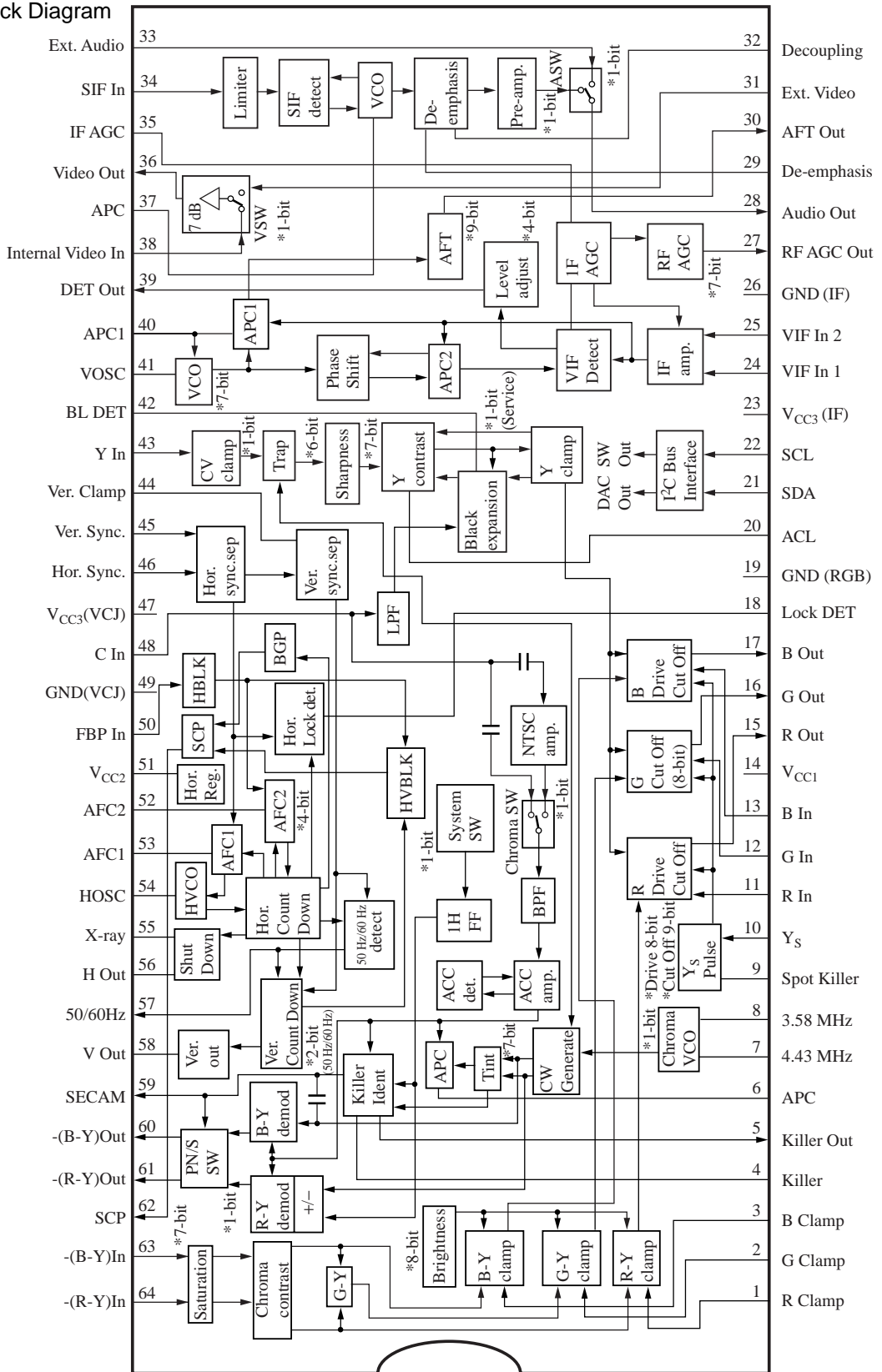
- Free of mechanical adjustment  
Built-in I<sup>2</sup>C bus interface eliminates the need for mechanical adjustment
- Rationalization of external components  
Built-in chroma trap and BPF reduce the external components

## ■ Applications

- TV, TV with VCR



■ Block Diagram



### ■ Pin Description

Pin No.	Description	Pin No.	Description
1	(R-Y) Clamp	33	External Audio Input
2	(G-Y) Clamp	34	SIF Input/DAC Output
3	(B-Y) Clamp	35	IF AGC Filter
4	Killer Filter	36	Video Output
5	Killer Output	37	SIF APC Filter
6	Chroma APC Filter	38	Internal Video Input
7	Chroma VCO (4.43 MHz)	39	VIF Detect Output
8	Chroma VCO (3.58 MHz)	40	VIF APC1 Filter
9	Spot Killer	41	VIF VCO ( $f_p/2$ )
10	Ys Input (Fast blanking)	42	Black Level Det./Blank off SW
11	External R Input	43	Y Input
12	External G Input	44	Ver.Sync.Clamp
13	External B Input	45	Ver.Sync.Input
14	V <sub>CC1</sub>	46	Hor.Sync.Input
15	R Output	47	V <sub>CC3-2</sub> (Chroma/Jungle/DAC)
16	G Output	48	Chroma Input/Black Expansion Start
17	B Output	49	GND (Video/Chroma/Jungle)
18	Hor.Lock Detect	50	FBP Input
19	GND (RGB/I <sup>2</sup> C/DAC)	51	V <sub>CC2</sub> (Hor.Stability Supply)
20	ACL	52	AFC2 Filter
21	SDA	53	AFC1 Filter
22	SCL	54	Hor.VCO (32 f <sub>H</sub> )
23	V <sub>CC3-1</sub> (VIF/SIF)	55	X-ray Protection Input
24	VIF Input 1	56	Hor.Pulse Output
25	VIF Input 2	57	50 Hz/60 Hz Detect Output
26	GND (VIF/SIF)	58	Ver. Pulse Output
27	RF AGC Output	59	SECAM Interface
28	Audio Output	60	-(B-Y) Output
29	De-emphasis	61	-(R-Y) Output
30	AFT Output	62	Sandcastle Pulse Output
31	External Video Input	63	-(B-Y) Input
32	DC Decoupling Filter	64	-(R-Y) Input

### ■ Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
Supply voltage	$V_{CC}$	$V_{CC1}$ (14)	10.5	V
		$V_{CC3}$ (23, 47)	6.0	
Supply current	$I_{CC}$	$I_{14}$	77	mA
		$I_{23+47}$	119	
		$I_{51}$	27	
Power dissipation *2	$P_D$	1 372		mW
Operating ambient temperature *1	$T_{opr}$	-20 to +70		°C
Storage temperature *1	$T_{stg}$	-55 to +150		°C

Note) \*1: Except for the operating ambient temperature and storage temperature, all ratings are for  $T_a = 25^\circ\text{C}$ .

\*2: The power dissipation shown is the value for  $T_a = 70^\circ\text{C}$ .

### ■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	$V_{CC1}$	8.1 to 9.9	V
Supply voltage	$V_{CC3}$	4.5 to 5.5	V
Supply current	$I_{51}$	10 to 25	mA

### ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply (DAC Data are typical)						
Supply current 1	$I_{14}$	Current at $V_{14} = 9\text{ V}$	44	55	66	mA
Supply current 2	$I_{23}$	Current at $V_{23} = 5\text{ V}$	8	11	14	mA
Supply current 3	$I_{47}$	Current at $V_{47} = 5\text{ V}$	56	71	85	mA
Stabilized power supply voltage	$V_{51}$	Voltage at $I_{51} = 15\text{ mA}$	5.8	6.5	7.2	V
Stabilized power supply current	$I_{51}$	Current at $V_{51} = 5\text{ V}$	2	5	7	mA
Stabilized power supply input resistance	$R_{51}$	DC measurement Gradient between $I_{51} = 10\text{ mA}$ and 25 mA	1	5	10	$\Omega$
VIF circuit (Typical input $f_p = 38.9\text{ MHz}$ , $V_{IN} = 90\text{ dB}\mu$ , DAC Data are typical)						
Video detection output (typ.)	$V_{PO}$	Modulation $m = 87.5\%$ Data 0A = 88	1.75	2.1	2.5	V[p-p]
Video detection output (max.)	$V_{POmax}$	Data 0A = F8	2.15	2.6	3.3	V[p-p]
Video detection output (min.)	$V_{POmin}$	Data 0A = 08	1.1	1.6	2.0	V[p-p]
Video detection output f characteristics	$f_{PC}$	Frequency to become -3 dB for 1 MHz	5.5	8	12	MHz
Sync. peak value voltage	$V_{SP}$	Sync. peak voltage in $V_{PO}$ measurement	1.6	2.0	2.4	V
APC pull-in range (high)	$f_{PPH}$	High band side pull-in range (Difference from $f_p = 38.9\text{ MHz}$ )	1.0	2.0	—	MHz

**■ Electrical Characteristics at  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIF circuit (continued) (Typical input $f_p = 38.9$ MHz, $V_{IN} = 90$ dB $\mu$ , DAC Data are typical)						
APC pull-in range (low)	$f_{PPL}$	Low band side pull-in range (Difference from $f_p = 38.9$ MHz)	—	-2.0	-1.0	MHz
RF AGC delay point adjusting range	$\Delta V_{RFDP}$	Input to become delay point ( $V_{27} =$ approx. 6.5 V) at Data 0C = 00 to 7F	75	—	95	dB $\mu$
VCO free-running frequency	$\Delta f_p$	Dispersion without input $V_{IN}$ , $V_{36}$ (IF AGC) = 0 V (Measurement of difference from 38.9 MHz)	-1.2	0	1.2	MHz
RF AGC maximum sink current	$I_{RFmax}$	Maximum current IC can sink when pin 27 is low	1.5	3.0	—	mA
RF AGC minimum sink current	$I_{RFmin}$	IC leakage current at which pin 27 is high	-50	0	50	$\mu\text{A}$
AFT discrimination sensitivity	$\mu_{AFT}$	$Df = \pm 25$ kHz	40	57	75	mV/kHz
AFT center voltage	$V_{AFT}$	$V_{30}$ without input $V_{IN}$	4.0	4.5	5.0	V
AFT maximum output voltage	$V_{AFTmax}$	$V_{30}$ at $f = f_p - 500$ kHz	7.8	8.1	8.7	V
AFT minimum output voltage	$V_{AFTmin}$	$V_{30}$ at $f = f_p + 500$ kHz	0.3	0.8	1.0	V
Detection output resistance	$R_{O39}$	DC measurement	70	120	170	$\Omega$
External mode output DC voltage	$V_{39EXT}$	Output DC voltage in AV SW external mode (04 - D6 = 1)	0.5	1.0	1.8	V
SIF circuit (Typical input $f_s = 6.0$ MHz, $f_M = 400$ Hz, $V_{IN} = 90$ dB $\mu$ )						
Audio detection output (PAL)	$V_{SOP}$	$\Delta f = \pm 50$ kHz 0D - D7 = 0, $R_{237} = 560$ k $\Omega$	480	600	720	mV[rms]
Audio detection output (NTSC/PAL)	$R_{SN/P}$	$\Delta f = \pm 25$ kHz, $R_{237} = 560$ k $\Omega$ 0D - D7 = 1, ratio to PAL	-2.5	-0.5	1.5	dB
Audio detection output linearity	$\Delta V_{SOP}$	Ratio of at $f_s = 6.0$ MHz to 6.5 MHz, and to 5.5 MHz (270 k $\Omega$ addition between pin 37 and $V_{CC1}$ )	-2.5	0	2.5	dB
SIF pull-in range (PAL)	$f_{SPP}$	PAL mode (0D - D7 = 0) pull-in range $R_{237} = 560$ k $\Omega$	5.7	—	6.8	MHz
SIF pull-in range (NTSC)	$f_{SPN}$	NTSC mode (0D - D7 = 1) pull-in range range $R_{237} = 560$ k $\Omega$	4.2	—	4.8	MHz
SIF pull-in range (5.5 MHz)	$f_{SP5.5}$	PAL mode (0D - D7 = 0) 270 k $\Omega$ addition between pin 37 and $V_{CC1}$	5.2	—	5.8	MHz
SIF input resistance	$R_{I34}$	DC measurement	8	10	12	k $\Omega$
De-emphasis pin output resistance (PAL)	$R_{29P}$	Impedance of pin 29 at PAL	32	40	48	k $\Omega$
De-emphasis pin output resistance (NTSC)	$R_{29N}$	Impedance of pin 29 at NTSC	48	60	72	k $\Omega$
AV SW circuit						
Video SW voltage gain	$G_{VSW}$	$f = 1$ MHz, $V_{IN} = 1$ V[p-p]	6.2	7.2	8.2	dB
Video SW f characteristics	$f_{VSW}$	Frequency to become -3 dB from $f = 1$ MHz	10	—	—	MHz

**■ Electrical Characteristics at T<sub>a</sub> = 25°C (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AV SW circuit (continued)						
Video SW external input pin voltage	V <sub>31</sub>	DC measurement	1.7	2.0	2.3	V
Video SW external output DC voltage	V <sub>36E</sub>	DC measurement Data 04 – D6 = 1	4.2	4.8	5.4	V
Video SW external input resistance	R <sub>I31</sub>	DC measurement	44	56	68	kΩ
Video SW output resistance	R <sub>O36</sub>	DC measurement	100	140	180	Ω
Audio SW voltage gain	G <sub>ASW</sub>	Data 04 – D6 = 1 (Outside) f = 400 Hz, V <sub>IN</sub> = 1 V[p-p]	–1	0	1	dB
Audio SW input pin voltage	V <sub>33</sub>	DC measurement	3.7	4.2	4.7	V
Audio SW input output DC voltage	V <sub>28</sub>	DC measurement	3.7	4.2	4.7	V
Audio SW input resistance	R <sub>I31</sub>	DC measurement	61	72	83	kΩ
Audio SW output resistance	R <sub>O28</sub>	DC measurement	200	400	600	Ω
Video SW internal clamp pin voltage	V <sub>38</sub>	DC measurement	1.3	1.6	1.9	V
Video SW internal output DC voltage	V <sub>36I</sub>	DC measurement, Data 04 – D6 = 0	3.1	3.7	4.3	V
Video signal processing circuit (In the following test conditions, the measurements are made with input 0.6 V[p-p] (V <sub>WB</sub> = 0.42 V[0-p]) stair-step, G-out.)						
Video output (typ.)	V <sub>YO</sub>	Data 03 = 40 (typ.) (Contrast)	1.65	2.1	2.55	V[p-p]
Video output (max.)	V <sub>YOmax</sub>	Data 03 = 7F (max.)	3.6	4.5	5.35	V[p-p]
Video output (min.)	V <sub>YOmin</sub>	Data 03 = 00 (min.)	0.07	0.25	0.5	V[p-p]
Contrast variable range	Y <sub>Cmax/min</sub>	03 = 7F 03 = 00	20	25	33	dB
Video frequency characteristics	f <sub>YC</sub>	Data 0E – D1 = 1(Trap Off) Data 04 = 00 (Sharpness) Frequency to become –3 dB from f = 0.2 MHz	5.5	6.8	—	MHz
Picture quality variable range	Y <sub>Smax/min</sub>	04 = 3F      f = 3.8MHz 04 = 00      Data 0E – D1 = 1	9	13	17	dB
Pedestal level (typ.)	V <sub>PED</sub>	Data 02 = 80 (typ.) (Brightness)	1.9	2.5	3.1	V
Pedestal level variable width	ΔV <sub>PED</sub>	Difference between Data 02 = 00 and FF	2.0	2.6	3.2	V
Brightness control sensitivity	ΔV <sub>BRT</sub>	Average amount of change for 1 Step between Data 02 = 60 and A0	7	11	14	mV/Step
Video input clamp voltage	V <sub>YCLP</sub>	Clamp voltage of pin 43	3.2	3.7	4.2	V
ACL sensitivity	ACL	Change of Y-out when V <sub>20</sub> = 3.0 V → 3.5 V	2.1	2.7	3.2	V/V
Blanking Off threshold voltage	V <sub>BOFF</sub>	Maximum blanking Off voltage in lowering pin 42 voltage	0.3	0.5	0.9	V
Blanking level	V <sub>YBL</sub>	DC voltage of blanking pulse	0.5	1.0	1.5	V
DC restoration ratio	T <sub>DC</sub>	APL 10% to 90% $T_{DC} = \frac{\Delta AC - \Delta DC}{\Delta AC} \times 100$	90	100	110	%

**■ Electrical Characteristics at  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Video signal processing circuit (continued) (In the following test conditions, the measurements are made with input: 0.6 V[p-p] ( $V_{WB} = 0.42$ V[0-p] stair-step) at G-out.)						
Video input clamp current	$I_{YCLP}$	DC measurement: IC inside sink current	8	13	18	$\mu\text{A}$
ACL start point	$V_{ACL}$	$V_{20}$ at which output amplitude becomes 90% in decreasing ACL pin ( $V_{20}$ ) from 5 V	3.4	3.7	4.0	V
Color signal processing circuit (In the following test conditions, burst 300 mV[p-p] (PAL) and reference is B-out)						
Color-difference output (typ.)	$V_{CO}$	Input: Color bar Data 00 = 40 (typ.), 03 = 40 (typ.)	2.6	3.3	4.0	V[p-p]
Color-difference output (max.)	$V_{COmax}$	Data 00 = 7F amplitude of one side Data 03 = 40	2.3	3.0	—	V[0-p]
Color-difference output (min.)	$V_{COmin}$	Data 00 = 00 Data 03 = 40	0	—	100	mV[p-p]
Contrast variable range	$C_{Cmax/min}$	03 = FF Data 00 = 40 03 = 00	20	25	33	dB
ACC characteristics 1	ACC1	Burst 300 mV[p-p]→600 mV[p-p] Input; Rainbow	0.9	1.0	1.2	Time
ACC characteristics 2	ACC2	Burst 300 mV[p-p]→60 mV[p-p] Input; Rainbow	0.7	1.0	1.1	Time
NTSC tint center	$\Delta\theta_C$	Difference from Data = 01 = 40 (Tint) at which tint is adjusted to center.	-13	0	+13	Step
NTSC tint variable range 1	$\Delta\theta_1$	Data 01 = 7F	30	50	65	deg
NTSC tint variable range 2	$\Delta\theta_2$	Data 01 = 00	-65	-50	-30	deg
Color-difference output ratio (R)	R/B	Input; Rainbow for both PAL/NTSC	0.71	0.83	0.95	Time
Color-difference output ratio (G)	G/B	Input; Rainbow for both PAL/NTSC	0.31	0.37	0.43	Time
Color-difference output angle (R)	$\angle R$	Input; Rainbow for both PAL/NTSC	78	90	102	deg
Color-difference output angle (G)	$\angle G$	Input; Rainbow for both PAL/NTSC	224	236	248	deg
PAL color killer tolerance	$V_{KillP}$	0 dB = 300 mV[p-p]	-57	-44	-34	dB
NTSC color killer tolerance	$V_{KillN}$	0 dB = 300 mV[p-p]	-57	-44	-34	dB
APC pull-in range (high)	$f_{CPH}$	For both PAL/NTSC	450	900	—	Hz
APC pull-in range (low)	$f_{CPL}$	For both PAL/NTSC	—	-900	-450	Hz
Color killer detection output voltage (Color)	$V_{KC}$	$V_5$ measured when chroma is input	4.5	5.0	—	V
Color killer detection output voltage (B&W)	$V_{KBW}$	$V_5$ measured when no chroma is input	0	0.1	0.5	V
Demodulation output-(B-Y)	$V_{DB}$	Input; Color bar, measurement by pin 60	555	695	835	mV[p-p]
Demodulation output-(R-Y)	$V_{DR}$	Input; Color bar, measurement by pin 61	430	540	650	mV[p-p]
Demodulation output angle $\angle B$	$\angle_{RDB}$	Phase shift of B-Y axis	-5	0	5	deg

**■ Electrical Characteristics at  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color signal processing circuit (continued) (In the following test conditions, burst 300 mV <sub>[p-p]</sub> (PAL) and reference is B-out)						
Demodulation output angle $\angle R$	$\angle_{RDR}$	Phase difference from B-Y axis	85	90	95	deg
CW output level (4.43 MHz)	$V_{CWP}$	AC component when $V_{CO}$ is set at 4.43 MHz	250	300	350	mV <sub>[p-p]</sub>
CW output level (3.58 MHz)	$V_{CWN}$	AC component when $V_{CO}$ is set at 3.58 MHz	—	0	50	mV <sub>[p-p]</sub>
CW output level period (SECAM)	$T_{CW}$	CW output period at SECAM	1.31	1.41	1.51	ms
SECAM discrimination current	$I_{SECAM}$	Minimum value for taking out current from pin 59 and discriminating as SECAM	50	100	150	$\mu\text{A}$
PAL/NTSC DC level	$V_{59PN}$	$V_{59}$ DC level at PAL/SECAM	0.8	1.3	1.65	V
SECAM DC level	$V_{59S}$	$V_{59}$ DC level at SECAM	4.1	4.6	5.1	V
PAL/NTSC output impedance	$R_{60,61PN}$	DC measurement. pin 60, 61 impedance at PAL/NTSC	390	480	570	$\Omega$
SECAM output impedance	$R_{60,61S}$	DC measurement. pin 60, 61 impedance at SECAM	100	—	—	k $\Omega$
RGB Processing Circuit (DAC Data are typical)						
Pedestal difference voltage	$\Delta V_{IPL}$	Difference voltage of R,G,B out pedestal	0	—	0.3	V
Brightness voltage tracking	$\Delta T_{BL}$	R, G, B out fluctuation level ratio of DATA 02 (Brightness) 02 = 40 to C0	0.9	1.0	1.1	Time
Video voltage gain relative ratio	$\Delta G_{YC}$	Output ratio of R,B out to G out	0.8	1.0	1.2	Time
Video voltage gain tracking	$\Delta T_{CONT}$	Gain ratio of R, G, B out of Data 03 (Contrast) 03 = 20 to 60	0.9	1.0	1.1	Time/ Time
Drive adjustment range	$G_{DV}$	AC change amount of R, B out between drive adjustment max. and min.	5.3	6.3	7.3	dB
Cut-off adjustment range	$V_{CUT-OFF}$	DC change amount of R, G, B out between cutoff adjustment at max. and min.	1.9	2.2	2.5	V
$Y_S$ threshold voltage	$V_{YS}$	Minimum DC voltage, when $Y_S$ turns on	0.7	1.0	1.3	V
External RGB pedestal voltage	$V_{EPL}$	$Y_S$ is On	1.7	2.3	2.9	V
External RGB pedestal difference voltage	$\Delta V_{EPL}$	$Y_S$ is On	0	—	250	mV
Internal and external pedestal difference voltage	$\Delta V_{PL/IE}$	Internal-external	50	200	400	mV
External RGB output voltage	$V_{ERGB}$	Input 3 V <sub>[p-p]</sub> , contrast 03 = 7F	4.3	5.4	6.5	V <sub>[p-p]</sub>
External RGB output difference voltage	$\Delta V_{ERGB}$	Input 3 V <sub>[p-p]</sub> , contrast 03 = 7F	-0.6	0	0.6	V
External RGB contrast variable range	$E_{Cmax/min}$	03 = 7F 03 = 00	10	13	16	dB
External RGB frequency characteristics	$f_{RGBC}$	Input 0.2 V <sub>[p-p]</sub> , DC = 1 V	8	12	—	MHz



**■ Electrical Characteristics at  $T_a = 25^\circ\text{C}$  (continued)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Synchronizing signal processing circuit</b>						
Horizontal free-running oscillation frequency	$f_{\text{HO}}$	Without sync. signal input	15.33	15.63	15.93	kHz
Horizontal output pulse duty cycle	$\tau_{\text{HO}}$	Upward going pulse duty cycle	31	37	43	%
Horizontal pull-in range	$f_{\text{HP}}$	Difference from $f_{\text{H}} = 15.625$ kHz	$\pm 500$	$\pm 650$	—	Hz
PAL vertical free-running oscillation frequency	$f_{\text{VO-P}}$	Data 0E – D2 = 1, D3 = 0 Forced 50 Hz mode, no sync. signal input	48	50	52	Hz
NTSC vertical free-running oscillation frequency	$f_{\text{VO-N}}$	Data 0E – D2 = 1, D3 = 1 Forced 60 Hz mode, no sync. signal input	58	60	62	Hz
Vertical output pulse width	$\tau_{\text{VO}}$	For both PAL/NTSC	9	10	11	$1/f_{\text{H}}$
PAL vertical pull-in range	$f_{\text{VP-P}}$	$f_{\text{H}} = 15.625$ kHz, forced 50 Hz mode	46	—	54	Hz
NTSC vertical pull-in range	$f_{\text{VP-N}}$	$f_{\text{H}} = 15.75$ kHz, forced 60 Hz mode	56	—	64	Hz
Horizontal output voltage (high)	$V_{56\text{H}}$	High level DC voltage	3.2	3.5	3.8	V
Horizontal output voltage (low)	$V_{56\text{L}}$	Low level DC voltage	0	—	0.3	V
Vertical output voltage (high)	$V_{58\text{H}}$	High level DC voltage	3.9	4.2	4.5	V
Vertical output voltage (low)	$V_{58\text{L}}$	Low level DC voltage	0	—	0.3	V
Picture center variable range	$\Delta T_{\text{HC}}$	Change amount of phase difference between H Sync. and H-out of Data 0A = 80 to 8F	2.6	3.2	4.4	$\mu\text{S}$
Overvoltage protective operation voltage	$V_{\text{XRAY}}$	Pin 55 minimum voltage at which H-out stops to appear	0.60	0.68	0.76	V
Vertical frequency discrimination (50)	$f_{50}$	Vertical frequency to become $V_{57}$ = Low (< 0.5 V)	47	—	55	Hz
Vertical frequency discrimination (60)	$f_{60}$	Vertical frequency to become $V_{57}$ = High (> 4.5 V)	57	—	63	Hz
Sync. signal clamp voltage (Ver.)	$V_{45}$	Clamp voltage of $V_{45}$	1.0	1.3	1.6	V
Sync. signal clamp voltage (Hor.)	$V_{46}$	Clamp voltage of $V_{46}$	1.0	1.3	1.6	V
Horizontal output start voltage	$V_{\text{fHS}}$	Minimum $V_{50}$ to become $f_0 > 10$ kHz, when horizontal oscillation output is 1 V[p-p] or more.	3.4	4.2	5.0	V
<b>I<sup>2</sup>C interface</b>						
Sink current when ACK	$I_{\text{ACK}}$	Maximum value of pin 21 sink current at ACK	2.0	2.5	5.0	mA
SCL, SDA signal input high level	$V_{\text{IHI}}$		3.1	—	5.0	V
SCL, SDA signal input low level	$V_{\text{ILO}}$		0	—	0.9	V
Maximum frequency allowable to input	$f_{\text{Imax}}$		100	—	—	Kbit/s

## ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

### • Design reference data

Note) The characteristic listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIF circuit (Typical input $f_p = 38.9$ MHz, $V_{IN} = 90$ dB $\mu$ )						
Input sensitivity	$V_{PS}$	Input level to become $V_{PO} = -3$ dB	—	45	51	dB $\mu$
Maximum allowable input	$V_{Pmax}$	Input level to become $V_{PO} = 1$ dB	104	110	—	dB $\mu$
SN ratio	$SN_P$		50	53	—	dB
Differential gain	$DG_P$		0	3	5	%
Differential phase	$DP_P$		0	3	5	deg
Black noise detection level	$\Delta V_{BN}$	Deference from sync. peak value	-55	-45	-35	IRE
Black noise clamp level	$\Delta V_{BNC}$	Deference from sync. peak value	35	45	35	IRE
RF AGC operation sensitivity	$G_{RF}$	Input level difference to become $V_{27} = 1$ V $\rightarrow$ 7 V	0.5	1.5	3.0	dB
VCO switch On drift	$\Delta f_{PD}$	Frequency drift from 5 seconds to 5 mins. after SW On	100	150	200	kHz
Intermodulation	IM	$V_{IC} - V_{IP} = -2$ dB, $V_{IS} - V_{IP} = -12$ dB	46	52	—	dB
RF AGC adjustment sensitivity	$S_{RF}$	Average amount of change of output voltage $V_{27}$ at Data 1Step	1.0	1.7	2.5	V/Step
AFT offset adjustment sensitivity	$S_{AFT}$	Average amount of change of output voltage $V_{30}$ per Data 1Step	0.15	0.2	0.25	V/Step
Video detection output fluctuation with $V_{CC}$	$\Delta V_{P/V}$	$V_{CC} = \pm 10\%$	—	$\pm 10$	$\pm 15$	%
Video detection output-temperature characteristics	$\Delta V_{P/T}$	$T_a = -10^\circ\text{C}$ to $+70^\circ\text{C}$	—	$\pm 5$	$\pm 10$	%
Input resistance (pin 24, 25)	$R_{I24, 25}$	$f = 38.9$ MHz	—	1.2	—	k $\Omega$
Input capacitance (pin 24, 25)	$C_{I24, 25}$	$f = 38.9$ MHz	—	4.0	—	pF
Sound IF output level	$V_{SIF}$	$f_s = 38.9$ MHz - 6.0 MHz, P/S = 20 dB	94	100	106	dB $\mu$
VCO control sensitivity	$\beta_P$	$\Delta V_{41} = \pm 0.1$ V	2.0	2.7	3.5	kHz/mV
VCO control range	$f_{VCO}$	Free-running frequency change width from Data 0D = 00 to 7F	3.0	4.0	5.0	MHz
RF AGC delay-point temperature characteristics	$\Delta V_{DP/T}$	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$	0	3	5	dB
VCO free-running frequency temperature characteristics	$\Delta f_{P/T}$	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$	—	300	—	kHz
AFT center frequency temperature characteristics	$\Delta f_{AFT/T}$	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$ , input frequency at which AFT output voltage becomes 4.5 V	—	300	—	kHz

## ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

### • Design reference data (continued)

Note) The characteristic listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SIF circuit (Typical input $f_s = 6.0\text{ MHz}$ , $f_M = 400\text{ Hz}$ , $V_{IN} = 90\text{ dB}\mu$ )						
Input limiting level	$V_{LIM}$	Input level to become $V_{SOP} = -3\text{ dB}$	—	44	50	$\text{dB}\mu$
AM rejection ratio	AMR	AM = 30%	60	70	—	dB
Total harmonic distortion	THD	$\Delta f = \pm 50\text{ kHz}$	0	0.3	0.5	%
SN ratio	$SN_A$		50	55	—	dB
Audio output with $V_{CC}$ fluctuation	$\Delta V_{S/V}$	$V_{CC} = \pm 10\%$	—	$\pm 3$	$\pm 6$	%
Audio output-temperature characteristics	$\Delta V_{S/T}$	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$	—	$\pm 5$	$\pm 10$	%
AV SW circuit						
Video SW cross-talk	$CT_{VSW}$	$f = 1\text{ MHz}$ , $V_{IN} = 1\text{ V[p-p]}$ Internal→External, External→Internal	—	-66	-60	dB
Audio SW cross-talk (Internal→External)	$CT_{AIE}$	$f_s = 6.0\text{ MHz}$ , $f_M = 400\text{ Hz}$ Without input from outside	—	-73	-67	dB
Audio SW cross-talk (External→Internal)	$CT_{AEI}$	$f_s = 6.0\text{ MHz}$ , $f_M = 0\text{ Hz}$ $f_M = 400\text{ Hz}$ , $V_{IN} = 600\text{ mV[rms]}$	—	-73	-67	dB
Video signal processing circuit (In the following test conditions, the measurements are made at G-out with input $0.6\text{ V[p-p]}$ ( $V_{WB} = 0.42\text{ V[0-p]}$ .) )						
Y signal delay time	$T_{DL}$	Phase difference from Y input (PAL: 4.43 MHz)	620	690	790	ns
Black level extension1	$V_{BL1}$	Input: Total black, difference between pin 42 of 9 V and Open (With RC filter)	-100	0	100	mV
Black level extension2	$V_{BL2}$	Input: Total black, difference between pin 42 of 3 V and 9 V	500	800	1100	mV
Black level extension3	$V_{BL3}$	Input: approx. 20IRE, voltage difference between pin 42 of Open and 9 V	100	300	500	mV
Contrast variation with sharpness	$\Delta V_{CS}$	Y-out output level difference between sharpness max. and min.	-300	0	300	mV
Brightness variation with sharpness	$\Delta V_{BS}$	Pedestal level DC difference between sharpness is at max. and min.	-250	0	250	mV
Input dynamic range	$V_{I_{max}}$	Contrast 03 = 40	1.0	1.7	—	$\text{V[p-p]}$
Y signal SN ratio	$SN_Y$	Contrast 03 = 7F	51	56	—	dB
Black level extension start point	$V_{BLS}$	Start point at $V_{48} = 4.5\text{ V}$	37	42	47	IRE
Trap on/off gain difference	$\Delta G_{TRAP}$	Trap on/off	-1	0	1	dB
Trap on/off delay time change amount	$\Delta T_{TRAP}$	Trap on/off	350	390	430	ns

## ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

### • Design reference data (continued)

Note) The characteristic listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Video signal processing circuit (continued) (In the following test conditions, the measurements are made at G-out with input 0.6 V[p-p] ( $V_{WB} = 0.42$ V[0-p]).						
Trap frequency error	$\Delta f_{TRAP}$	Trap center frequency, when chroma input is 4.43 MHz	-70	0	70	kHz
Trap attenuation amount	$A_{TT TRAP}$	Attenuation amount of 4.43 MHz, when chroma input is 4.43 MHz	26	30	—	dB
Trap automatic adjustment range	$f_{TRAP}$	VCO frequency of $\Delta f_{TRAP} \leq 70$ kHz	3	—	5	MHz
Trap fixed frequency	$f_{ST}$	Data 0E – D6 = 1, Trap frequency	4.0	4.8	5.6	MHz
Video output fluctuation with $V_{CC}$	$\Delta V_{Y/V}$	$V_{CC1} = 9$ V (allowance: $\pm 10\%$ )	0	100	200	mV/V
Video output-temperature characteristics	$\Delta V_{Y/T}$	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$	0	5	10	%
PAL/NTSC delay time difference	$\Delta T_{P/N}$	Trap On (NTSC-PAL)	-10	10	30	ns
Color signal processing circuit (Burst 300 mV[p-p] (PAL), reference is B-out)						
Demodulation output residual carrier	$V_{CAR1}$	$2f_{SC}$ level of pin 60 and 61	0	—	30	mV
Color difference output residual carrier	$V_{CAR2}$	$2f_{SC}$ level of pin 15, 16, and 17	0	—	50	mV
VCO free-running frequency (PAL)	$f_{CP}$	Difference from $f = 4.433619$ MHz	-300	0	300	Hz
VCO free-running frequency (NTSC)	$f_{CN}$	Difference from $f = 3.579545$ MHz	-300	0	300	Hz
$f_{CO}$ fluctuation with $V_{CC}$	$\Delta V_{C/V}$	$V_{CC1} = 9$ V (allowance: $\pm 10\%$ ), $V_{CC3} = 5$ V (allowance: $\pm 10\%$ )	-300	0	300	Hz
Static phase error (PAL)	$\Delta \theta_P$	Tint shift from $\Delta f_C = -300$ Hz to $+300$ Hz change	0	2	5	deg/ 100 Hz
Static phase error (NTSC)	$\Delta \theta_N$	Tint shift from $\Delta f_C = -300$ Hz to $+300$ Hz change	0	2	5	deg/ 100 Hz
PAL/NTSC	$R_{P/N}$	Output amplitude ratio of PAL to NTSC	0.8	1.0	1.2	Time
Line crawling	$\Delta V_{PAL}$	Pin 61: Output amplitude difference per 1H for-(R-Y) pin	0	—	50	mV
Color difference output bandwidth	$f_{CC}$	Band to become -3 dB	—	1.0	—	MHz
Chroma BPF characteristics (PAL)	$BPF_P$	Output level difference between $f = 4.43$ MHz and 3.58 MHz	—	10	—	dB
Chroma BPF characteristics (NTSC)	$BPF_N$	Output level difference between $f = 3.58$ MHz and 2.0 MHz (when Ext. video)	—	13	—	dB
Color-difference output fluctuation with $V_{CC}$	$\Delta V_{C/V}$	$V_{CC1} = 9$ V (allowance: $\pm 10\%$ ) $V_{CC3} = 5$ V (allowance: $\pm 10\%$ )	—	$\pm 10$	$\pm 15$	%
Color-difference output -temperature characteristics	$\Delta V_{C/T}$	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$	—	$\pm 10$	$\pm 15$	%

## ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

### • Design reference data (continued)

Note) The characteristic listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color signal processing circuit (continued) (Burst 300 mV[p-p] (PAL), reference is B-out)						
Brightness variation with color	$V_{BC}$	Pedestal level DC difference between at contrast max. and min.	-250	0	250	mV
Brightness variation difference voltage with color	$\Delta V_{BC}$	R, G, B out variation voltage difference	0	—	20	mV
RGB processing circuit						
(C-Y)/Y	$R_{CY}$	Color bar input, B-out Contrast typ., color Data 00 = 60	0.9	1.2	1.5	V[0-p]/ V[p-p]
(C-Y), Y delay difference	$\Delta T_{CY}$	Color bar input, B-out Phase of green→magenta	-100	0	100	ns
$Y_S$ changeover speed	$f_{YS}$	$f_{YS}$ , when external input is 3 V, output level -3 dB	7	11	—	MHz
External RGB input dynamic range	$V_{DEXT}$	Contrast max., Data 03 = 77F	2.0	2.5	3.2	V[0-p]
Internal/external crosstalk	$CT_{RGB}$	Leakage when $f = 1$ MHz, 1 V[p-p], and $Y_S = 5$ V	—	-60	-50	dB
Spot killer operation	$V_{SPK}$	$V_9$ , when $V_9$ is decreased from 9 V and spot killer turns on.	7.4	7.8	8.2	V
Brightness variation with contrast	$V_{BAC}$	Pedestal level DC difference between contrast max. and min.	-250	0	250	mV
Brightness variation difference voltage with contrast	$\Delta V_{BAC}$	R, G, B out variation voltage difference	0	—	20	mV
Pedestal level fluctuation with $V_{CC}$	$\Delta V_{PL/V}$	$V_{CC1} = 9$ V (allowance: $\pm 10\%$ )	0	200	400	mV/V
Pedestal level- temperature characteristics	$\Delta V_{PL/T}$	$T_a = -20^\circ\text{C}$ to $+70^\circ\text{C}$	-2.6	-2.2	-1.8	mV/ $^\circ\text{C}$
Pedestal level 2	$V_{PD2}$	Pedestal level, when G cutoff Data 05 = 18	2.1	2.7	3.3	V
Synchronizing signal processing circuit						
Lock detection output voltage	$V_{LD}$	$V_{18}$ at horizontal AFC lock	5.7	6.3	6.9	V
Lock detection charge and discharge current	$I_{LD}$	DC measurement	$\pm 0.6$	$\pm 0.8$	$\pm 1.1$	mA
EBP (RGB) slice level	$V_{FBP}$	Minimum voltage of pin 50, when blanking is applied to RGB output	0.4	0.75	1.1	V
EBP (AFC2) slice level	$V_{FBPH}$	Minimum voltage of pin 50 at which AFC2 operates	1.5	1.9	2.3	V
Horizontal AFC $\mu$	$\mu_H$	DC measurement	30	37	44	$\mu\text{A}/\mu\text{s}$
Horizontal VCO $\beta$	$\beta_H$	$\beta$ curve gradient near $f = 15.7\text{kHz}$	1.4	1.9	2.4	Hz/mV
Burst gate pulse position	$P_{BGP}$	For both PAL/NTSC, delay from H. Sync. rise	0.2	0.4	0.6	$\mu\text{s}$

## ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

### • Design reference data (continued)

Note) The characteristic listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Synchronizing signal processing circuit (continued)						
PAL burst gate pulse width	$W_{BGPP}$		3.4	4.0	4.6	$\mu\text{s}$
NTSC burst gate pulse width	$W_{BGPN}$		2.5	3.0	3.5	$\mu\text{s}$
Burst gate pulse output voltage	$V_{BGP}$	DC voltage of pin 62 in BGP period	4.5	4.7	4.9	V
H blanking pulse output voltage	$V_{HBLK}$	DC voltage in H-blanking pulse period of pin 62	2.1	2.4	2.7	V
V blanking pulse output voltage	$V_{VBLK}$	DC voltage in V-blanking pulse period of pin 62	2.1	2.4	2.7	V
PAL V blanking pulse width	$W_{VP}$	Pulse width at $f_H = 15.625\text{ kHz}$	1.31	1.41	1.51	ms
NTSC blanking pulse width	$W_{VN}$	Pulse width at $f_H = 15.73\text{ kHz}$	1.01	1.11	1.21	ms
FBP allowable range	$T_{FBP}$	Time from H-out rise to FBP center	12	—	19	$\mu\text{s}$
I <sup>2</sup> C interface						
Bus free before start	$t_{BUF}$		4.0	—	—	$\mu\text{s}$
Start condition set-up time	$t_{SU,STA}$		4.0	—	—	$\mu\text{s}$
Start condition hold time	$t_{HD,STA}$		4.0	—	—	$\mu\text{s}$
Low period SCL, SDA	$t_{LOW}$		4.0	—	—	$\mu\text{s}$
High period SCL	$t_{HIGH}$		4.0	—	—	$\mu\text{s}$
Rise time SCL, SDA	$t_r$		—	—	1.0	$\mu\text{s}$
Fall time SCL, SDA	$t_f$		—	—	0.35	$\mu\text{s}$
Data set-up time (write)	$t_{SU,DAT}$		0.25	—	—	$\mu\text{s}$
Data hold time (write)	$t_{HD,DAT}$		0	—	—	$\mu\text{s}$
Acknowledge set-up time	$t_{SU,ACK}$		—	—	3.5	$\mu\text{s}$
Acknowledge hold time	$t_{HD,ACK}$		0	—	—	$\mu\text{s}$
Stop condition set-up time	$t_{SU,STO}$		4.0	—	—	$\mu\text{s}$
DAC						
4, 6, 7bit DAC DNLE	$L_{4,6,7}$	$1\text{LSB} = \{\text{Data (max.)} - \text{Data (00)}\} / 15,63,127$	0.1	1.0	1.9	$\frac{\text{LSB}}{\text{Step}}$
8bit DAC DNLE	$L_8$	$1\text{LSB} = \{\text{Data (FF)} - \text{Data (00)}\} / 255$	0.1	1.0	1.9	$\frac{\text{LSB}}{\text{Step}}$
Cut off DAC overlap	$\Delta\text{Step}$	Overlap of 8-bit 2-stage changeover (Same for AFT) of R, B cut-off	27	32	37	Step

## ■ Electrical Characteristics at $T_a = 25^\circ\text{C}$ (continued)

### • Typical conditions when testing

#### 1. Input signal

- 1) VIF :  $f_p = 38.9\text{ MHz}$ ,  $V_{IN} = 90\text{ dB}\mu$   
Video modulation: modulated signal is 10-staircase. Modulation  $m = 87.5\%$   
 $V_{IN} = 90\text{ dB}\mu$ , pin 25 input level approx.  $84\text{ dB}\mu$
- 2) SIF :  $f_s = 6.0\text{ MHz}$ ,  $V_{IN} = 90\text{ dB}\mu$ , modulated signal  $f_M = 400\text{ Hz}$ , Deviation: PAL  $\pm 50\text{ kHz}$ ,  
NTSC  $\pm 25\text{ kHz}$
- 3) Video : 10-staircase  $0.6\text{ V[p-p]}$  ( $V_{BW} = 0.42\text{ V[0-p]}$ )
- 4) Chroma : Color bar signal: Burst level  $300\text{ mV[p-p]}$   
: Rainbow signal : Burst level  $300\text{ mV[p-p]}$
- 5) Sync. signal : Video signal  $1.5\text{V[p-p]}$  to  $2.5\text{ V[p-p]}$  for both horizontal and vertical sync. signal input

#### 2. I<sup>2</sup>C BUS conditions: (PAL)

Sub Address	Data(H)
00	40
01	40
02	80
03	40
04	80
05	00
06	00
07	00
08	80
09	80
0A	88
0B	01
0C	40
0D	40
0E	01

Control	Data(H)
Color	00 = 40
Tint	01 = 40
Brightness	02 = 80
Contrast	03 = 40
Sharpness	04 = 00
Cut-off R, B	05, 07 = 00
Cut-off G	06 = 00
Drive R, B	08, 09 = 80
Video output	0A (Upper rank) = 8*
Picture center position	0A (Lower rank) = *8
AFT	0B = 01 04 - D7 = 1
RF AGC	0C = 40
VIF VCO	0D = 40

■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	I/O
1 2 3		<p>Pin 1: Color difference signal clamp pin (R-Y)</p> <p>Pin 2: Color difference signal clamp pin (G-Y)</p> <p>Pin 3: Color difference signal clamp pin (B-Y)</p> <ul style="list-style-type: none"> <li>Color difference signal inputted from pin 63, 64 is clamped according to brightness control voltage.</li> <li>Clamp pulse uses internal clamp pulse (BGP)</li> </ul>	DC approx. 7 V
4		<p>Killer filter pin</p> <ul style="list-style-type: none"> <li>Filter pin for killer detection circuit (operates for BGP period)</li> <li>Killer turned On (Without color output) 2.8 V or less</li> </ul>	DC approx. 3.3 V
5		<p>Killer output pin</p> <ul style="list-style-type: none"> <li>Output pin of killer detection circuit</li> <li>Connect 33 kΩ load resistor of pin 5 to microcomputer V<sub>CC</sub></li> </ul>	DC Killer On 0.2 V Killer Off 5 V
6		<p>Pin for APC filter</p> <ul style="list-style-type: none"> <li>Filter pin for APC detection circuit (operates for BGP period)</li> <li>Detection sensitivity becomes large when external R→large (Tends to pull-in easily. Tends to be affected by noise)</li> </ul> <p>β curve</p> <p>• When SECAM, APC circuit is stopped by short circuiting 40 kΩ resistor</p>	DC approx. 2.5 V



■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
7 8		<p>Pin 7: Chroma oscillation pin (4.43 MHz) Pin 8: Chroma oscillation pin (3.58 MHz)</p> <ul style="list-style-type: none"> <li>• Oscillation pin for chroma. Either one of 4.43 MHz or 3.58 MHz is oscillated</li> <li>• Oscillation frequency changeover is performed by 0E – D0 bit of I<sub>2</sub>C Bus</li> <li>• When 0E – D0 = 1 I<sub>P1</sub> and I<sub>P2</sub> turn On and 4.43 MHz oscillates. When 0E – D0 = 0 I<sub>N1</sub> and I<sub>N2</sub> turn on and 3.58 MHz oscillates.</li> <li>• Pattern from pin to oscillator element should be as short as possible.</li> </ul>	<p>AC f = f<sub>C</sub> approx. 0.3 V[p-p]</p>
9		<p>Spot killer pin</p> <ul style="list-style-type: none"> <li>• To be used for discharging electric charge on CRT quickly when power of set is turned Off.</li> <li>• DC voltage of R,G,B output pin is raised when V<sub>CC1</sub> drops.</li> </ul>	<p>DC approx. 9 V</p>
10		<p>Y<sub>S</sub> input pin</p> <ul style="list-style-type: none"> <li>• Fast blanking pulse input pin for OSD</li> <li>• Turns on at a voltage higher than 1 V[0-p]</li> </ul>	<p>AC (pulse)</p>
11 12 13		<p>Pin 11: External R input pin Pin 12: External G input pin Pin 13: External B input pin</p> <ul style="list-style-type: none"> <li>• External input pin for OSD</li> <li>• Output changes linearly according to input level.</li> </ul> <ul style="list-style-type: none"> <li>• Limit voltage of input changes according to contrast control level.</li> </ul>	<p>AC (pulse)</p>

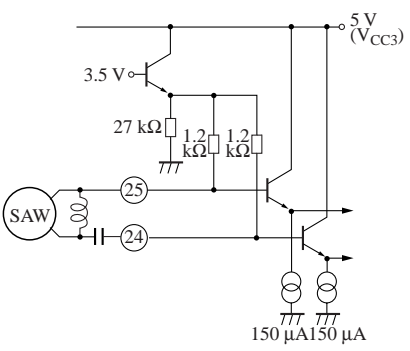
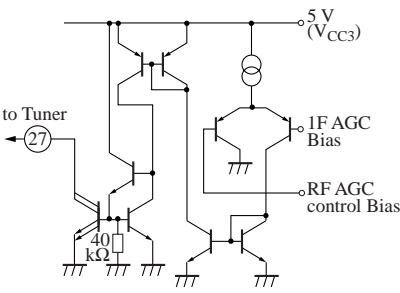
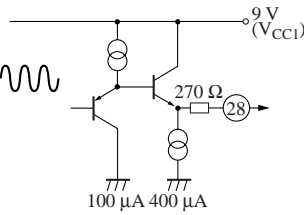
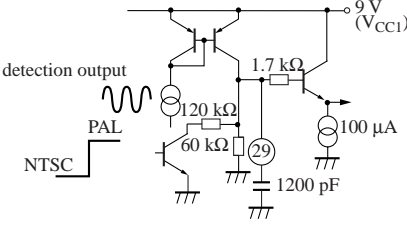
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
14		<p><math>V_{CC1}</math> (typ. 9 V)</p> <ul style="list-style-type: none"> <li>• Output part of VIF and SIF circuit</li> <li>• AV SW circuit</li> <li>• Video circuit</li> <li>• RGB circuit</li> </ul>	<p>DC</p> <p>9 V</p>
15 16 17		<p>Pin15: R-out pin Pin16: G-out pin Pin17: B-out pin</p> <ul style="list-style-type: none"> <li>• BLK level approx. 0.9 V</li> <li>• Black (Pedestal) level approx. 2.2 V</li> <li>• Blanking can be released when pin 42 (Black level detection pin) is set at 0 V.</li> </ul>	<p>AC</p>
18		<p>Horizontal sync. detection pin</p> <ul style="list-style-type: none"> <li>• Phase of horizontal synchronizing signal and horizontal output pulse is detected and outputted.</li> <li>• Pin18 is low when out of phase.</li> <li>• In asynchronous state, color control becomes min. and chroma output disappears.</li> <li>• Pay attention to impedance when the voltage of pin 18 is utilized for microcomputer (<math>Z_O \geq 1 M\Omega</math> is required)</li> </ul> <p> </p> <ul style="list-style-type: none"> <li>• H Sync. period When pin 56 is high: <math>I_1</math> On When pin 56 is low: <math>I_2</math> On</li> </ul>	<p>DC</p> <p>when synchronous <math>V_{CC2} - V_{SAT}</math> when asynchronous approx. 0.3 V</p>
19		<p>GND</p> <ul style="list-style-type: none"> <li>• RGB circuit</li> <li>• DAC I<sup>2</sup>C circuit</li> <li>• VIF (VCO) circuit</li> </ul>	

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
20		<p>ACL pin</p> <ul style="list-style-type: none"> <li>Contrast can be reduced when DC voltage of pin 20 is decreased from the outside.</li> </ul>	<p>DC approx. 3 V</p>
21		<p>I<sup>2</sup>C Bus Data input pin</p>	<p>AC (pulse)</p>
22		<p>I<sup>2</sup>C Clock input pin</p>	<p>AC (pulse)</p>
23		<p>V<sub>CC3-1</sub> (typ. 5 V) • For VIF, SIF circuit</p>	<p>DC 5 V</p>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
24 25		<p>Pin 24: VIF input pin 1 Pin 25: VIF input pin 2</p> <ul style="list-style-type: none"> <li>• Input for VIF amp. and balanced input</li> <li>• Input max. 120 dBμ</li> </ul>	<p>AC f = f<sub>p</sub> DC level approx. 2.7 V</p>
26		<p>GND</p> <ul style="list-style-type: none"> <li>• VIF, SIF circuit</li> </ul>	DC
27		<p>RF AGC output pin</p> <ul style="list-style-type: none"> <li>• Collector open output</li> </ul>	DC
28		<p>Audio output pin</p> <ul style="list-style-type: none"> <li>• There is fluctuation of DC due to internal and external changeover</li> </ul>	<p>AC 0 kHz to 20 kHz DC approx. 4.2 V</p>
29		<p>De-emphasis pin</p> <ul style="list-style-type: none"> <li>• De-emphasis filter pin for sound detection signal.</li> <li>• External C is the same for PAL and NTSC (Internal impedance changes)</li> <li>• PAL: 120 kΩ//60 kΩ × 1 200 pF = 48 μs</li> <li>• NTSC: 60 kΩ × 1200 pF = 72 μs</li> </ul>	<p>AC 0 kHz to 20 kHz</p>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
30		<p>AFT output pin</p> <ul style="list-style-type: none"> <li>Center voltage offset should be adjusted by using a bus.</li> <li>AFT defeat SW is turned on (0B = 00), <math>V_{30}</math> becomes a value determined by the value of externally attached resistor-divider.</li> <li>AFT <math>\mu</math> is variable by impedance of externally attached resistor.</li> </ul>	DC
31		<p>External video input pin</p> <ul style="list-style-type: none"> <li>Input pin for external video signal. DC cut input.</li> <li>Typical 1 V[p-p] (max. 1.5 V[p-p])</li> </ul>	<p>AC 1 V[p-p] (Composite)</p> <p>DC approx. 2.1 V</p>
32		<p>Decoupling pin</p> <ul style="list-style-type: none"> <li>S curve inside IC is wide band but DC feedback is applied so that DC voltage of output signal becomes constant.</li> <li>DC level (typ. 4.5 V) <math>f_S \rightarrow</math>High: <math>V_{32} \rightarrow</math>Low</li> </ul>	DC
33		<p>External audio input pin</p> <ul style="list-style-type: none"> <li>Input pin for external audio signal input. DC cut input.</li> <li>Typical input level should be adjusted to internal sound level.</li> <li>Input max. 7 V[p-p]</li> </ul>	<p>AC 0 kHz to 20 kHz</p>

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
34		<p>SIF Signal input Input max. 110 dBμ</p>	<p>AC <math>f = f_s</math> DC approx. 2.3 V</p>
35		<p>IF AGC filter pin</p> <ul style="list-style-type: none"> <li>Pin for IF AGC filter. The current obtained from peak AGC circuit is smoothed by external capacitor.</li> <li>Since response becomes faster when <math>C \rightarrow</math> small, but sag tends to appear easily.</li> </ul>	<p>DC approx. 2 V</p>
36		<p>Video output pin</p> <ul style="list-style-type: none"> <li>Int. video or Ext. video signal selected by AV SW is outputted.</li> <li>DC fluctuates by internal/external changeover</li> </ul>	<p>AC 2 V[p-p]</p> <p>DC level approx. 4.5 V</p>
37		<p>SIF APC filter pin</p> <ul style="list-style-type: none"> <li>Filter pin for APC circuit of SIF</li> <li>Recommended resistance value for single frequency (R237: Connect between the pin and <math>V_{CC1}</math>)</li> </ul> <p>6.5 MHz: Open 6.0 MHz: 560 kΩ 5.5 MHz: 200 kΩ 4.5 MHz: 560 kΩ</p>	<p>DC approx. 2.5 V</p>

Application Circuit Example

