JMF616

ARM Base SATAII to Flash Controller

Overview

JMF616 is a single chip, supports external SDRAM, SATA II to NAND flash interface. It is native design to provide higher bandwidth for flash memory access.

JMF616 can support the maximum read and write speed to drive the limit of flash memory. JMF616 has the best supporting to the latest NAND flash memory, including Samsung, Toshiba, Hynix, Micron and IM Flash. It also provides the embedded hardware error correction code (ECC), wear leveling, and bad block management technology in this chip. In order to resolve compatibility issue, JMF616 provides the on line firmware upgrade ability.

JMF616 provides embedded processor, internal masked ROM, data SRAM, SATA link/transport layer, SATA PHY. Data swap between different interfaces can be done very efficiency by DMA without CPU involvement. Based on the efficient architecture, the JMF616 can provide the best performance.

Features

Compliance

- Compliant with Universal Serial Bus Specification Revision 2.0.
- Compliant with Serial ATA International Organization: Serial ATA Revision 2.6.

SATA I/II

- Supports 1-port 1.5/3.0Gbps SATA I/II interface.

CPU

- Embedded data buffer.
- 32bits Embedded processor.
- 32Kbytes Embedded masked program ROM.
- 128Kbytes Embedded system RAM.

FLASH

- Support maximum 16CE’s flash per channel.
- Support 5x/4x/3x/2x nm Flash
- Enhanced endurance by dynamic/static wear-leveling.
- Support 4K/8K bytes page size.

- Support dynamic power management.
- SMART (Self-Monitoring, Analysis and Reporting Technology).
- Data integrity under power-cycling.
- Support online SATA firmware update.
- Supports 8 bits Flash interface.
- Supports BCH 16/24 bits ECC.

SDRAM

- Support DDR/DDR2
- Support 128Mbits to 2Gbits.

SYSTEM

- Integrated 1-SATA II port and 8-channels Flash controller.
- LED indicator for SATA read/write access.
- LED indicator for SATA PHY link up.
- Provides 14 GPIO pins for customer.
- Provides UART and JTAG for S/W debugging.
- Built-in power-up self-test (BIST).
- Manual and automatic self-diagnostics.
- 281-ball TFBGA package.

Firmware

- Support NCQ on this controller.
- Support LBA24 & LBA48 on this controller.
- Support 1 to 8 banks selected free.
- Support 2 to 8 channels selected free.

Block Diagram

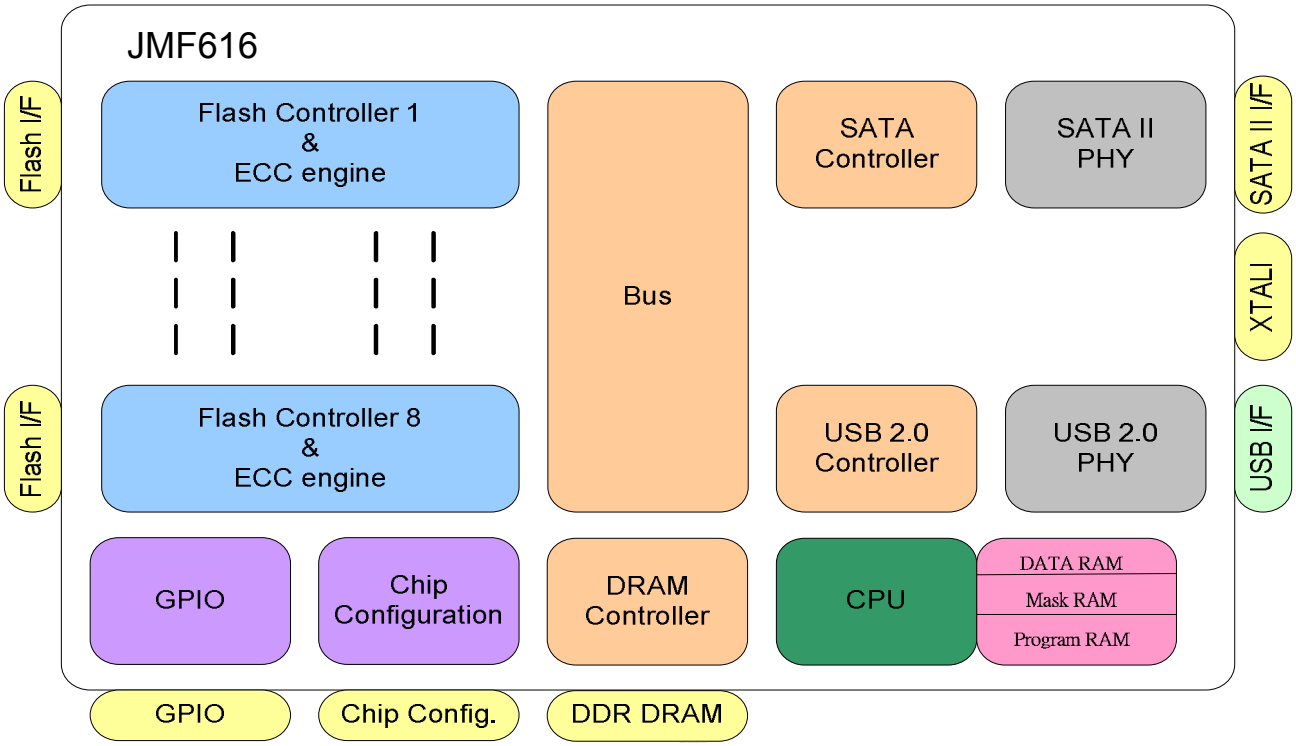

Figure 1: JMF616 Block Diagram

Total capacity

density/per flash	Support CE pins/per flash	maximum flash number	Total capacity
1G x 8 Bits (8Gb)	1 CE pin	32	32G Bytes
2G x 8 Bits (16Gb)	1 CE/ 2 CE pin	32	64G Bytes
4G x 8 Bits (32Gb)	1 CE/ 2 CE pin	32	128G Bytes
8G x 8 Bits (64Gb)	2 CE pin	32	256G Bytes
16G x 8 Bits (128Gb)	4 CE pin	32	512G Bytes

Table 1: JMF616 Total capacity table

Product Information

Name	Description
JMF616	ARM Base SATA-II to Flash Controller

Document

1	JMF616 Data Sheet
2	JMF616 Specification
3	JMF616 Hardware Design Guide
4	JMF616 Hardware Sehcmatic

Contact Information

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