JMF616 SATA II SSD Controller

Overview

JMF616 supports external SDRAM, SATA Generation 2 interface to NAND interface. It is native design SSD controller to provide outstanding performance.

JMF616 can support the maximum read and write speed to drive the limit of flash memory. JMF616 has the best supporting to the latest NAND flash memory, including Samsung, Toshiba, Hynix, Micron and IM Flash. It also provides the embedded hardware error correction code (ECC), wear leveling, and bad block management technology in this chip. In order to resolve compatibility issue, JMF616 provides the on line firmware upgrade ability.

MF616 uses chip internal hardware accelerator to offload CPU loading and increase performance. In tradition, CPU need look up mapping table and set physical row address command to NAND flash. Currently, the hardware engine of JMF616 can help CPU read mapping table and depend on different flash type, send correct command to NAND flash. For example, two plan read, two plan program, copyback and cache mode. JMF616 can check NAND flash status to start next command sequence. CPU only need set hardware register to control hardware behavior.

JMF616 provides embedded processor, internal masked ROM, data SRAM, SATA link/transport layer, SATA PHY. Data swap between different interfaces can be done very efficiency by DMA without CPU involvement. Based on the efficient architecture, the JMF616 can provide the best performance.

Features

Compliance

- Compliant with Universal Serial Bus Specification Revision 2.0.
- Compliant with USB Mass Storage Class specification version 1.0.
- Compliant with Serial ATA International Organization: Serial ATA Revision 2.6.

SATAI\II

- Supports 1-port 1.5/3.0Gbps SATA I/II interface.

CPU

- Embedded data buffer.
- 32bits Embedded processor.
- 32 KBytes Embedded masked program ROM.
- 128 KBytes Embedded system RAM.

Flash

- Support maximum 16CE’s Flash per channel.
- Support 5x/4x/3x nm Flash.

- Enhanced endurance by dynamic/static wear-leveling.
- Supports 4K/8K bytes page size.
- Supports dynamic power management.
- SMART (Self-Monitoring, Analysis and Reporting Technology).
- Data integrity under power-cycling.
- Supports online SATA/USB firmware update.
- Supports 8 bits Flash interface.
- Supports BCH 16/24 bits ECC.

SDRAM

- Supports DDR/DDR2
- Support 128Mbits to 2Gbits

SYSTEM

- Integrated 1-USB2.0 port, 1-SATA II port and 8-channels Flash controller.
- LED indicator for USB2.0 and SATA read/write access.
- LED indicator for USB2.0 and SATA PHY link up.
- Provides 14 GPIO pins for customer.
- Provides UART and JTAG for S/W debugging.
- Built-in power-up self-test (BIST).
- Manual and automatic self-diagnostics.
- 281-ball TFBGA package

Firmware

- Support NCQ on this controller.
- Support LBA24 & LBA48 on this controller.
- Support 1 to 8 banks selected free.
- Support 2 to 8 channels selected free.

Block Diagram

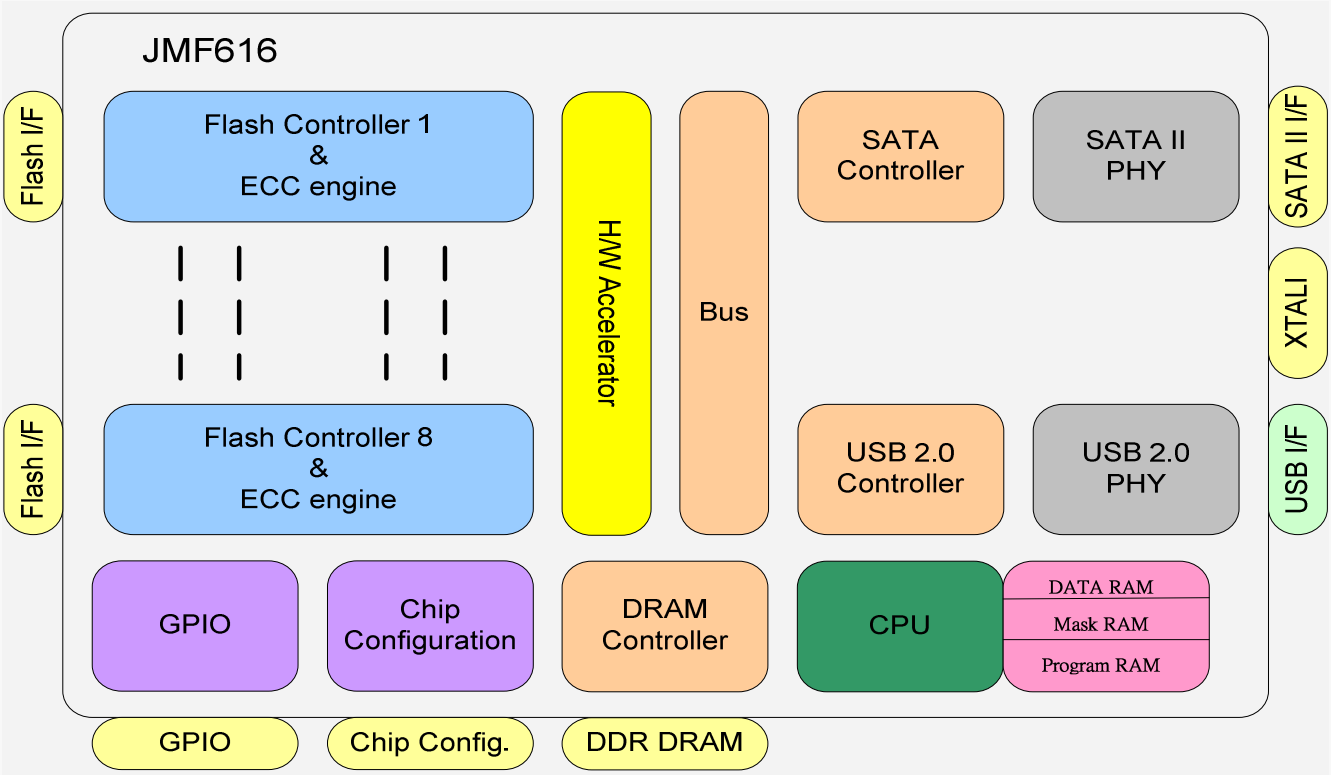

Figure 1 *Block diagram of JMF616*