

# HA12240FP

## Bus Interface Driver/Receiver IC

REJ03F0095-0100Z

Rev.1.0

Dec.01.2003

### Description

The HA12240FP is developed to be used as a bus interface driver/receiver IC in automotive audio equipment controllers. It implements a two-wire serial bus.

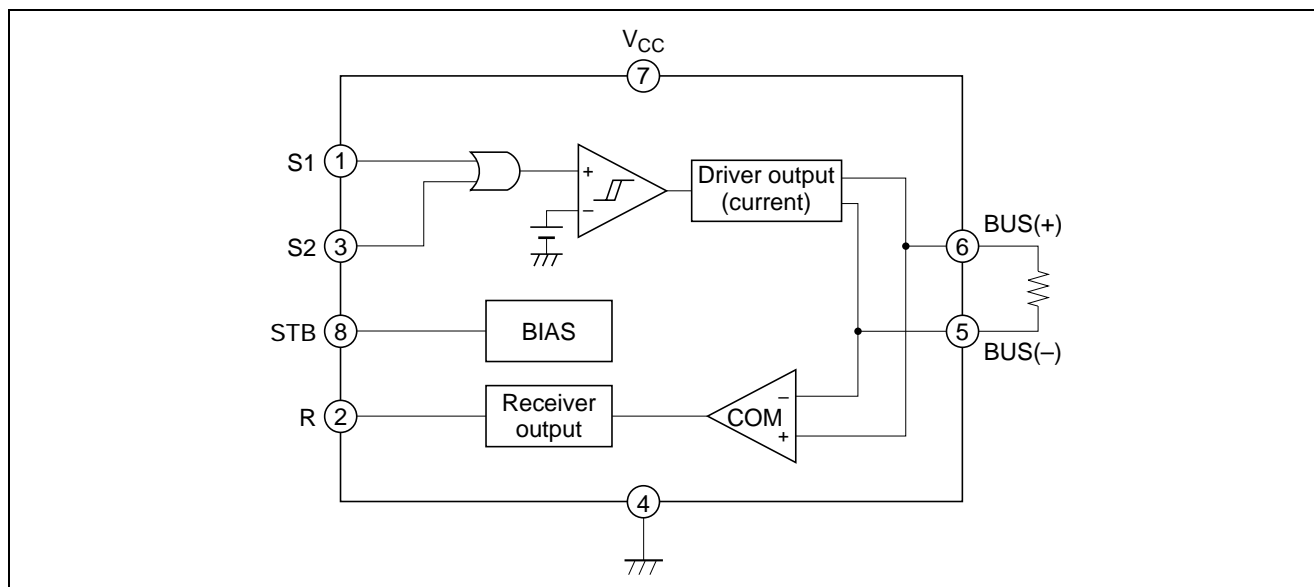
### Functions

- Two-input OR circuit
- Input comparator circuit (3.3 V and 5.0 V available)
- Current output driver circuit
- Receiver input comparator circuit
- Receiver output circuit (Open-collector output)
- Standby circuit

### Features

- Supports two data inputs (Pins 1 and 3 are the input pins)
- Comparators with hysteresis characteristics are adopted for the inputs (3.3 V and 5.0 V available)
- Current drive output drivers adopted (Output current: 3.8 mA typical)
- Comparators with hysteresis characteristics are adopted for the receivers
- Wide receiver common-mode input operating range (Common-mode input operating range: 0 to 5 V typical)
- The driver output /the receiver input (pins 5 and 6) can withstand high voltages (Maximum ratings of 18 V)
- Standby functions (standby mode when pin 8 becomes low level)
- Operating power-supply voltage range of  $5\text{ V} \pm 0.5\text{ V}$

### Block Diagram



Pin Functions

Pin No.	Symbol	Function	Equivalent Circuit
1	S1	Data input pin 1	
2	R	Receiver output pin	
3	S2	Data input pin 2	
4	GND	GND pin	
5	BUS(-)	Bus output (-), Receiver input (-) pin	
6	BUS(+)	Bus output (+), Receiver input (+) pin	
7	V <sub>CC</sub>	Power supply pin	
8	STB	Standby input pin (Lo: ON, Hi: OFF)	

## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Power-supply voltage	V <sub>CC</sub>	7	V	
Input voltage	V <sub>IN</sub>	GND–0.3 to V <sub>CC</sub> +0.3	V	
Bus input voltage	V <sub>bus</sub>	18	V	
Allowable power dissipation	P <sub>d</sub>	400	mW	Ta ≤ 85°C
Operating temperature	T <sub>opr</sub>	–40 to +85	°C	
Storage temperature	T <sub>stg</sub>	–55 to +125	°C	

Note: Recommended operating power supply voltage range: 5 V ± 0.5 V

## Electrical Characteristics

(V<sub>CC</sub> = 5.0 V, Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Test Pin	Test Circuit	
S1	High-level input voltage	V <sub>IHS1</sub>	2.1	—	—	V	V1 = 0→5 V, V3 = 0 V, V6 – V5 = 110 mV↑	1	Fig. 1
	Low-level input voltage	V <sub>ILS1</sub>	—	—	1.65	V	V1 = 5→0 V, V3 = 0 V, V6 – V5 = 30 mV↓	1	
	High-level input current	I <sub>IHS1</sub>	—	—	1	μA	V1 = 5 V, V3 = 0 V	1	
	Low-level input current	I <sub>ILS1</sub>	—	—	1	μA	V1 = 0 V, V3 = 0 V	1	
S2	High-level input voltage	V <sub>IHS2</sub>	2.1	—	—	V	V3 = 0→5 V, V1 = 0 V, V6 – V5 = 110 mV↑	3	Fig. 1
	Low-level input voltage	V <sub>ILS2</sub>	—	—	1.65	V	V3 = 5→0 V, V1 = 0 V, V6 – V5 = 30 mV↓	3	
	High-level input current	I <sub>IHS2</sub>	—	—	1	μA	V1 = 0 V, V3 = 5 V	3	
	Low-level input current	I <sub>ILS2</sub>	—	—	1	μA	V1 = 0 V, V3 = 0 V	3	
Driver	High-level output voltage (+)	V <sub>OHD+</sub>	1.8	2.5	3.2	V	V1 = 5 V, V3 = 0 V	6	Fig. 1
	High-level output voltage (–)	V <sub>OHD–</sub>	1.8	2.5	3.2	V	V1 = 5 V, V3 = 0 V	5	
	High-level output current	I <sub>OH</sub>	3.1	3.8	4.5	mA	V1 = 5 V, V3 = 0 V, I <sub>OH</sub> = ((V <sub>OHD+</sub> ) – (V <sub>OHD–</sub> ))/60	5, 6	
	Low-level output current	I <sub>OL</sub>	—	—	1	μA	V1 = 0 V, V3 = 0 V, I <sub>OL</sub> = ((V <sub>OP+</sub> ) – (V <sub>OP–</sub> ))/R <sub>I</sub>	5, 6	
Reference operating voltage (+)	V <sub>OP+</sub>	2.3	2.5	2.7	V	V1 = 0 V, V3 = 0 V	6	Fig. 1	
Reference operating voltage (–)	V <sub>OP–</sub>	2.3	2.5	2.7	V	V1 = 0 V, V3 = 0 V	5	Fig. 1	
Driver output resistance *1	R <sub>O</sub>	5	10	15	kΩ	V1 = 5 V, V3 = 0 V, V8 = 5 V, R <sub>O</sub> = 0.6 V/(I6A – I6B)		Fig. 3	

Note: 1. Measure the current when V6 = (V<sub>OP+</sub>) + 0.3 V to make I6A and measure the current when V6 = (V<sub>OP+</sub>) – 0.3 V to make I6B.

## Electrical Characteristics (cont.)

(V<sub>CC</sub> = 5.0 V, T<sub>a</sub> = 25°C)

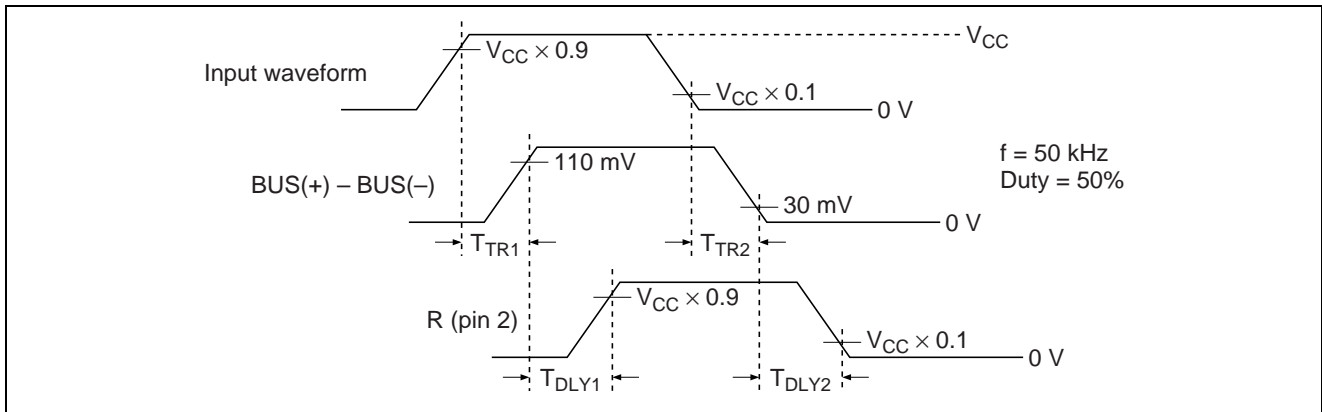
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Test Pin	Test Circuit
Receiver High-level input voltage (1)	V <sub>IH1</sub>	—	80	110	mV	V6 = 0→5 V, Pin2 = 4 V or more, V1 = 0 V, V3 = 0 V, V5 = 0 V, V <sub>IH1</sub> = V6 – V5	2	Fig. 2
High-level input voltage (2)	V <sub>IH2</sub>	—	80	110	mV	V6 = 0→5 V, Pin2 = 4 V or more, V1 = 0 V, V3 = 0 V, V5 = 4.5 V, V <sub>IH2</sub> = V6 – V5	2	
Low-level input voltage (1)	V <sub>IL1</sub>	30	50	—	mV	V6 = 5→0 V, Pin2 = 1 V or less, V1 = 0 V, V3 = 0 V, V5 = 0 V, V <sub>IL1</sub> = V6 – V5	2	
Low-level input voltage (2)	V <sub>IL2</sub>	30	50	—	mV	V6 = 5→0 V, Pin2 = 1 V or less, V1 = 0 V, V3 = 0 V, V5 = 4.5 V, V <sub>IL2</sub> = V6 – V5	2	
Input hysteresis voltage (1)	V <sub>IHYS1</sub>	15	30	45	mV	V <sub>IHYS1</sub> = V <sub>IH1</sub> – V <sub>IL1</sub>		
Input hysteresis voltage (2)	V <sub>IHYS2</sub>	15	30	45	mV	V <sub>IHYS2</sub> = V <sub>IH2</sub> – V <sub>IL2</sub>		
High-level common-mode input voltage	V <sub>IHCOM</sub>	4.5	—	—	V	V5 = 0→5 V, V5 when pin2 = 4 V or less, V1 = 0 V, V3 = 0 V, V6 – V5 = 110 mV	5	Fig. 2
Low-level common-mode input voltage	V <sub>ILCOM</sub>	5	—	—	V	V5 = 0→5 V, V5 when pin2 = 0.3 V or more, V1 = 0 V, V3 = 0 V, V6 – V5 = 30 mV	5	
Input resistance *1	R <sub>I</sub>	25	35	45	kΩ	V1 = 0 V, V3 = 0 V, V8 = 5 V, R <sub>I</sub> = 0.6 V/(I6A – I6B)	5, 6	Fig. 3
High-level output leakage current 1	I <sub>OH1</sub>	—	—	1	μA	V1 = 5 V, V3 = 0 V, V8 = 5 V	2	Fig. 1
High-level output leakage current 2	I <sub>OH2</sub>	—	—	1	μA	V <sub>CC</sub> = 0 V, V1, V3, V8 = 0 V	2	
High-level output leakage current 3	I <sub>OH3</sub>	—	—	1	μA	V1, V3, V8 = 0 V	2	
Low-level output voltage 1	V <sub>OL1</sub>	—	—	0.6	V	V1 = 0 V, V3 = 0 V, V8 = 5 V, Adjust V <sub>RL</sub> to make apply current = 1.5 mA	2	
Low-level output voltage 2	V <sub>OL2</sub>	—	—	0.3	V	V1 = 0 V, V3 = 0 V, V8 = 5 V, Adjust V <sub>RL</sub> to make apply current = 200 μA	2	
Quiescent current 1	I <sub>CCH</sub>	4.5	6.5	8.5	mA	V1 = 5 V, V3 = 0 V	7	Fig. 1
Quiescent current 2	I <sub>CCL</sub>	1.05	1.46	1.87	mA	V1 = 0 V, V3 = 0 V	7	Fig. 1
Driver delay time (L→H)	T <sub>TR1</sub>	—	100	300	ns	See operating waveform figure	5, 6	Fig. 5
Driver delay time (H→L)	T <sub>TR2</sub>	—	100	300	ns	See operating waveform figure	5, 6	
Receiver delay time (L→H)	T <sub>DLY1</sub>	—	600	1200	ns	See operating waveform figure	2	
Receiver delay time (H→L)	T <sub>DLY2</sub>	—	200	600	ns	See operating waveform figure	2	

Note: 1. Measure the current when V6 = (V<sub>OP+</sub>) + 0.3 V to make I6A and measure the current when V6 = (V<sub>OP+</sub>) – 0.3 V to make I6B.

Electrical Characteristics (cont.)

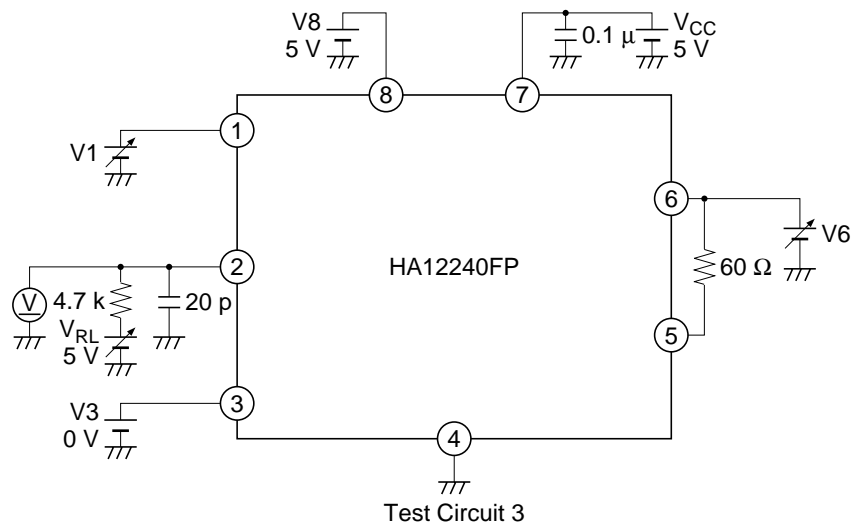
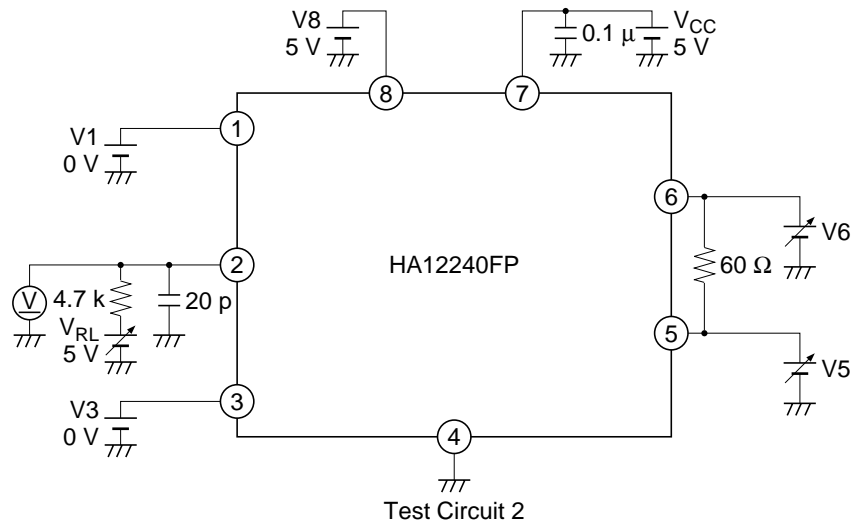
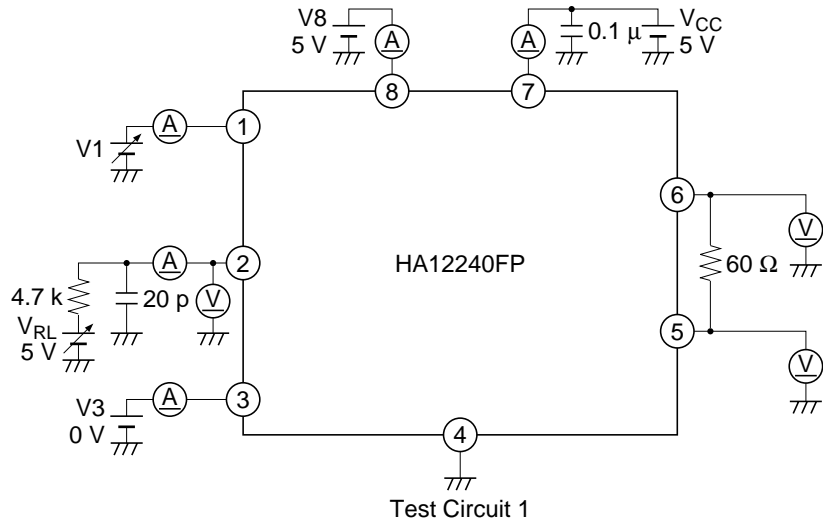
( $V_{CC} = 5.0\text{ V}$ ,  $T_a = 25^\circ\text{C}$ )

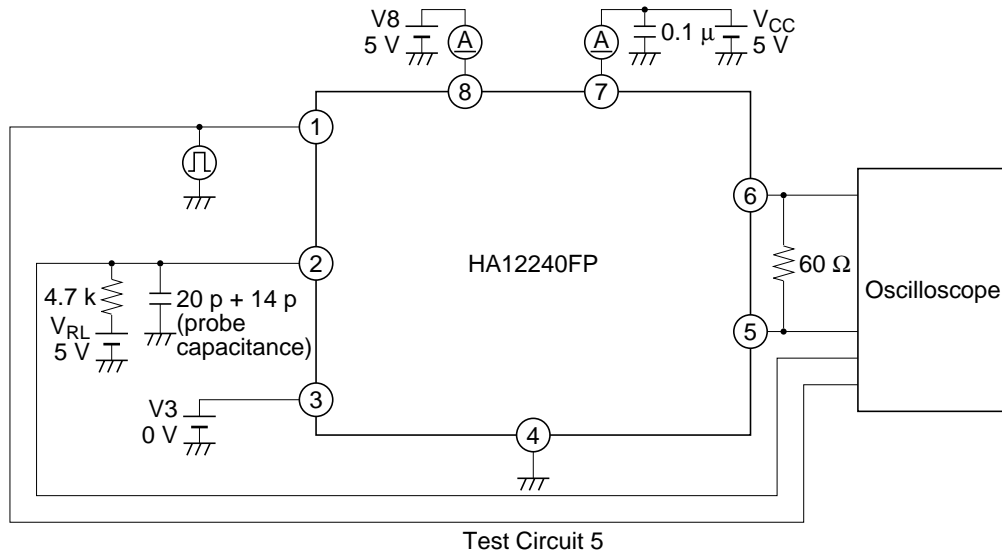
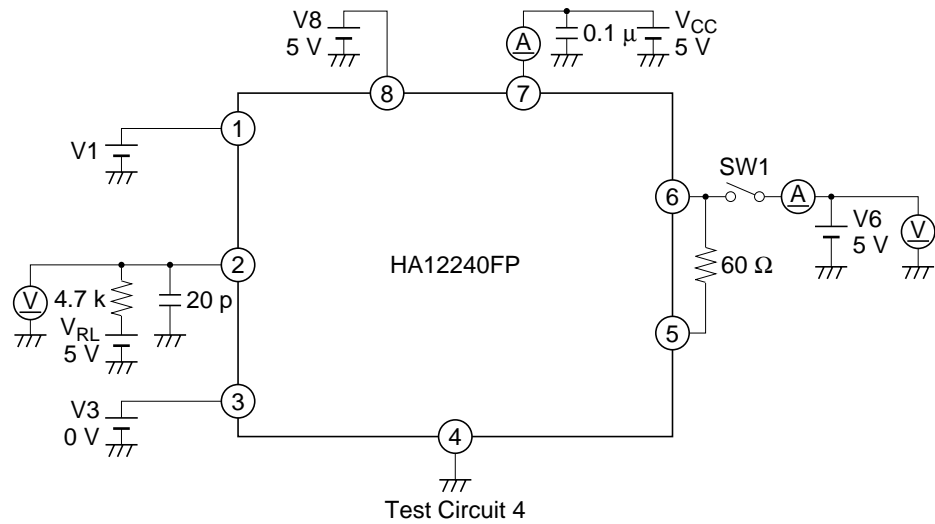
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Test Pin	Test Circuit
Power-supply off output leakage current	$I_{OLEAK}$	—	—	1	$\mu\text{A}$	$V_{CC} = 0\text{ V}$ , $V_8 = 0\text{ V}$ , $V_6 = 5\text{ V}$ , $V_1 = 0\text{ V}$ , $V_3 = 0\text{ V}$ , SW1 ON	6	Fig. 4
Standby mode current drain	$I_{CCstb}$	—	—	1	$\mu\text{A}$	$V_1 = 5\text{ V}$ , $V_3 = 0\text{ V}$ , $V_8 = 0\text{ V}$	7	Fig. 4
Standby mode output leakage current	Istb-Leak	—	—	1	$\mu\text{A}$	$V_1 = 5\text{ V}$ , $V_3 = 0\text{ V}$ , $V_8 = 0\text{ V}$ , $V_6 = 5\text{ V}$ , SW1 ON	6	Fig. 4
Standby mode high-level input voltage	VstbH	2	—	—	V	$V_8 = 0 \rightarrow 5\text{ V}$ , $V_8$ when pin5,6 = 2.3 V or more, $V_1 = 0\text{ V}$ , $V_3 = 0\text{ V}$	8	Fig. 1
Standby mode low-level input voltage	VstbL	—	—	0.9	V	$V_8 = 5 \rightarrow 0\text{ V}$ , $V_8$ when current flowing into pin7 = $1\text{ }\mu\text{A}$ or less, $V_1 = 5\text{ V}$ , $V_3 = 0\text{ V}$	8	Fig. 1
Standby mode high-level input current	IstbH	—	50	100	$\mu\text{A}$	$V_1 = 5\text{ V}$ , $V_3 = 0\text{ V}$ , $V_8 = 5\text{ V}$	8	Fig. 1
Standby mode low-level input current	IstbL	—	—	1	$\mu\text{A}$	$V_1 = 5\text{ V}$ , $V_3 = 0\text{ V}$ , $V_8 = 0\text{ V}$	8	Fig. 1



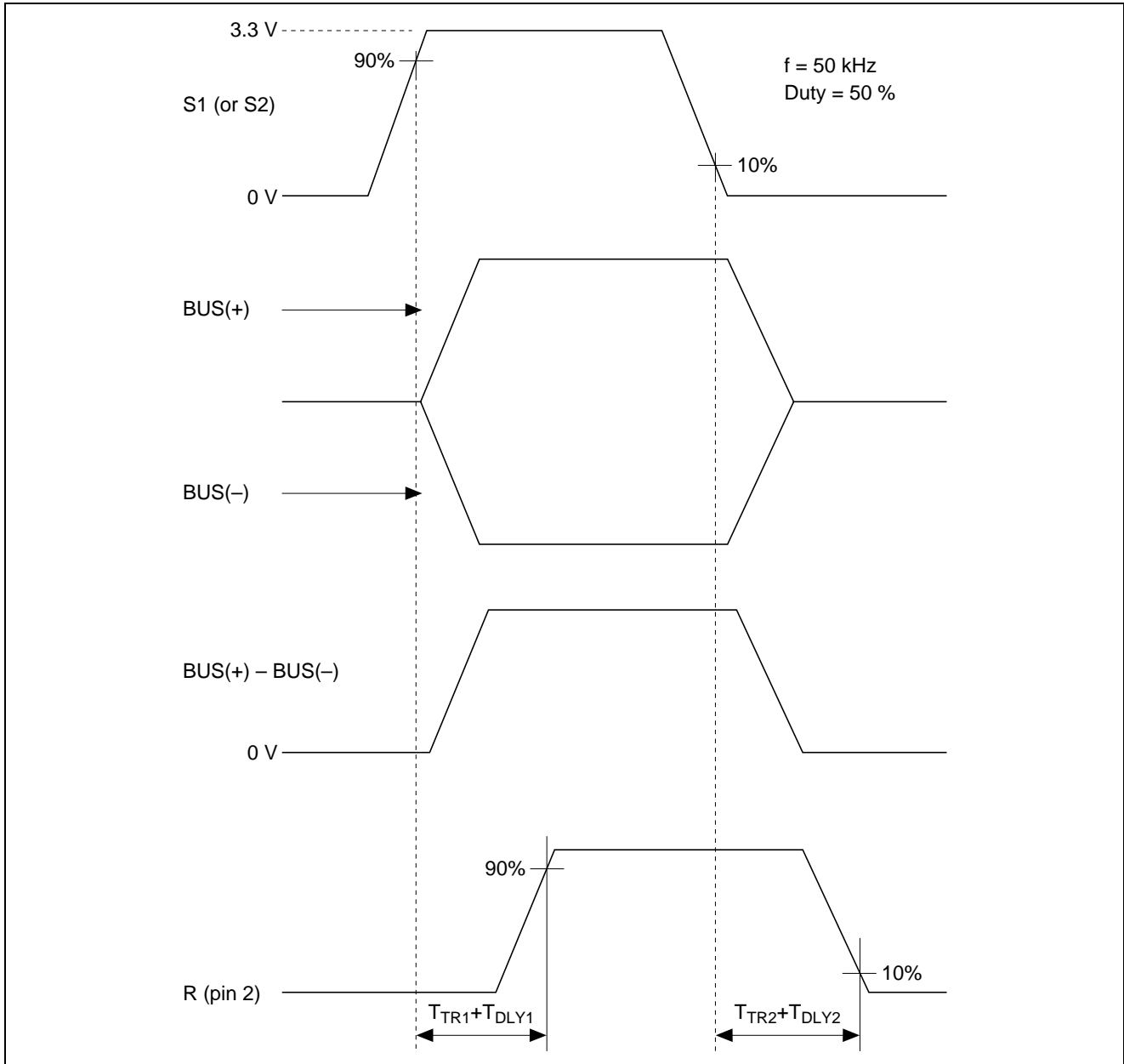
Input/Output Waveform Figure

Test Circuits



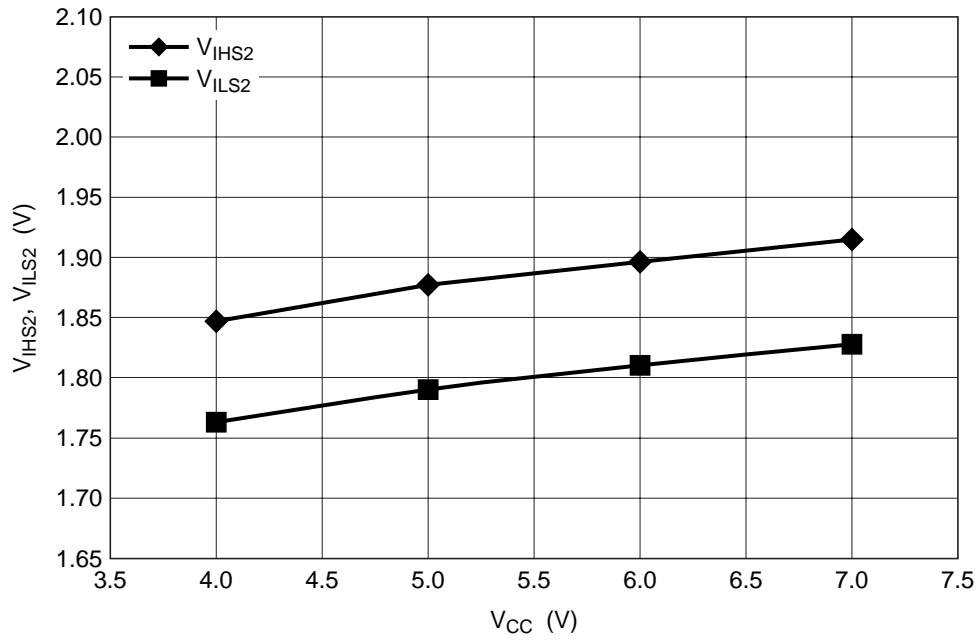
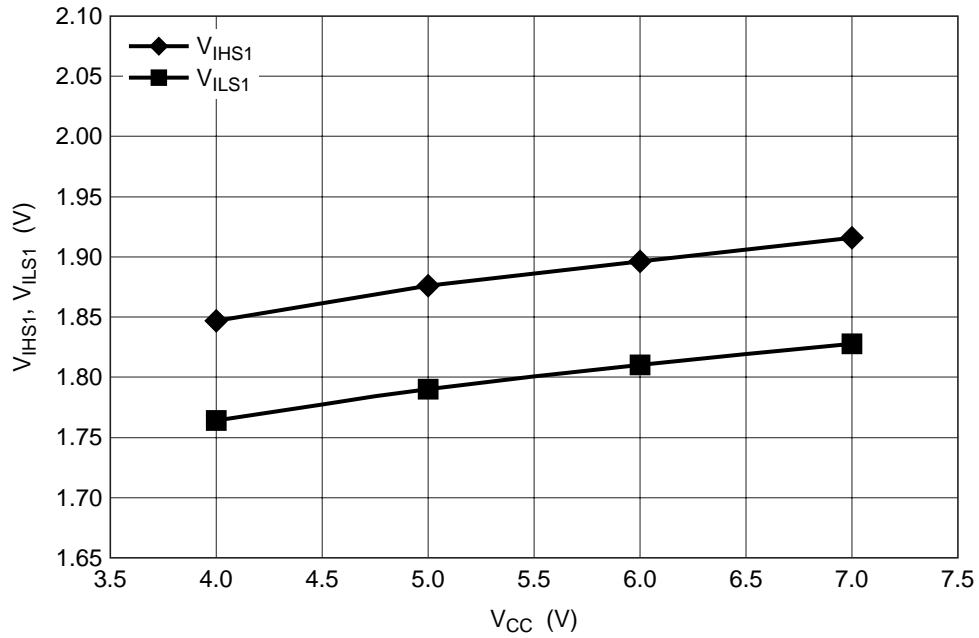


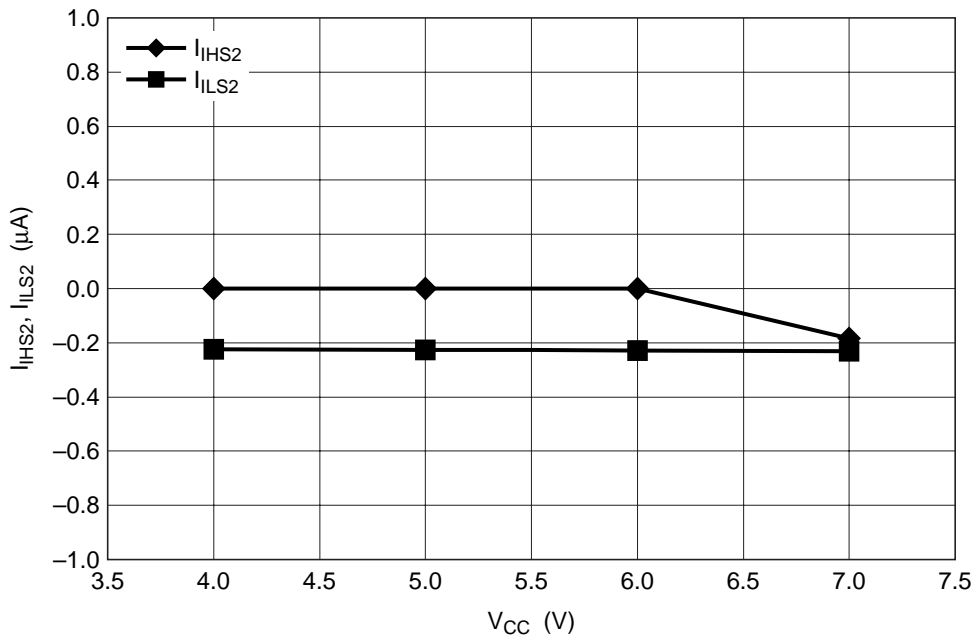
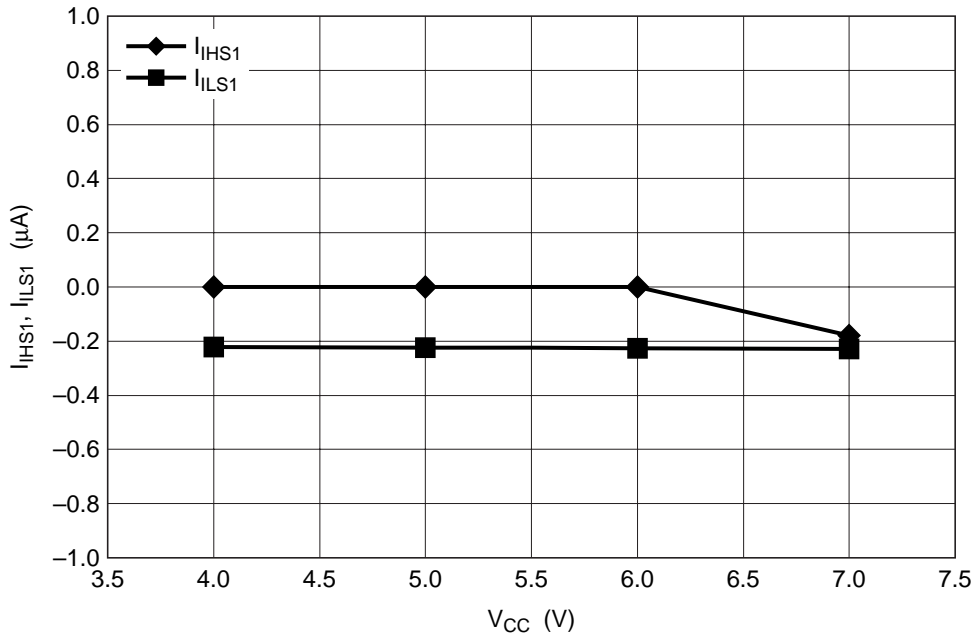
Operating Waveforms

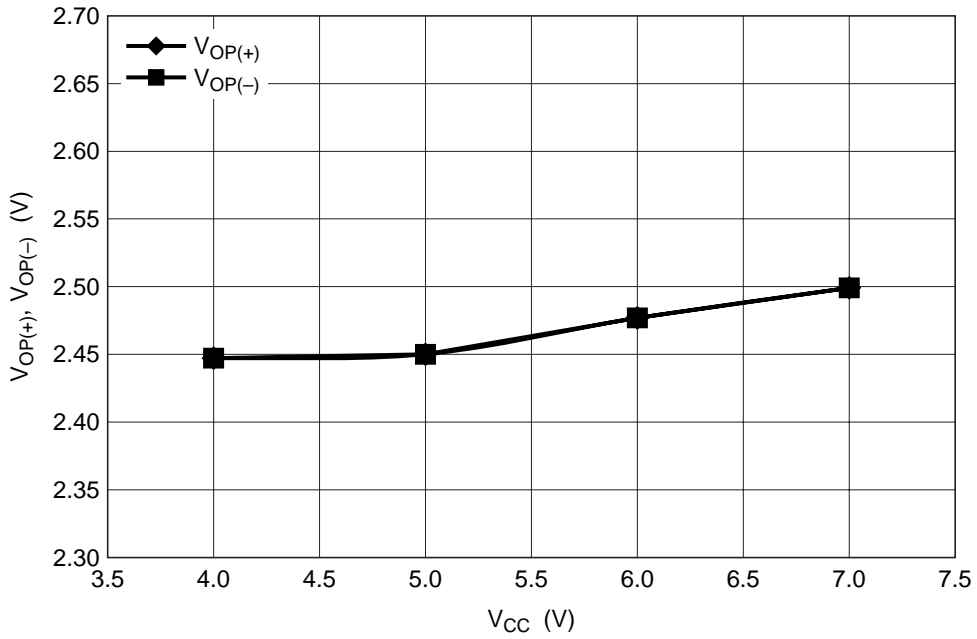
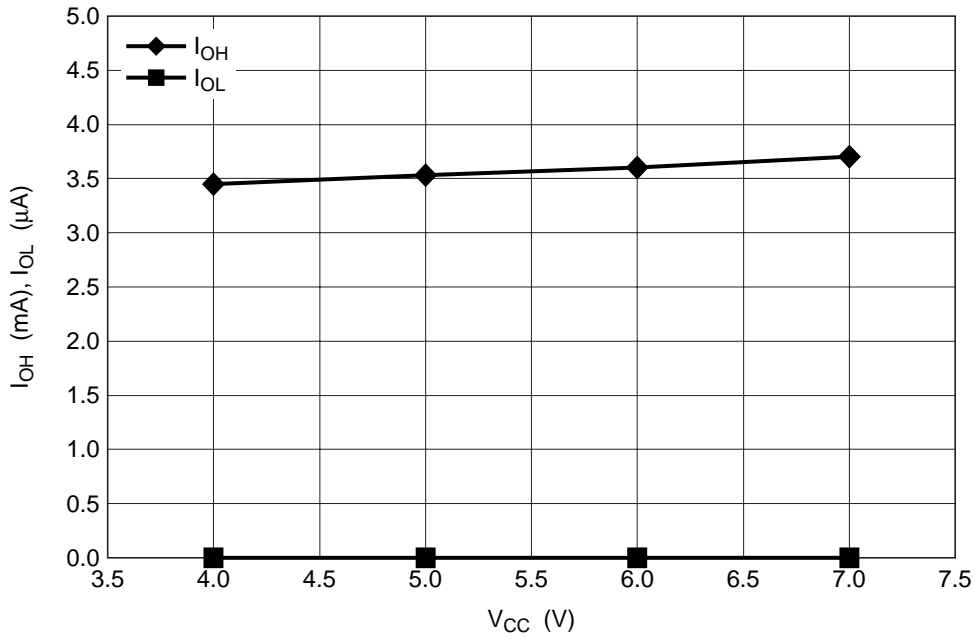


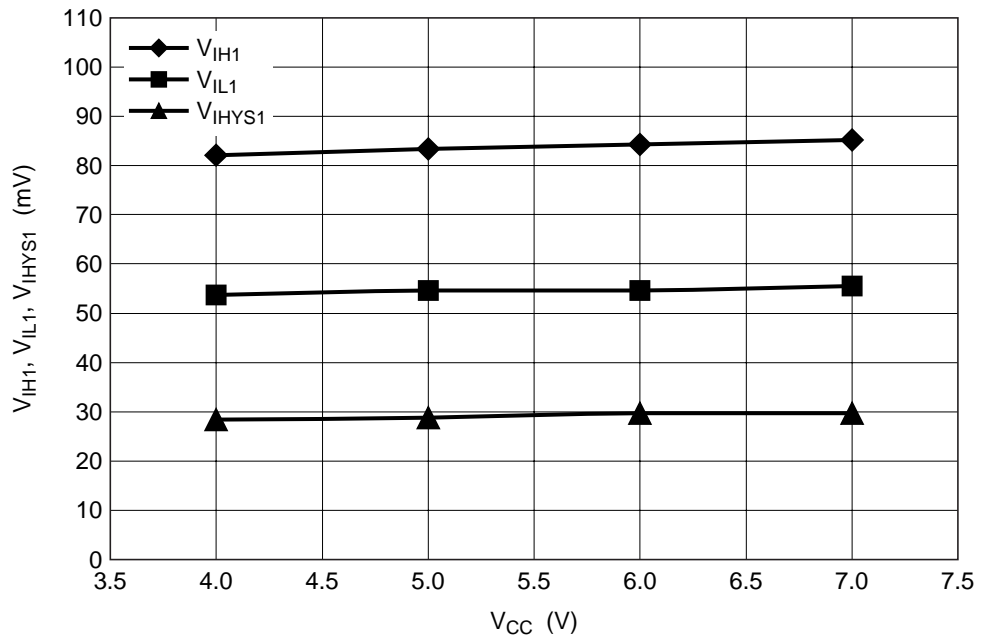
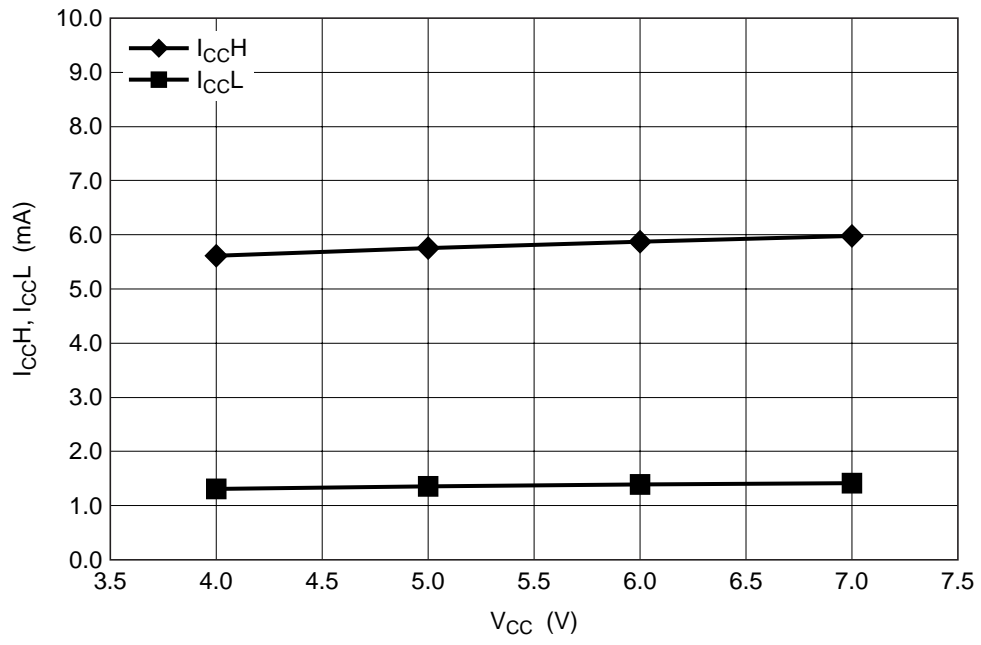


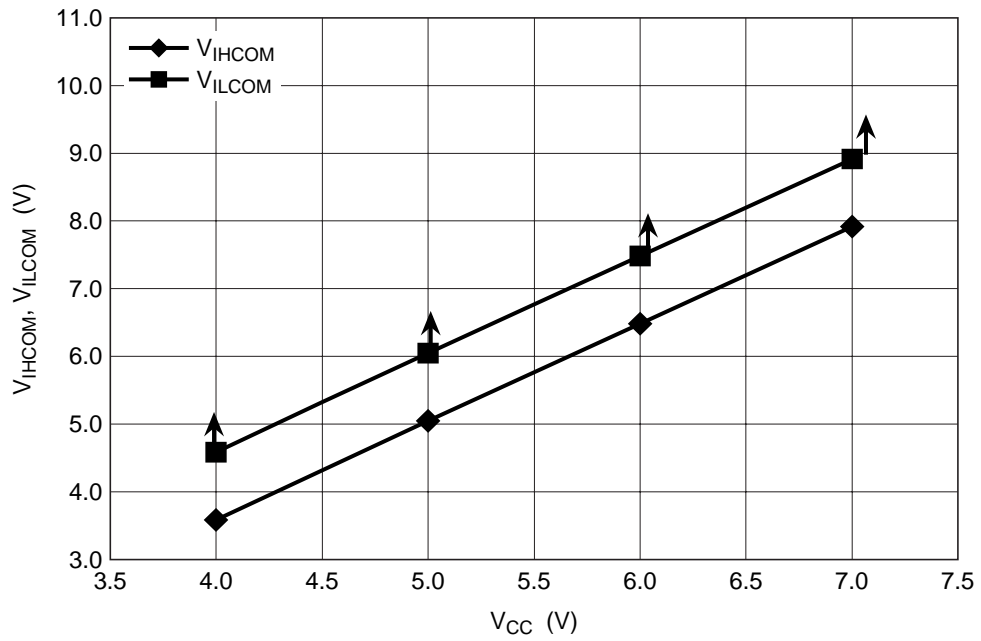
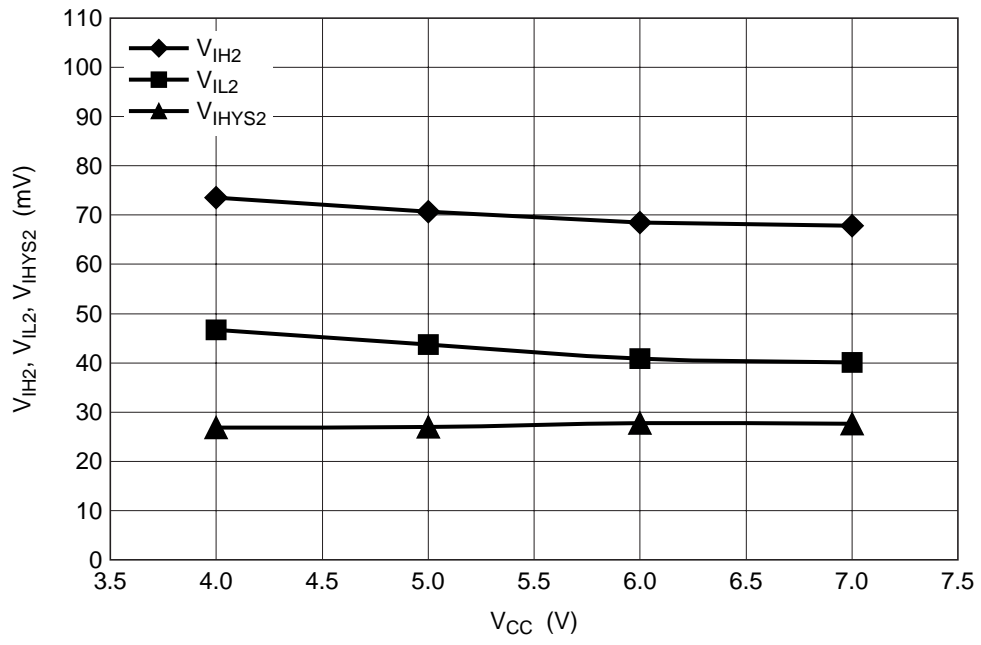
Main Characteristics

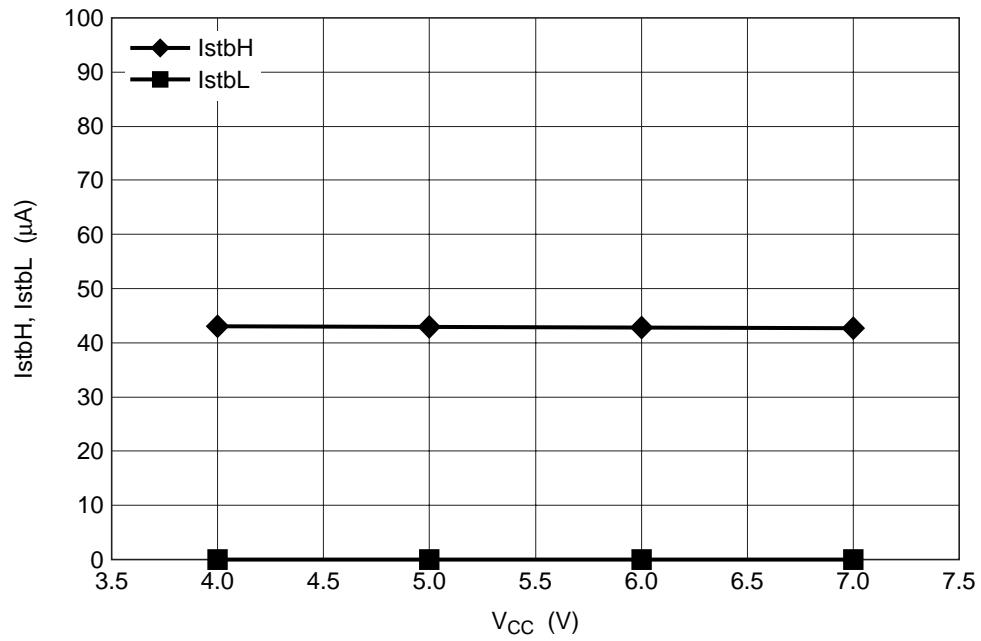
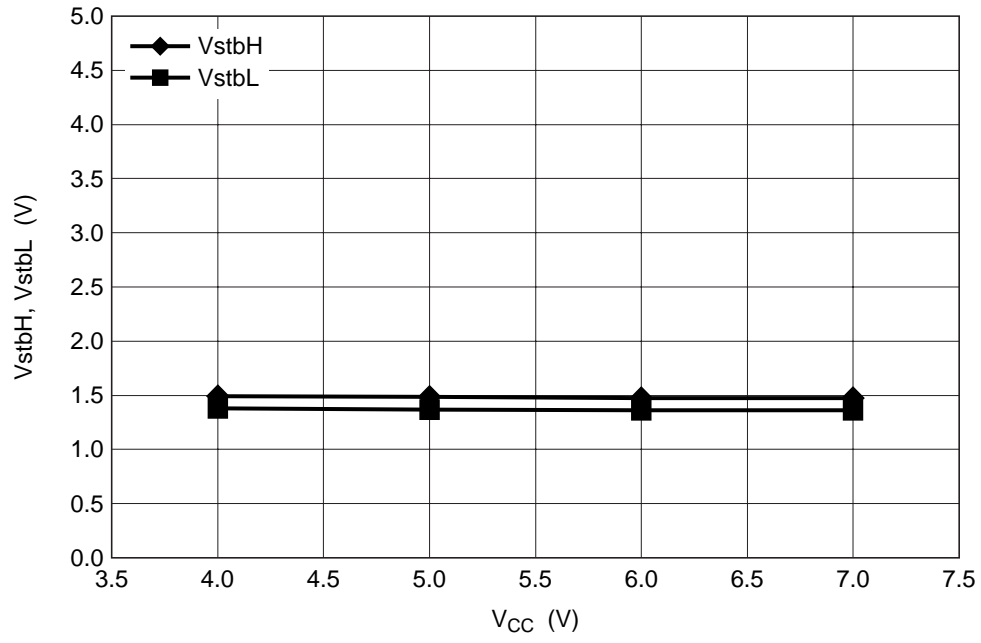


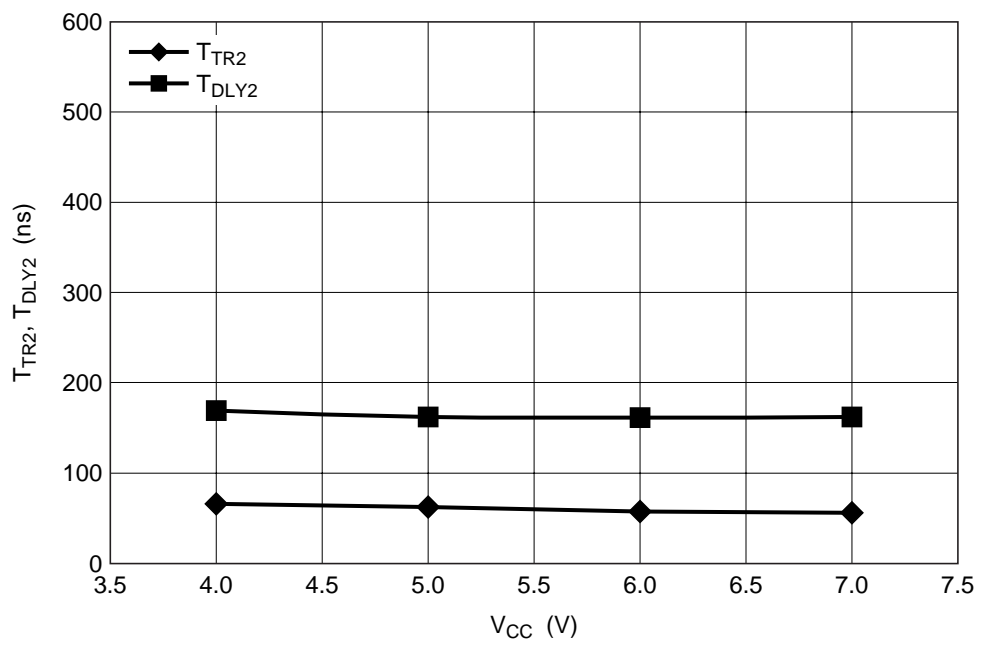
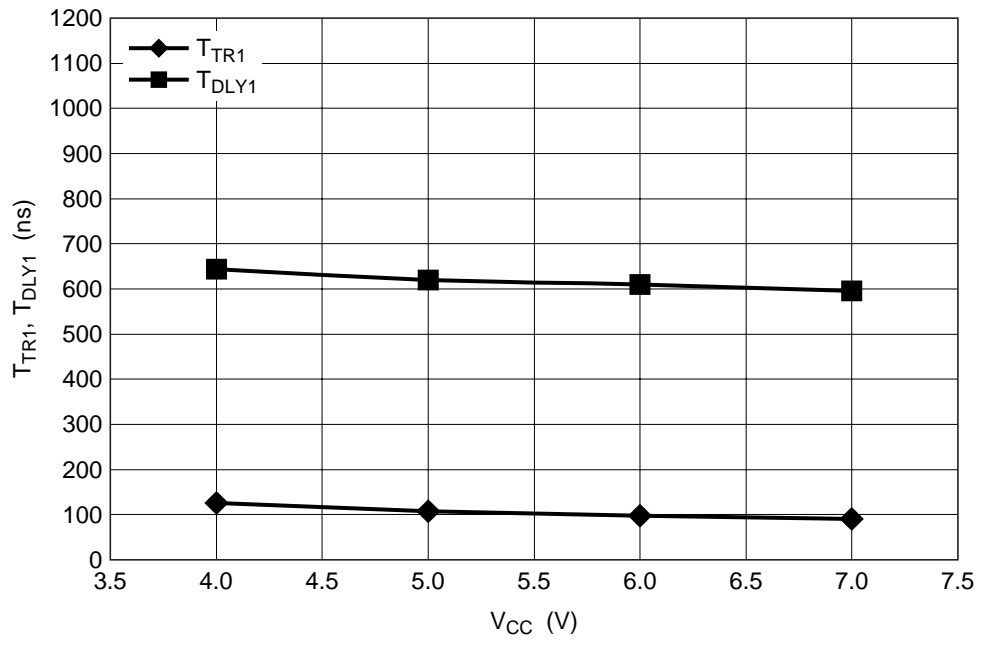


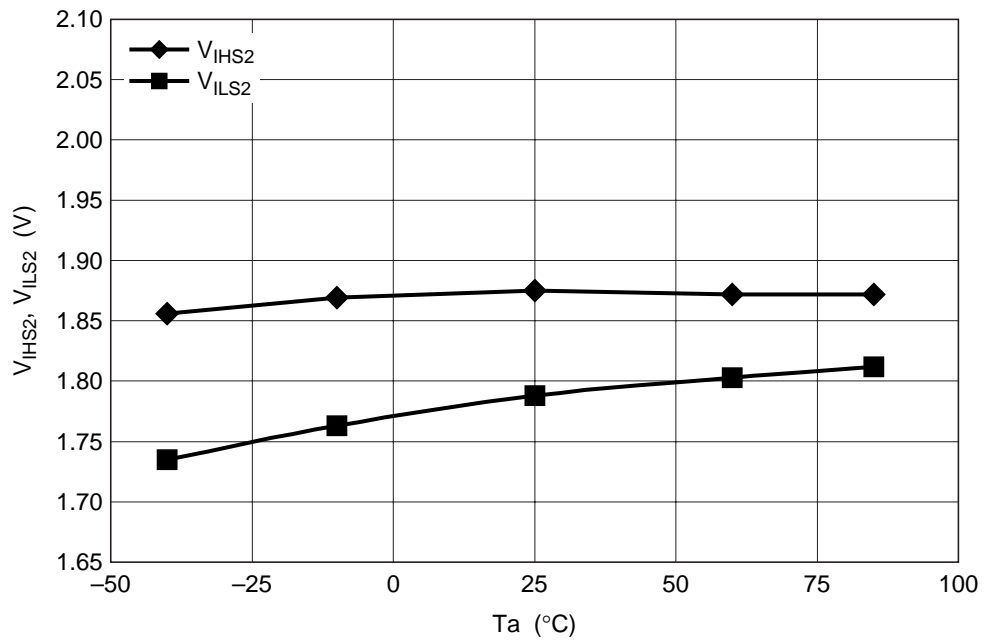
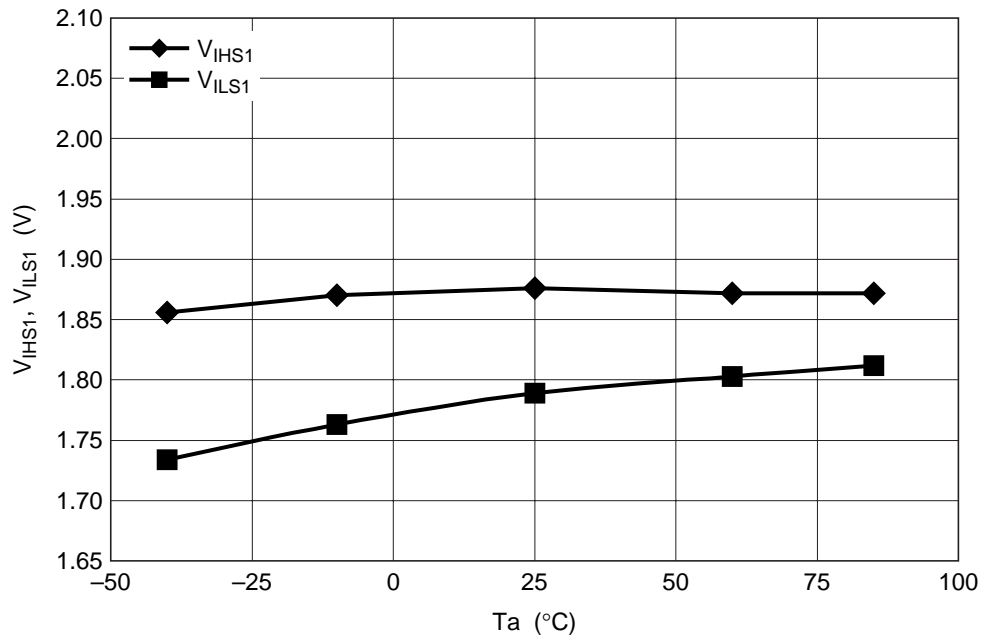




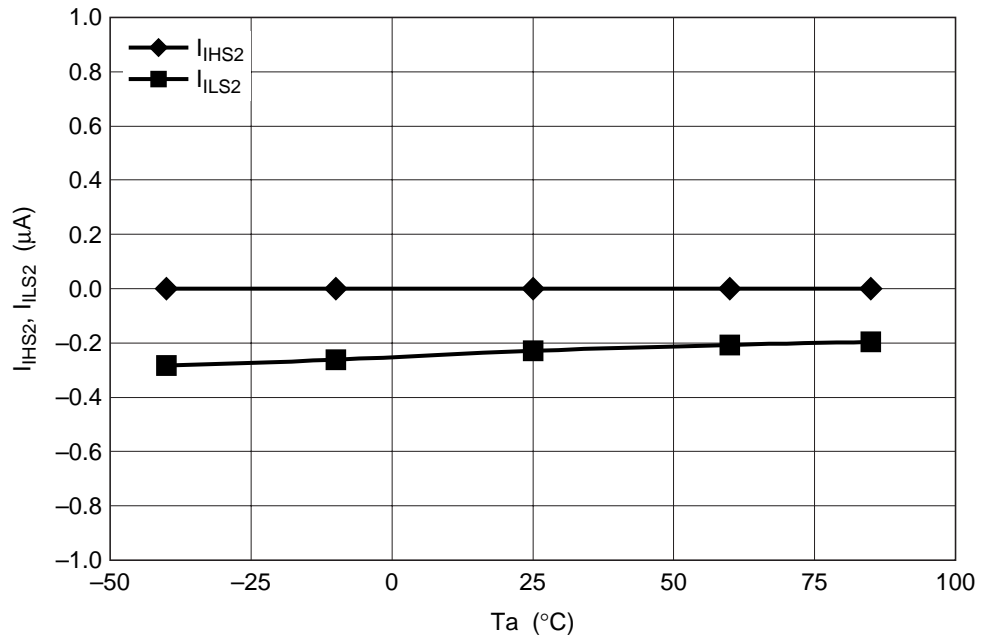
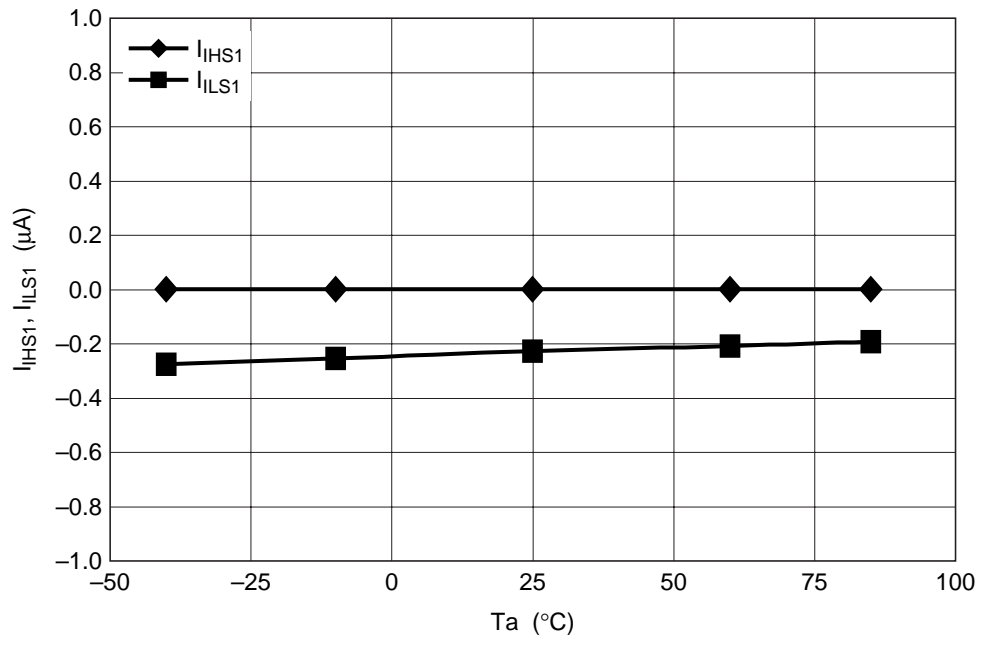


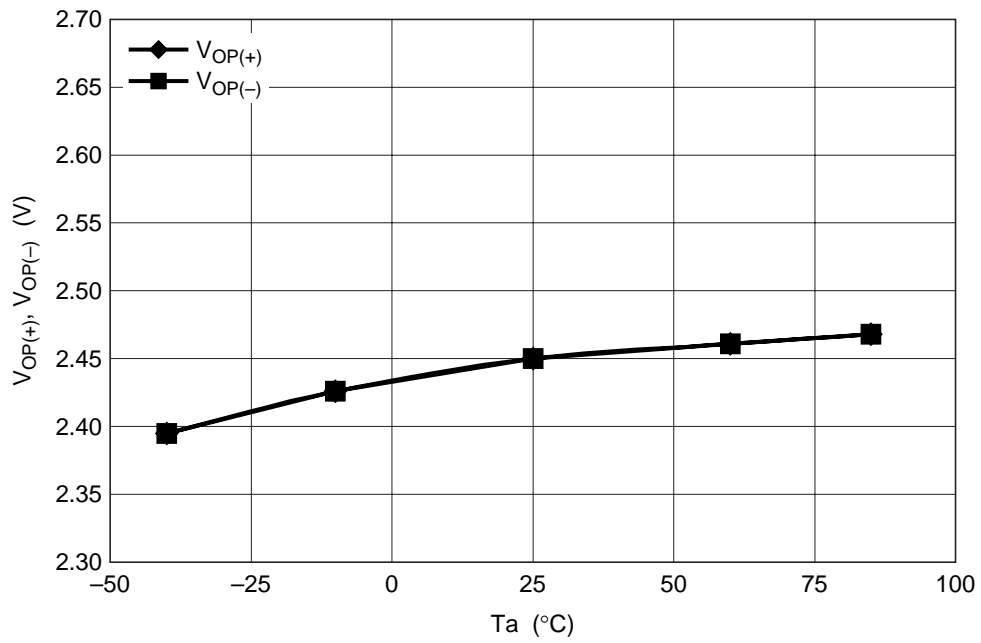
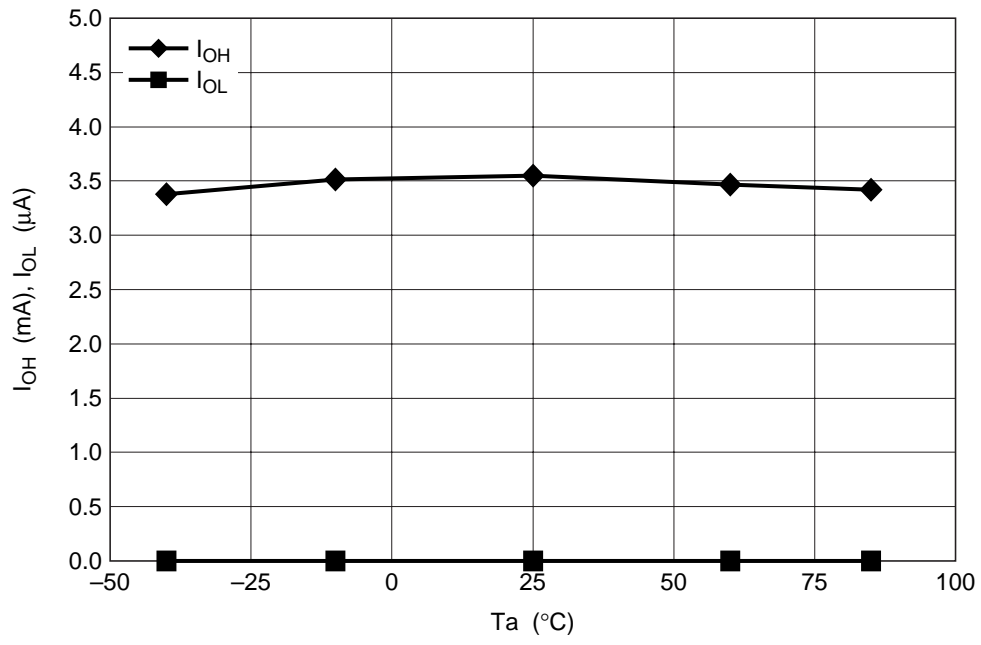


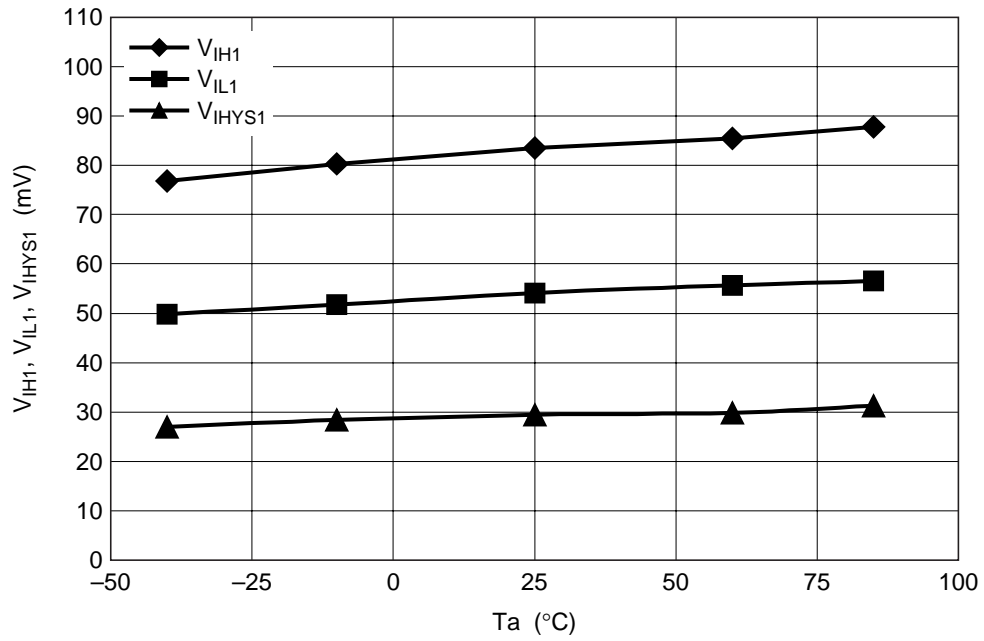
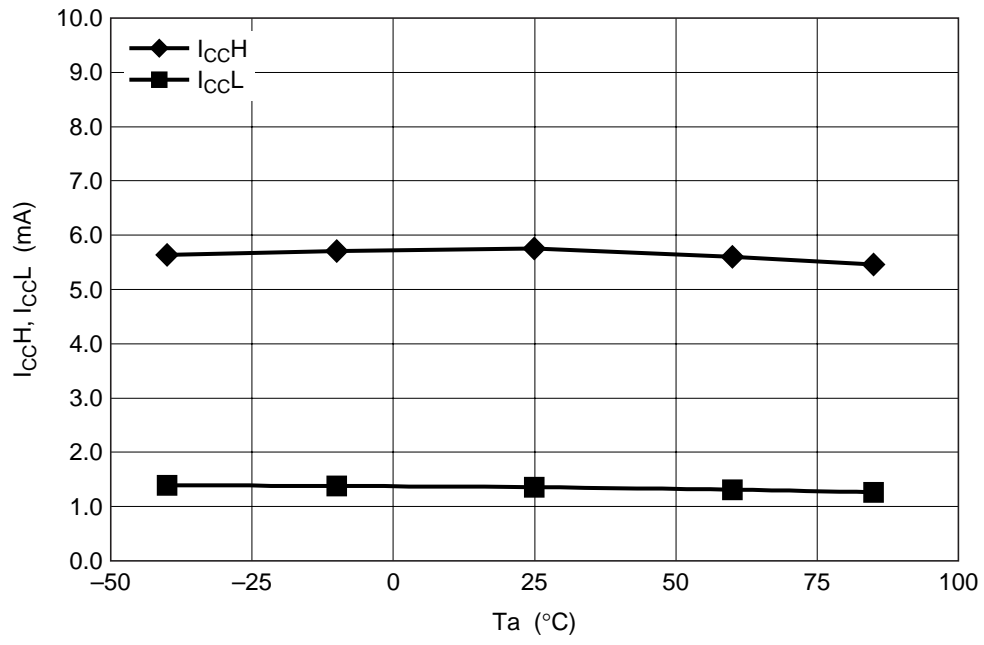


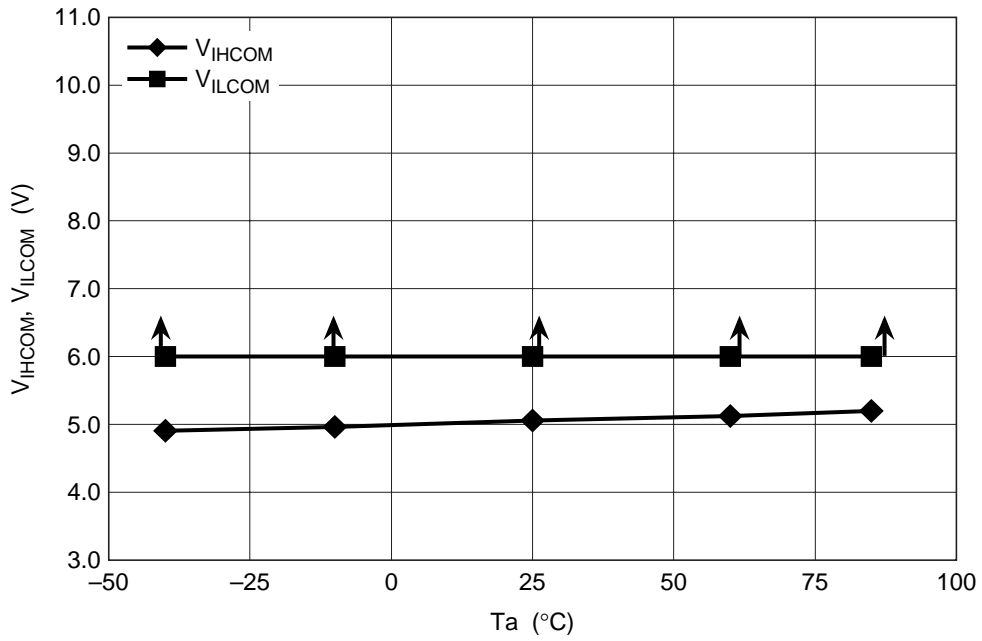
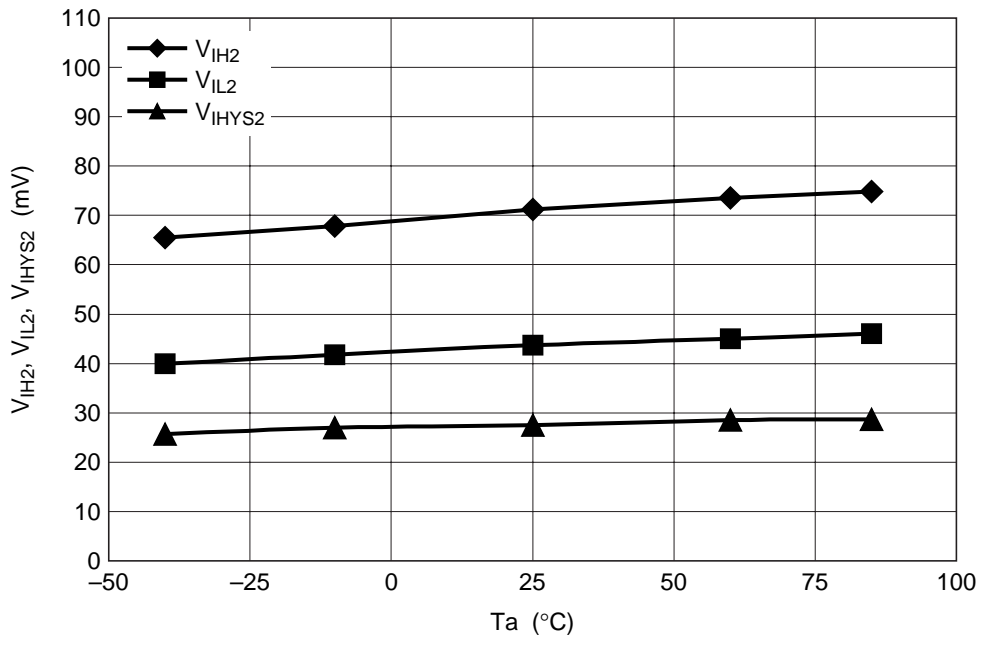


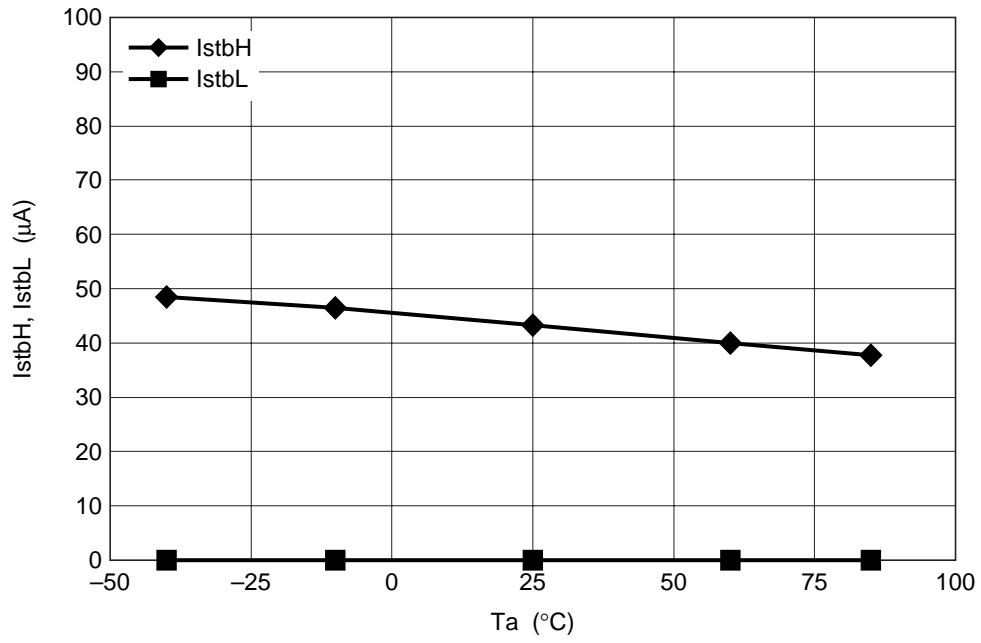
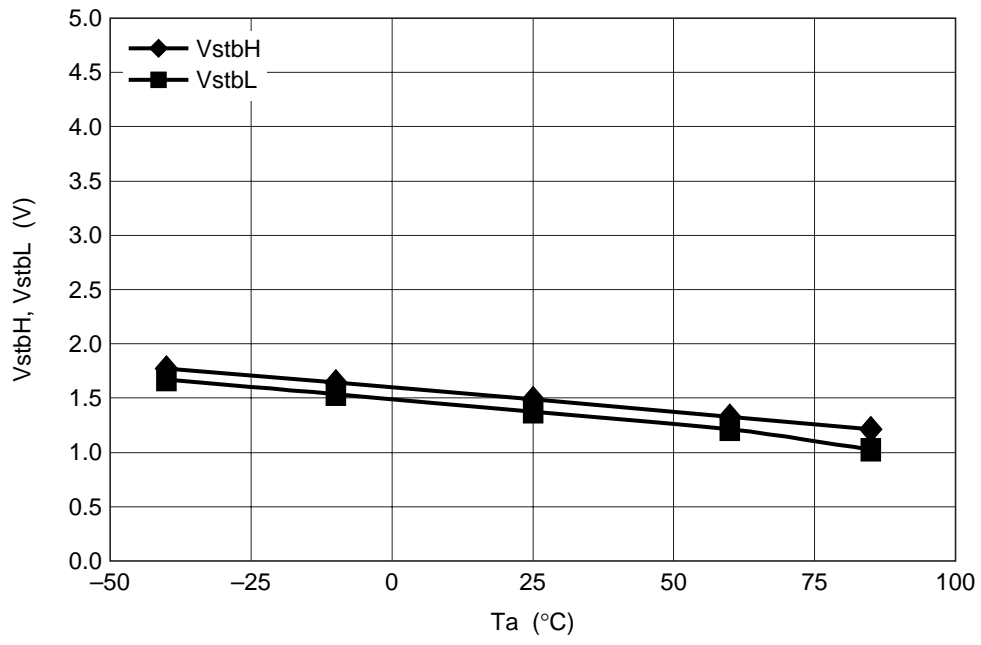


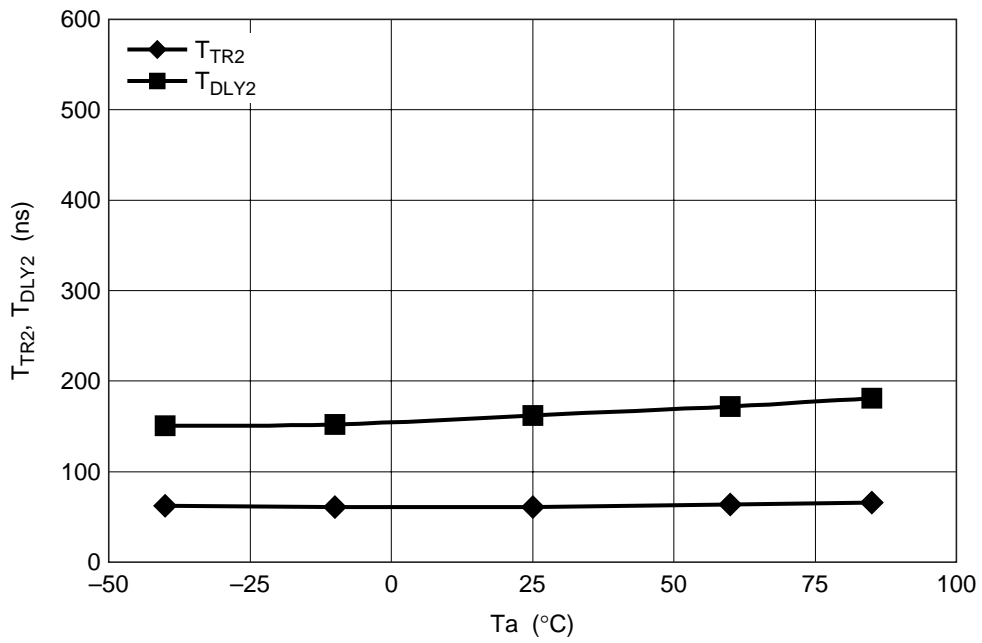
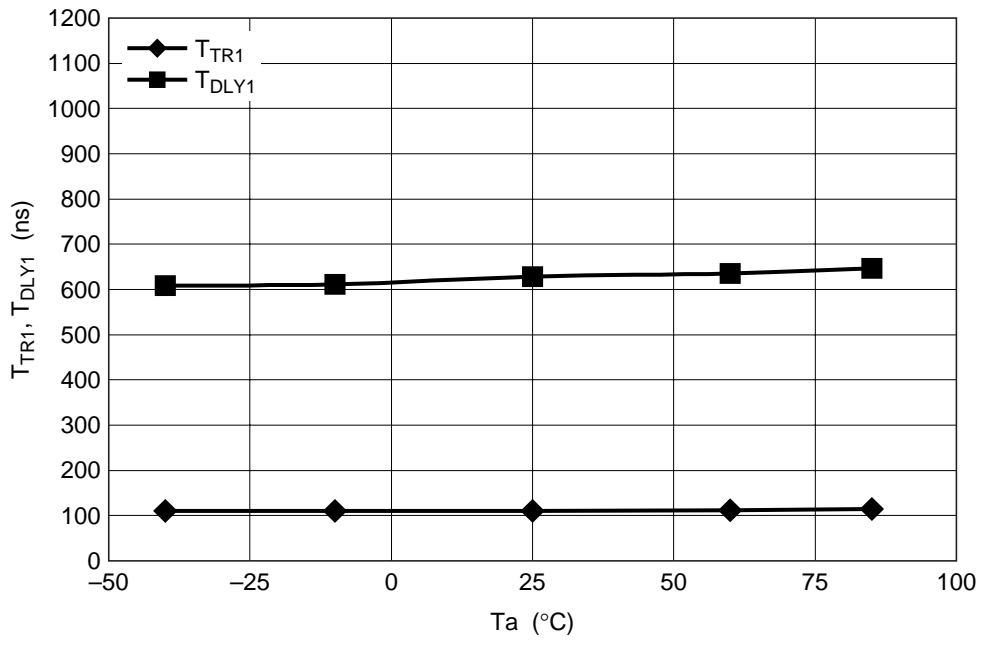






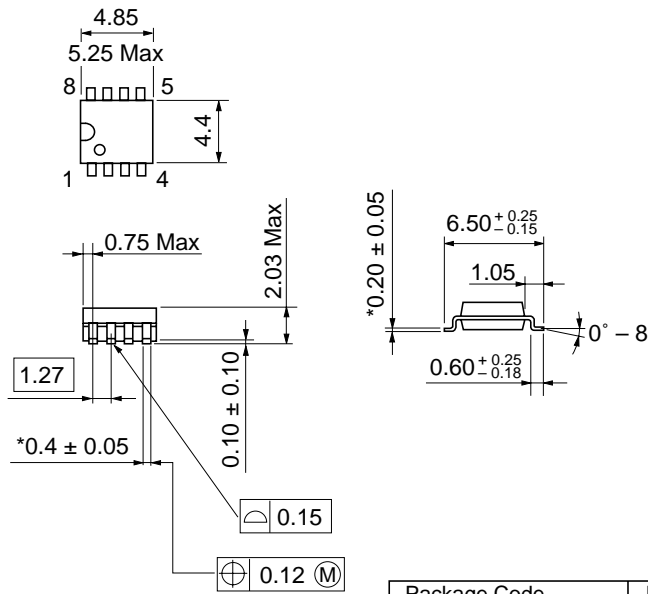






Package Dimensions

Unit: mm



\*Dimension including the plating thickness

Package Code	FP-8DGV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.10 g

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