AOZ1214

EZBuck 3A™ Simple Buck Regulator with Linear Controller

General Description

The AOZ1214 is a high efficiency, simple to use, buck regulator plus one linear regulator controller optimized for a variety of applications.

The AOZ1214 works from a 4.5V to 28V wide input voltage range. The buck regulator provides up to 3A of continuous output current. Each output voltage is adjustable down to 0.8V. The buck regulator and LDO can be enabled independently.

The AOZ1214 is available in a 4x3 DFN-12 package and can operate over a -40°C to +85°C ambient temperature range.

Features

- 4.5V to 28V operating input voltage range
- Integrated linear regulator controller
- 40 mΩ internal NFET, efficiency: up to 95%
- Internal soft start
- Each output voltage adjustable down to 0.8V
- 3A continuous output current
- Fixed 370 kHz PWM operation
- Cycle-by-cycle current limit
- Short-circuit protection
- Thermal shutdown
- Small size 4x3 DFN-12 package
- Independent enable input for Buck and LDO

Applications

- Point of load DC/DC conversion
- Set top boxes
- LCD Monitors & TVs
- Cable modems
- Telecom/Networking/Datacom equipment

Green Product

Typical Application

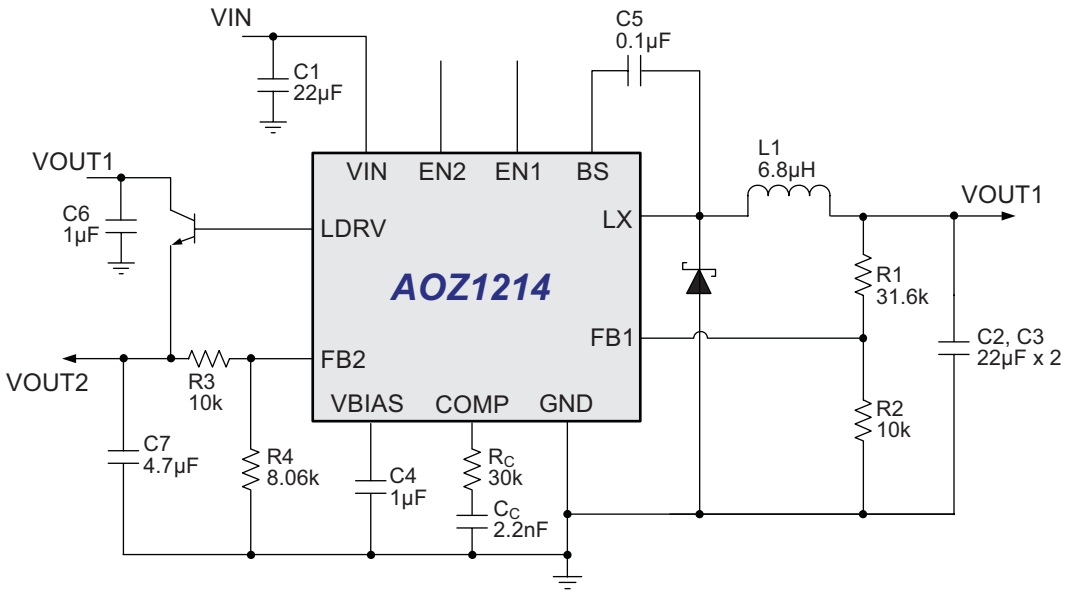


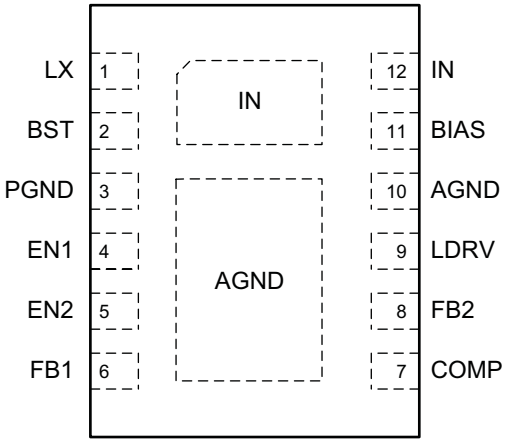
Figure 1. Typical Application Circuit

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ1214DI	-40°C to +85°C	4x3 DFN-12L	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration

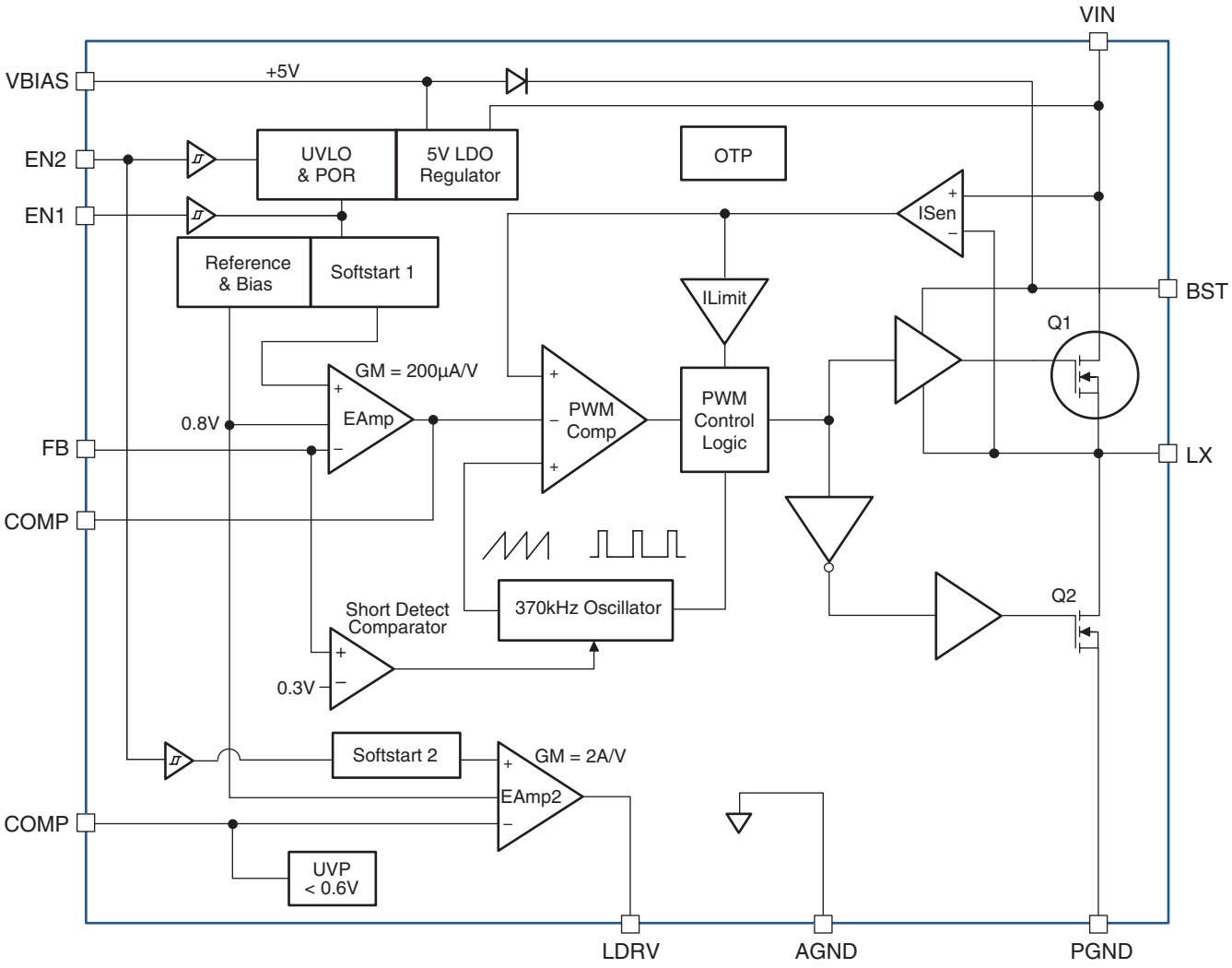


DFN-12
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	LX	Buck Regulator Switching Node.
2	BST	Buck Regulator Bootstrap Pin. BST is the high side driver supply. Connect a 0.1μF capacitor between BST and LX to form a bootstrap circuit.
3	PGND	Power Ground.
4	EN1	Enable1 input for buck regulator. EN1 is active high. Connect EN1 to IN if not used. Do not leave EN1 floating.
5	EN2	Enable2 input for linear regulator. EN2 is active high.
6	FB1	Buck Regulator Feedback Input. FB1 is regulated to 0.8V. Set the buck regulator output voltage using a resistive voltage divider.
7	COMP	Buck Regulator Compensation Pin. COMP is the output of the internal transconductance error amplifier. Connect a RC network between COMP and GND to compensate the control loop.
8	FB2	Linear Regulator Feedback Input. FB2 is regulated to 0.8V. Set the linear regulator output voltage using a resistive voltage divider.
9	LDRV	Linear Regulator Drive Output. LDRV controls the gate of an external pass transistor.
10	AGND	Analog Ground.
11	BIAS	Internal Bias Regulator Output. Connect a 1μF between BIAS and GND.
12	IN	Input Supply Pin. The input range is between 4.5V and 28V.

Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
Supply Voltage (V_{IN})	30V
LX to GND	-0.7V to V_{IN} + 0.3V
EN1, EN2 to GND	-0.3V to V_{IN} + 0.3V
FB1, FB2 to GND	-0.3V to 6V
COMP to GND	-0.3V to 6V
BST to GND	V_{LX} + 6V
LDRV to GND	-0.3V to 6V
PG to GND	-0.3V to 30V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (V_{IN})	4.5V to 28V
Output Voltage Range	0.8V to V_{IN}
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance 4 x 3 DFN-12 (Θ_{JA})(1) 4 x 3 DFN-12 (Θ_{JC})	 64.6°C/W 7.1°C/W

Note:

1. The value of Θ_{JA} is measured with the device mounted on 1-in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.

Electrical Characteristics

T_A = 25°C, V_{IN} = V_{EN} = 12V, unless otherwise specified(2).

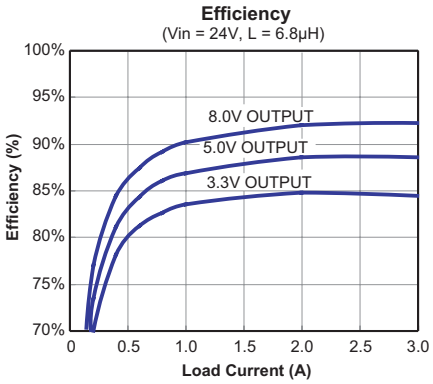
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN}	Supply Voltage		**4.5**		**28**	V
V_{UVLO}	Input Under-Voltage Lockout Threshold	V_{IN} Rising V_{IN} Falling		**4.0** **3.7**		V V
I_{IN}	Supply Current (Quiescent)	I_{OUT} = 0, VFB = 1.2V, V_{EN} > 2V		**2**	**3**	mA
I_{OFF}	Shutdown Supply Current	V_{EN1} = V_{EN2} = 0V		3	20	µA
$V_{FB1, 2}$	Feedback Voltage		0.788	0.8	0.812	V
	Load Regulation			0.5		%
	Line Regulation			0.1		%
I_{FB1}	Feedback Voltage Input Current				200	nA
ENABLE						
$V_{EN1,2}$	EN1,2 Input Threshold	Off Threshold On Threshold	 **2.5**		**0.6**	V V
V_{HYS}	EN1,2 Input Hysteresis			**200**		mV
$I_{EN1,2}$	EN1,2 Sink/Source Current				50	nA
MODULATOR						
f_O	Frequency		315	370	425	kHz
D_{MAX}	Maximum Duty Cycle			85		%
D_{MIN}	Minimum Duty Cycle			5		%
G_{VEA}	Error Amplifier Voltage Gain			500		V / V
G_{EA}	Error Amplifier Transconductance			200		µA / V
PROTECTION						
I_{LIM}	Current Limit		4	5	6	A
	Over-Temperature Shutdown Limit	T_J Rising T_J Falling		145 100		°C °C
t_{SS1}	Soft Start Interval 1			6		ms
t_{SS2}	Soft Start Interval 2			6		ms
PWM OUTPUT STAGE						
$R_{DS(ON)}$	High-Side Switch On-Resistance			40	50	mΩ
	High-Side Switch Leakage	V_{EN} = 0V, V_{LX} = 0V			10	µA
LINEAR CONTROLLER						
LDRV Vout	Drive Output High Voltage	Vfb2 = 0.7V, LDRV Iout = 20mA, Iout1 = 0	4			V
LDRV Iout	Drive Output Current	Vfb2 = 0.7V, Iout1 = 0	10			mA
	Under Voltage Threshold			0.6		V
	Line Regulation			0.5		%
	Load Regulation			1		%
I_{FB2}	FB2 Leakage				150	nA

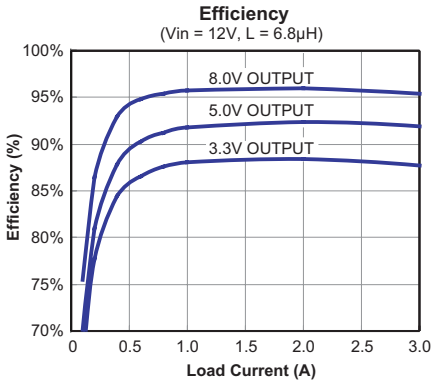
Note:

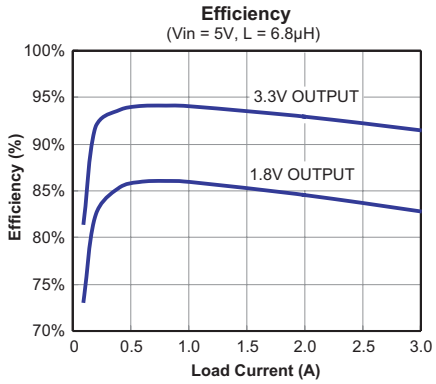
2. Specification in **BOLD** indicate an ambient temperature range of -40°C to +85°C. These specifications are guaranteed by design.

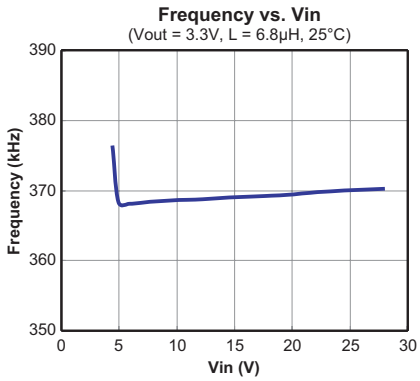
Typical Performance Characteristics

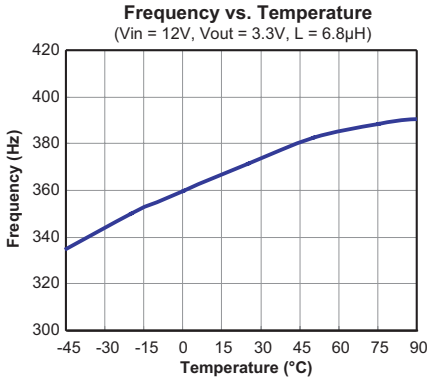
Circuit of Figure 1. T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V unless otherwise specified.

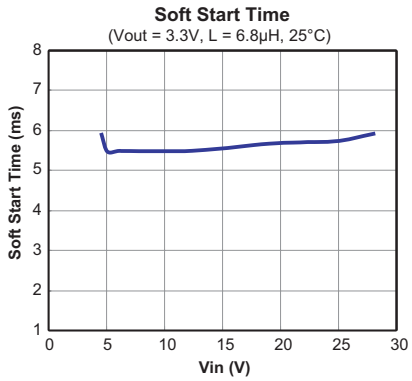


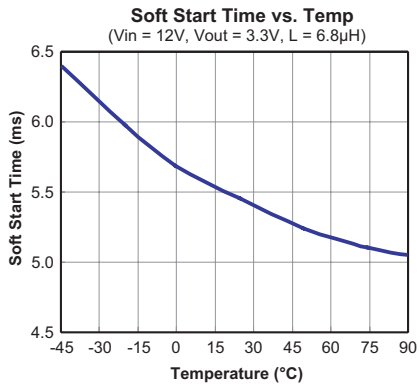


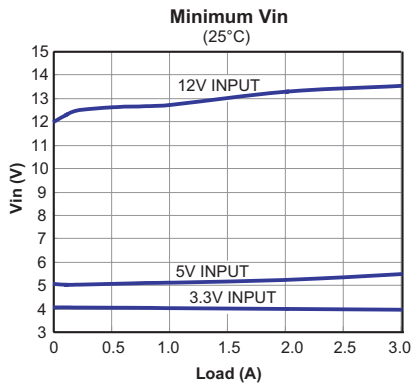


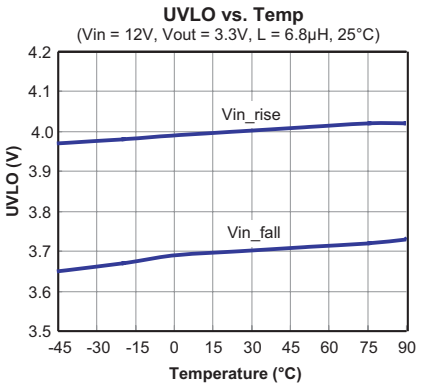


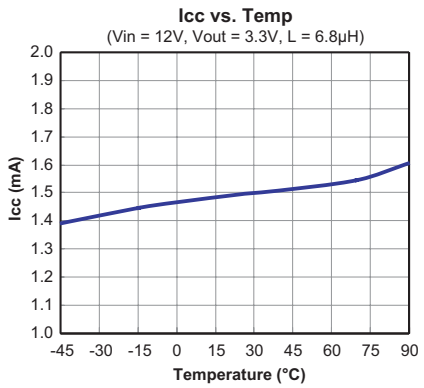


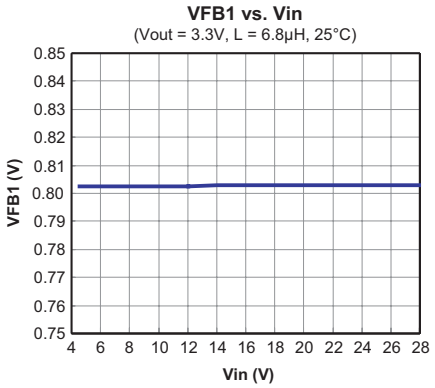


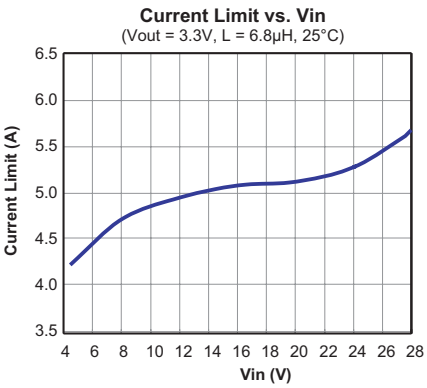








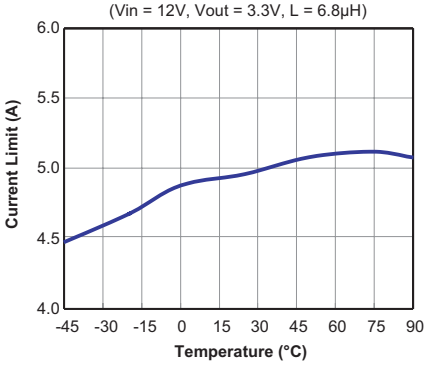




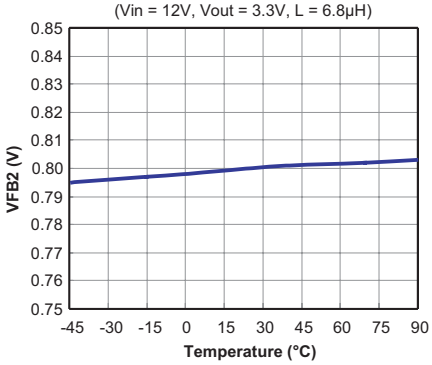
Typical Performance Characteristics (Continued)

Circuit of Figure 1. T_A = 25°C, V_{IN} = V_{EN} = 12V, V_{OUT} = 3.3V unless otherwise specified.

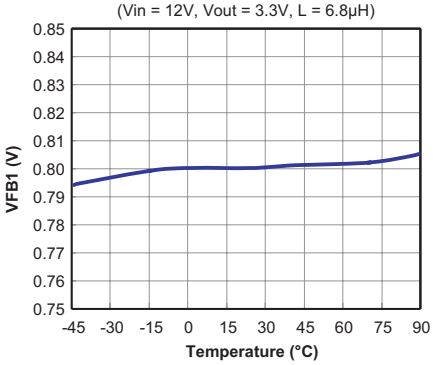
Current Limit vs. Temp
(Vin = 12V, Vout = 3.3V, L = 6.8µH)



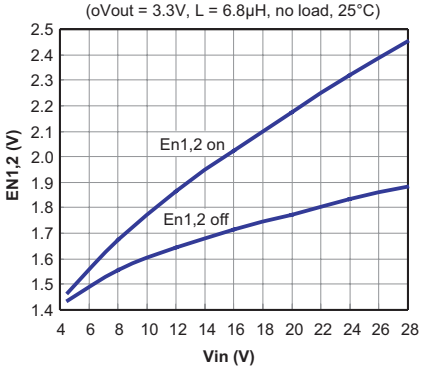
VFB2 vs. Temp
(Vin = 12V, Vout = 3.3V, L = 6.8µH)



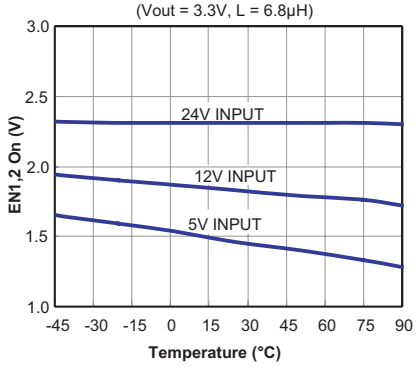
VFB1 vs. Temp
(Vin = 12V, Vout = 3.3V, L = 6.8µH)



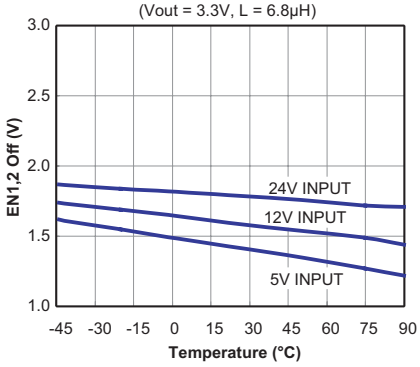
EN1,2 vs. Vin
(oVout = 3.3V, L = 6.8µH, no load, 25°C)



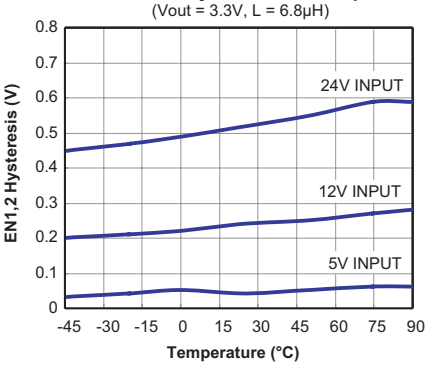
EN1,2 On vs. Temp
(Vout = 3.3V, L = 6.8µH)



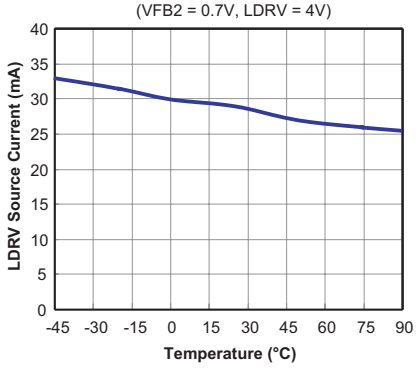
EN1,2 Off vs. Temp
(Vout = 3.3V, L = 6.8µH)



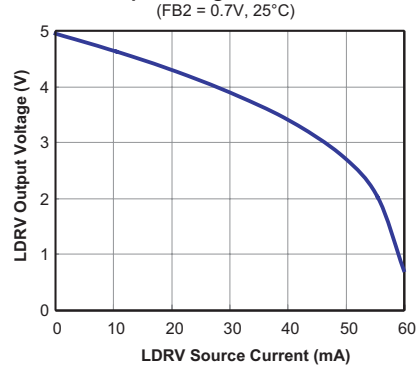
EN1,2 Hysteresis vs Temp
(Vout = 3.3V, L = 6.8µH)

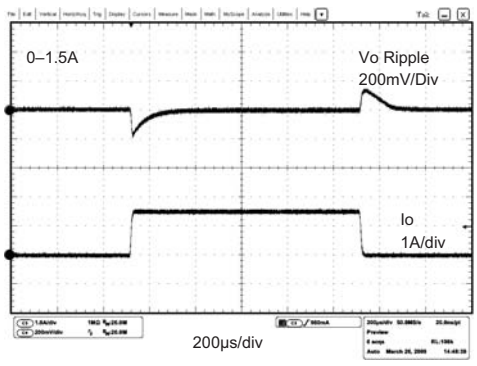


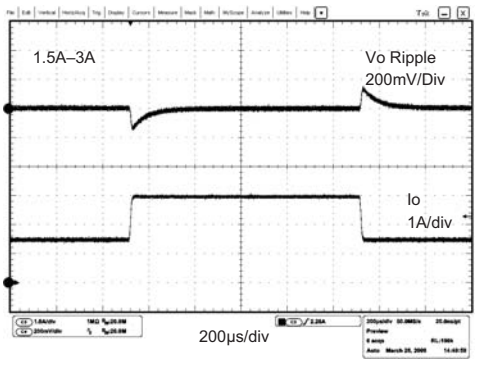
LDRV Source Current vs. Temp
(VFB2 = 0.7V, LDRV = 4V)



LDRV Output Voltage vs. Source Current
(FB2 = 0.7V, 25°C)







Detailed Description

The AOZ1214 is a current-mode step down regulator with integrated high side NMOS switch. It operates from a 4.5V to 28V input voltage range and supplies up to 3A of load current. The duty cycle can be adjusted from 5% to 85% allowing a wide range of output voltage. Features include independent enable control for buck and linear regulator, Power-On Reset, input under voltage lockout, fixed internal soft-start and thermal shut down. The linear regulator controller is designed to drive an external NPN power transistor or an N channel power MOSFET to provide up to 1A of current to an auxiliary load.

The AOZ1214 is available in 4x3 DFN-12 package.

Enable and Soft Start

The AOZ1214 has independent internal soft start feature to limit buck and LDO in-rush current and ensure the output voltage ramps up smoothly to regulation voltage. When the input voltage rises to 4.0V and voltage on EN1, EN2 pin is HIGH, the soft start processes of buck and linear regulator independently begin. In each soft start process, the buck or linear regulator output voltage is ramped to regulation voltage in typically 6ms. The 6ms soft start time is set internally.

Connect the EN1, EN2 pin to VIN if enable function is not used. Pull EN1 and EN2 to ground will disable the buck and linear regulator independently. Do not leave them open. The voltage on EN1, EN2 pin must be above 2.5V to active. When voltage on EN1, EN2 pin falls below 0.6V, the buck and linear regulator is disabled independently. If an application circuit requires the AOZ1214 buck or linear regulator to be disabled, an open drain or open collector circuit should be used to interface to EN1 or EN2 pin.

Steady-State Operation

Under steady-state conditions, the converter operates in fixed frequency and Continuous-Conduction Mode (CCM).

The AOZ1214 integrates an internal N-MOSFET as the high-side switch. Inductor current is sensed by amplifying the voltage drop across the drain to source of the high side power MOSFET. Since the N-MOSFET requires a gate voltage higher than the input voltage, a boost capacitor connected between LX pin and BST pin drives the gate. The boost capacitor is charged while LX is low. An internal 10 ohm switch from LX to PGND is used to insure that LX is pulled to PGND even in the light load. Output voltage is divided down by the external voltage divider at the FB pin. The difference of the FB pin voltage and reference is amplified by the internal trans-conductance error amplifier. The error voltage, which shows on the COMP pin, is compared against the current signal, which is sum of inductor current signal and ramp compensation signal, at PWM comparator input. If the current signal is less than the error voltage, the internal high-side switch is on. The inductor current flows from the input through the inductor to the output. When the current signal exceeds the error voltage, the high-side switch is off. The inductor current is freewheeling through the Schottky diode to output.

Switching Frequency

The AOZ1214 switching frequency is fixed and set by an internal oscillator. The switching frequency is set 370 kHz.

Output Voltage Programming

Output voltage can be set by feeding back the output to the FB pin with a resistor divider network. In the application circuit shown in Figure 1. The resistor divider network includes R_1 and R_2. Usually, a design is started by picking a fixed R_2 value and calculating the required R_1 with equation below.

$$V_{OUT1} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Some standard value of R_1, R_2 for most commonly used output voltage values are listed in Table 1.

Table 1.

Vo (V)	R_1 (kΩ)	R_2 (kΩ)
0.8	1.0	Open
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	31.6	10
5.0	52.3	10
12.0	140	10

The combination of R1 and R2 should be large enough to avoid drawing excessive current from the output, which will cause power loss.

Protection Features

The AOZ1214 has multiple protection features to prevent system circuit damage under abnormal conditions.

Over Current Protection (OCP)

The sensed inductor current signal is also used for over current protection. Since the AOZ1214 employs peak current mode control, the COMP pin voltage is proportional to the peak inductor current. The COMP pin voltage is limited to be between 0.4V and 2.5V internally. The peak inductor current is automatically limited cycle by cycle.

The cycle by cycle current limit threshold is internally set. When the load current reaches the current limit threshold, the cycle by cycle current limit circuit turns off the high side switch immediately to terminate the current duty cycle. The inductor current stop rising. The cycle by cycle current limit protection directly limits inductor peak current. The average inductor current is also limited due to the limitation on peak inductor current. When cycle by cycle current limit circuit is triggered, the output voltage drops as the duty cycle decreasing.

The AOZ1214 has internal short circuit protection to protect itself from catastrophic failure under output short circuit conditions. The FB pin voltage is proportional to the output voltage. Whenever FB pin voltage is below 0.3V, the short circuit protection circuit is triggered. To prevent current limit running away, when comp pin voltage is higher than 2.1V, the short circuit protection is also triggered. Before short protection is triggered, there is about 1 ms blank time to prevent false trigger caused by glitch or noise. The converter will start up via a soft start once the short circuit condition disappears.

Power-On Reset (POR)

A power-on reset circuit monitors the input voltage. When the input voltage exceeds 4.0V, the converter starts operation. When input voltage falls below 3.7V, the converter will stop switching.

Linear Regulator

The AOZ1214 contains an error amplifier which can be configured as a linear regulator controller. By adding an external follower (NPN or NMOS) and divider resistors as shown in Figure 1, the FB2 and LDRV pins can be configured as a controller for a Low Dropout Regulator.

The LDRV pin source capability come from LDO inside which is capable more than 10mA of base current to the external NPN transistor.

The FB2 voltage is monitored by an Under Voltage Protection circuit, which shutdown LDRV output when FB2 voltage is under 0.6V.

Thermal Protection

An internal temperature sensor monitors the junction temperature. It shuts down the internal control circuit and high side NMOS if the junction temperature exceeds 145ºC. The regulator will restart automatically under the control of soft-start circuit when the junction temperature decreases to 100ºC.

Application Information

The basic AOZ1214 application circuit is shown in Figure 1. Component selection is explained below.

Buck Regulator Design

Input Capacitor

The input capacitor (C_1 in Figure 1) must be connected to the V_{IN} pin and GND pin of the AOZ1214 to maintain steady input voltage and filter out the pulsing input current. The voltage rating of input capacitor must be greater than maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}}\left(1 - \frac{V_O}{V_{IN}}\right)}$$

if let *m* equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relationship between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 2 below. It can be seen that when V_O is half of V_{IN}, C_{IN} is under the worst current stress. The worst current stress on C_{IN} is 0.5 x I_O.

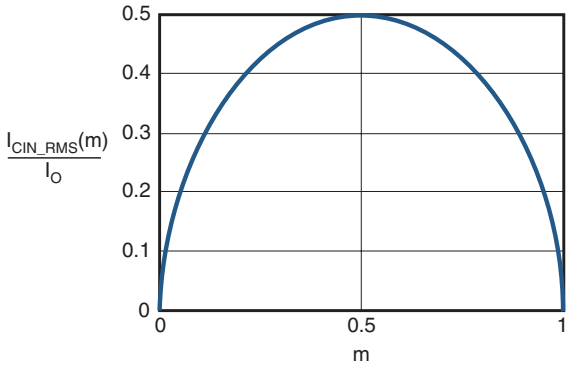


Figure 2. I_{CIN} vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have current rating higher than I_{CIN_RMS} at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufactures is based on certain amount of life time. Further de-rating may be necessary for practical design requirement.

Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is,

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through inductor and switches, which results in less conduction loss.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It can be calculated by the equation below:

$$\Delta V_O = \Delta I_L \times \left(ESR_{CO} + \frac{1}{8 \times f \times C_O}\right)$$

where;

C_O is output capacitor value and

ESR_{CO} is the Equivalent Series Resistor of output capacitor.

When low ESR ceramic capacitor is used as output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \left(\frac{1}{8 \times f \times C_O}\right)$$

If the impedance of ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type of ceramic, or other low ESR tantalum capacitor or aluminum electrolytic capacitor may also be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak to peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

Schottky Diode Selection

The external freewheeling diode supplies the current to the inductor when the high side NMOS switch is off. To reduce the losses due to the forward voltage drop and recovery of diode, Schottky diode is recommended to use. The maximum reverse voltage rating of the chosen Schottky diode should be greater than the maximum input voltage and size for average forward current in normal condition. Average forward current can be calculated from:

$$I_{D\_AVE} = \frac{I_O}{V_{IN}}(V_{IN} - V_{OUT})$$

Loop Compensation

The AOZ1214 employs peak current mode control for easy use and fast transient response. Peak current mode control eliminates the double pole effect of the output L&C filter. It greatly simplifies the compensation loop design.

With peak current mode control, the buck power stage can be simplified to be a one-pole and one-zero system in frequency domain. The pole is dominant pole and can be calculated by:

$$f_{p1} = \frac{1}{2\pi \times C_O \times R_L}$$

The zero is a ESR zero due to output capacitor and its ESR. It is can be calculated by:

$$f_{Z1} = \frac{1}{2\pi \times C_O \times ESR_{CO}}$$

where;

C_O is the output filter capacitor,

R_L is load resistor value, and

ESR_{CO} is the equivalent series resistance of output capacitor.

The compensation design is actually to shape the converter close loop transfer function to get desired gain and phase. Several different types of compensation network can be used for AOZ1214. For most cases, a series capacitor and resistor network connected to the COMP pin sets the pole-zero and is adequate for a stable high-bandwidth control loop.

In the AOZ1214, FB pin and COMP pin are the inverting input and the output of internal transconductance error amplifier. A series R and C compensation network connected to COMP provides one pole and one zero. The pole is:

$$f_{P2} = \frac{G_{EA}}{2\pi \times C_C \times G_{VEA}}$$

where;

G_{EA} is the error amplifier transconductance, which is 200 x 10^{-6} A/V,

G_{VEA} is the error amplifier voltage gain, which is 500 V/V, and

C_C is the compensation capacitor.

The zero given by the external compensation network, capacitor C_C and resistor R_C, is located at:

$$f_{Z2} = \frac{1}{2\pi \times C_C \times R_C}$$

To design the compensation circuit, a target crossover frequency f_C for close loop must be selected. The system crossover frequency is where control loop has unity gain. The crossover frequency is also called the converter bandwidth. Generally a higher bandwidth means faster response to load transient. However, the bandwidth should not be too high due to system stability concern. When designing the compensation loop, converter stability under all line and load condition must be considered.

Usually, it is recommended to set the bandwidth to be less than 1/10 of switching frequency. It is recommended to choose a crossover frequency less than 30 kHz.

$$f_C = 30kHz$$

The strategy for choosing R_C and C_C is to set the cross over frequency with R_C and set the compensator zero with C_C. Using selected crossover frequency, f_C, to calculate R_C:

$$R_C = f_C \times \frac{V_O}{V_{FB}} \times \frac{2\pi \times C_O}{G_{EA} \times G_{CS}}$$

where;o

f_C is desired crossover frequency,

V_{FB} is 0.8V,

G_{EA} is the error amplifier transconductance, which is $200x10^{-6}$ A/V, and

G_{CS} is the current sense circuit transconductance, which is 5.64 A/V.

The compensation capacitor C_C and resistor R_C together make a zero. This zero is put somewhere close to the dominate pole f_{p1} but lower than 1/5 of selected crossover frequency. C_C can is selected by:

$$C_C = \frac{1.5}{2\pi \times R_C \times f_{p1}}$$

Equation above can also be simplified to:

$$C_C = \frac{C_O \times R_L}{R_C}$$

Table 2. Recommended Parameters

V_{in}	V_O		
	1.2V	**3.3V**	**5V**
12V	L = 1.5µH–3.3µH R_C = 10KΩ C_C = 6.8nF	L = 4.7µH–10µH R_C = 30KΩ C_C = 2.2nF	L = 6.8µH–15µH R_C = 30KΩ C_C = 3.3nF
20V	L = 1.5µH R_C = 10KΩ C_C = 6.8nF	L = 4.7µH–10µH R_C = 30KΩ C_C = 2.2nF	L = 6.8uH–15µH R_C = 30KΩ C_C = 3.3nF

An easy-to-use application software which helps to design and simulate the compensation loop can be found at www.aosmd.com.

Linear Regulator Design

Adjustable Output Voltage

The output voltage can be set by feeding back the output to FB2 pin with a resistor divider network. In the application circuit shown in Figure 1. The linear regulator output voltage can be obtained using the following equation:

$$V_{OUT2} = 0.8 \times \left(1 + \frac{R3}{R4}\right)$$

R4 should be less than 10 kohm to avoid bias current errors.

External NPN Pass Transistor or MOSFET

Both Transistor and MOSFET can be used as an external follower. Some cautions must be noticed:

1. The transistor and MOSFET should be able to supply maximum operating current for the linear regulator supply.
2. DC current gain h_{FE} must be large enough so that the pass transistor and supply the maximum load current with 30 mA with base current. However, too big h_{FE} may cause the LDO sensitive to current noise, and a compromised DC current gain transistor should be selected.
3. The total power dissipation should not be higher than the rated value.
4. Comparing with transistor, MOSFET has lower dropout voltage which is $R_{DS(ON)}$ times the output current. But the minimum input voltage will increase to V_O plus V_{GS} while transistor is V_O plus V_{BE}.

Linear Regulator Output Capacitor

The linear regulator requires using an output capacitor as part of the frequency compensation network, which affects the stability and high frequency response. The regulator has a finite band width. For high frequency transient loads, recovery from transient is determined by both output capacitor and the bandwidth of the regulator. A minimum output capacitor of 4.7 µF is recommended to prevent oscillations and provide good transient response.

The ESR value should be maintained in the range that determines the loop stability. When small signal ringing

occurs with ceramics due to insufficient ESR in low output voltage condition, adding ESR or increasing the capacitor value improves the stability and reduces the ringing. But too high ESR is also not suggested, which will cause the zero too big and the phase margin is not satisfied. High ESR also brings in high voltage ripple. The lower the output voltage is, the higher value ESR is needed. Basically, ESR between 0.02 ohm and 3 ohm can make sure the circuit stable.

Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, only if their capacitance and ESR meet the requirements.

Output Voltage Ripple

The LDO is designed to provide low output voltage noise while operating at any load. Because of the existence of stray inductance and capacitance, sometimes there could be a big ripple voltage in the output which is unexpected. The following tips could decrease the ripple voltage to a lower value:

1. Improve the PCB layout.

   Signal grounds should connect to AGND to insure the noise is small.

   Low side divider resistor connects to AGND directly.

   Keep sensitive signal trace such as FB2 pin, LDRV pin as short as possible, and far away from noise trace;
2. Adding a bypass capacitor from FB2 pin to AGND, which will lower the bandwidth of the loop. The impedance of the FB2 pin capacitor at the ripple frequency should be less than the value of R3.
3. Adding a resistor R_G between LDRV and base of transistor (gate of MOSFET), which can structure a RC filter with the capacitor of Base-Emitter to reduce the noise. As the increasing of R_G value, the noise getting smaller. Considering the power dispassion of the R_G, its value is often between 10 ohm and 100 ohm.
4. Increasing the capacitance of output capacitor or add the ESR of the output capacitor.
5. Change the pass transistor to a lower h_{FE} type (MOSFET to a lower g_{FS} type), thus the loop gain can be smaller as a source follower. But the h_{FE} and g_{FS} should be large enough to meet the output current requirement.

Thermal Management and Layout Consideration

In the AOZ1214 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the VIN pin, to the LX pins, to the filter inductor, to the output capacitor and load, and then return to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from inductor, to the output capacitors and load, to the GND pin of the AOZ1214, to the LX pins of the AZO1214. Current flows in the second loop when the low side diode is on.

In PCB layout, minimizing the two loops area reduces the noise of this circuit and improves efficiency. A ground plane is recommended to connect input capacitor, output capacitor, and GND pin of the AOZ1214.

In the AOZ1214 buck regulator circuit, the three major power dissipating components are the AOZ1214, external diode and output inductor. The total power dissipation of converter circuit can be measured by input power minus output power.

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of inductor can be approximately calculated by output current and DCR of inductor.

$$P_{inductor\_loss} = I_O^2 \times R_{inductor} \times 1.1$$

The power dissipation of diode is:

$$P_{diode\_loss} = I_O \times V_F \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The actual AOZ1214 junction temperature can be calculated with power dissipation in the AOZ1214 and thermal impedance from junction to ambient.

$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss}) \times \Theta_{JA} + T_{ambient}$$

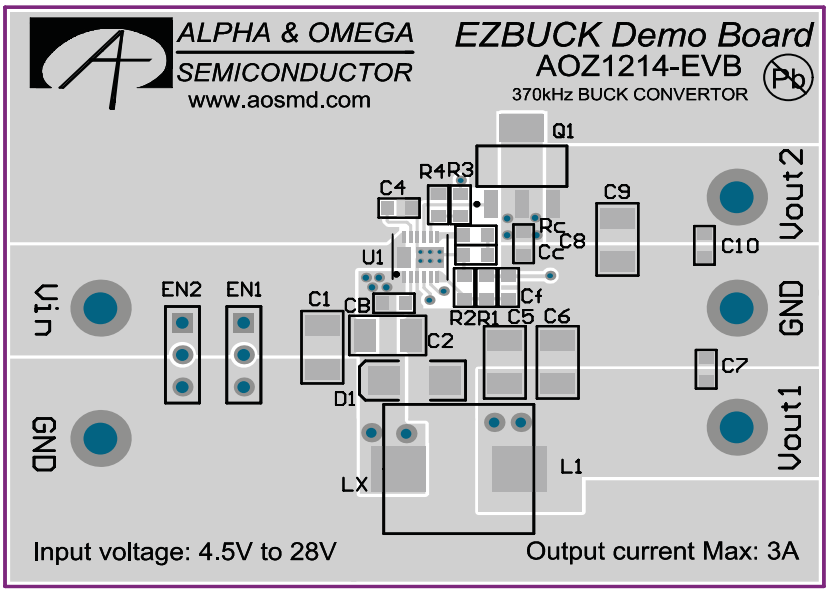
The maximum junction temperature of AOZ1214 is 145ºC, which limits the maximum load current capability.

The thermal performance of the AOZ1214 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

Several layout tips are listed below for the best electric and thermal performance. Figure 3 is the layout example.

1. Do not use thermal relief connection to the VIN and the GND pin. Pour a maximized copper area to the GND pin and the VIN pin to help thermal dissipation.
2. Input capacitor should be connected to the VIN pin and the GND pin as close as possible.
3. Make the current trace from LX pins to L to Co to the GND as short as possible.
4. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.
5. Keep sensitive signal trace such as trace connected with FB pin and COMP pin far away form the LX pins.

Top Side



Bottom Side

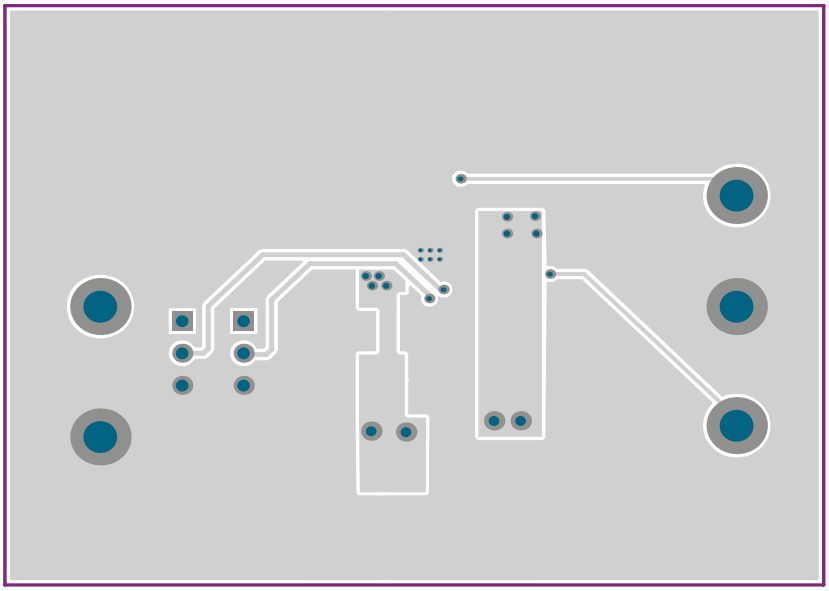
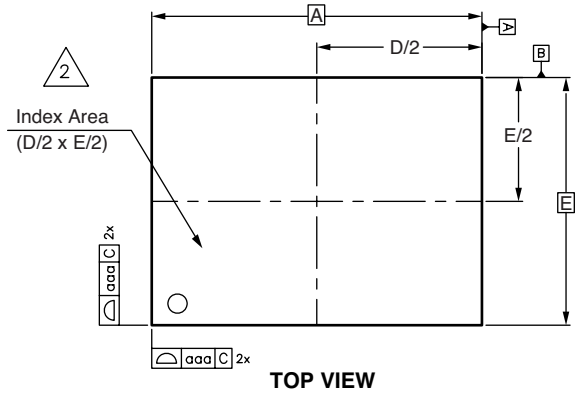
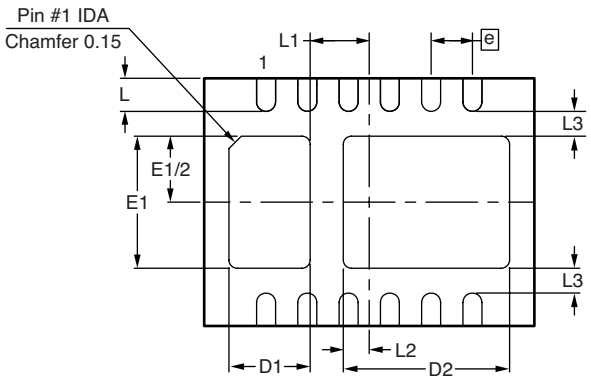


Figure 3. Layout Example for the AOZ1214

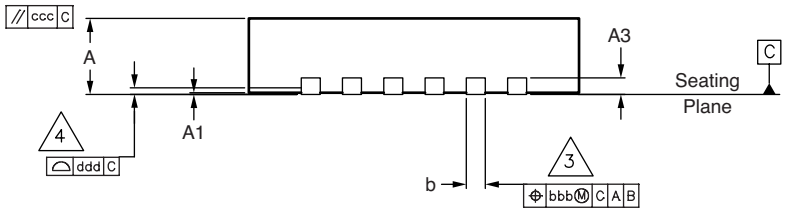
Package Dimensions, DFN 4x3, 12L



TOP VIEW

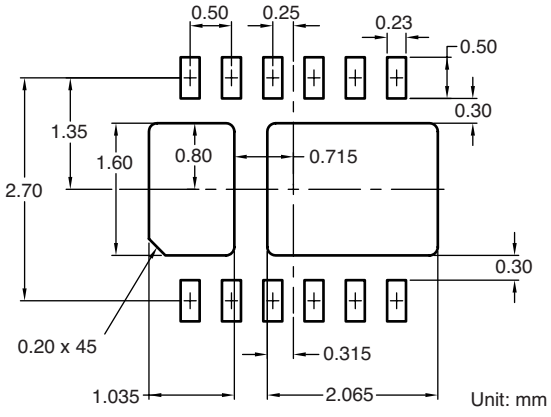


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.20	0.23	0.35
D		4.00 BSC	
D1	0.83	0.985	1.09
D2	1.86	2.015	2.12
E		3.00 BSC	
E1	1.45	1.60	1.70
e		0.50 BSC	
L	0.30	0.40	0.50
L1	0.61	0.715	0.82
L2	0.21	0.315	0.42
L3		0.30 REF.	
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.08	

Dimensions in inches

Symbols	Min.	Nom.	Max.
A	0.031	0.035	0.039
A1	0.000	0.001	0.002
A3		0.008 REF.	
b	0.008	0.009	0.014
D		0.157 BSC	
D1	0.033	0.039	0.043
D2	0.073	0.079	0.083
E		0.118 BSC	
E1	0.057	0.063	0.067
e		0.020 BSC	
L	0.012	0.016	0.020
L1	0.024	0.028	0.032
L2	0.008	0.012	0.017
L3		0.012 REF.	
aaa		0.006	
bbb		0.004	
ccc		0.004	
ddd		0.003	

Notes:

1. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

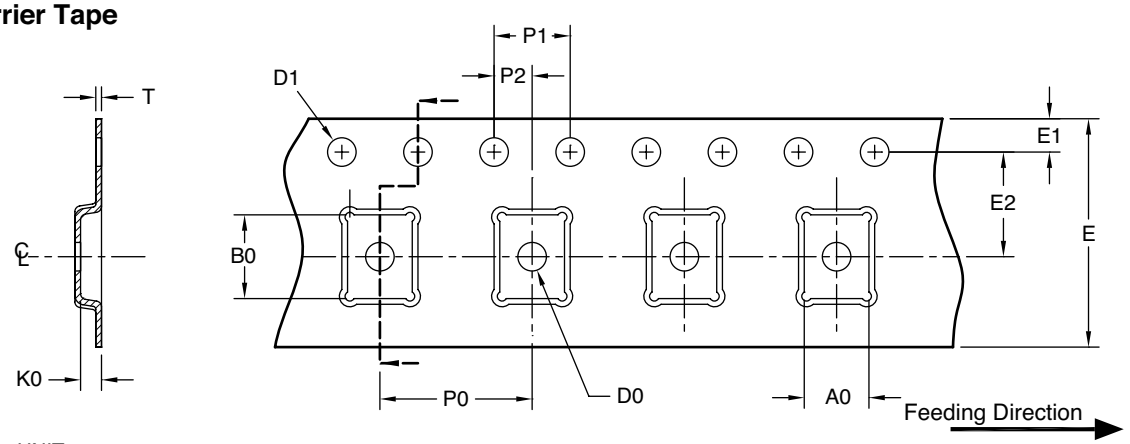
2. The location of the terminal #1 identifier and terminal numbering conforms to JEDEC publication 95 SPP-002.

3. Dimension b applied to metallized terminal and is measured between 0.20mm and 0.35mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, dimension b should not be measured in that radius area.

4. Coplanarity ddd applies to the terminals and all other bottom surface metallization.

Tape and Reel Dimensions, DFN 4x3

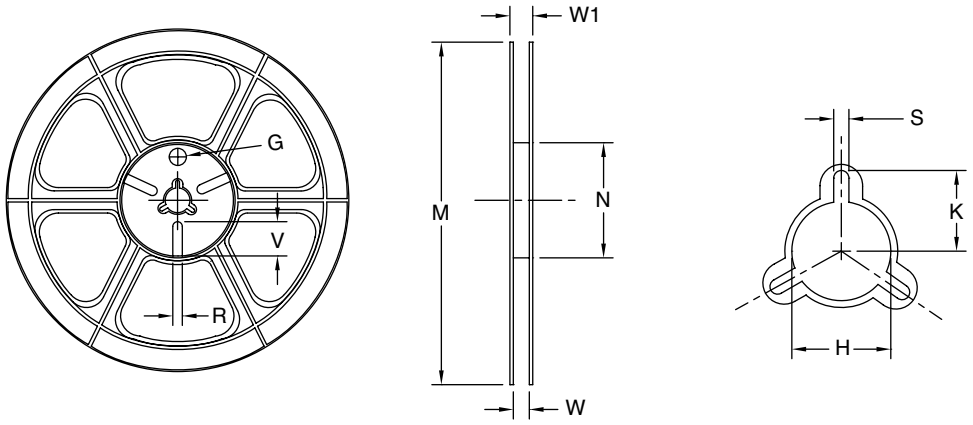
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 4 x 3 (12 mm)	3.40 ±0.10	4.40 ±0.10	1.10 ±0.10	1.50 Min.	1.50 +0.10/-0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.30 ±0.05

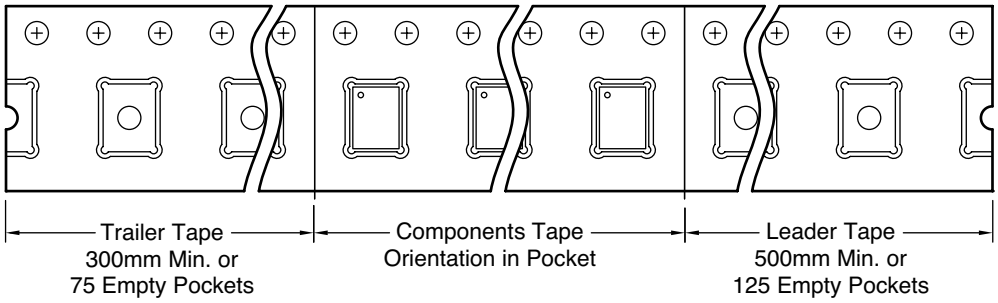
Reel



UNIT: mm

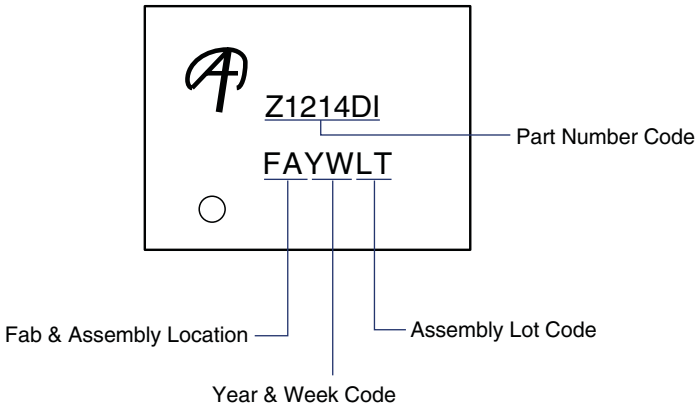
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0/-0	17.0 +2.6/-0	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	—	—	—

Leader / Trailer & Orientation



Part Marking

AOZ1214DI
(4 x 3 DFN-12)



This datasheet contains preliminary data; supplementary data may be published at a later date.
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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.