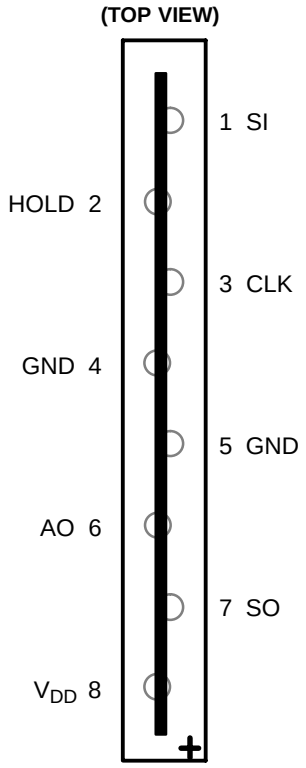
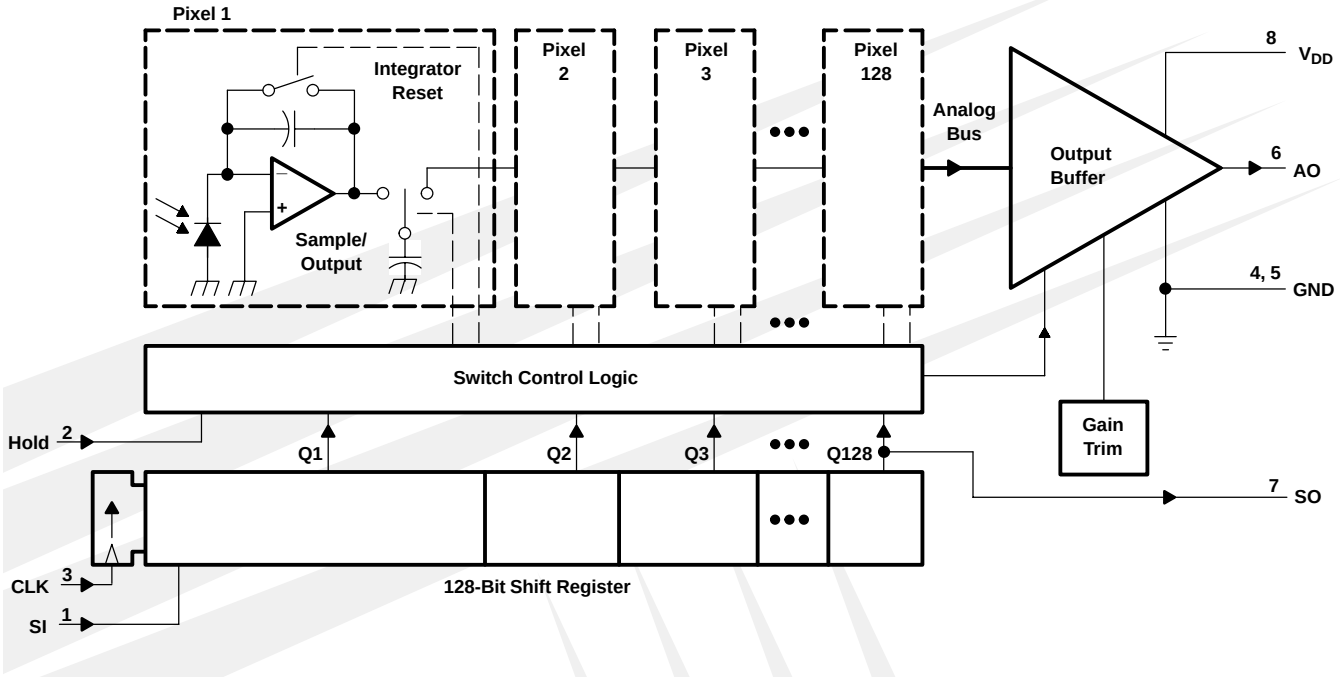
- **128 × 1 Sensor-Element Organization**
- **400 Dots-Per-Inch (DPI) Sensor Pitch**
- **High Linearity and Uniformity**
- **Wide Dynamic Range . . . 4000:1 (72 dB)**
- **Output Referenced to Ground**
- **Low Image Lag . . . 0.5% Typ**
- **Operation to 8 MHz**
- **Single 3-V to 5-V Supply**
- **Rail-to-Rail Output Swing (AO)**
- **No External Load Resistor Required**



Description

The TSL1401CS linear sensor array consists of a 128 × 1 array of photodiodes, associated charge amplifier circuitry, and a pixel data-hold function that provides simultaneous-integration start and stop times for all pixels. The pixels measure 63.5 µm (H) by 55.5 µm (W) with 63.5-µm center-to-center spacing and 8-µm spacing between pixels. Operation is simplified by internal control logic that requires only a serial-input (SI) signal and a clock.

Functional Block Diagram



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AO	6	Analog output
CLK	3	Clock. The clock controls charge transfer, pixel output, and reset.
GND	4, 5	Ground (substrate). All voltages are referenced to the substrate.
HOLD	2	Hold signal. HOLD freezes the result of a 128 pixel scan.
SI	1	Serial input. SI defines the start of the data-out sequence.
SO	7	Serial output. SO provides a signal to drive the SI input of another device for cascading or as an end-of-data indication.
V_{DD}	8	Supply voltage. Supply voltage for both analog and digital circuits.

Detailed Description

The sensor consists of 128 photodiodes arranged in a linear array. Light energy impinging on a photodiode generates photocurrent, which is integrated by the active integration circuitry associated with that pixel.

During the integration period, a sampling capacitor connects to the output of the integrator through an analog switch. The amount of charge accumulated at each pixel is directly proportional to the light intensity and the integration time.

The output and reset of the integrators is controlled by a 128-bit shift register and reset logic. An output cycle is initiated by clocking in a logic 1 on SI. For proper operation, after meeting the minimum hold time condition, SI must go low before the next rising edge of the clock. The signal called Hold is normally connected to SI. Then, the rising edge of SI causes a HOLD condition. This causes all 128 sampling capacitors to be disconnected from their respective integrators and starts an integrator reset period. As the SI pulse is clocked through the shift register, the charge stored on the sampling capacitors is sequentially connected to a charge-coupled output amplifier that generates a voltage on analog output AO. Simultaneously, during the first 18 clock cycles, all pixel integrators are reset, and the next integration cycle begins on the 19th clock. On the 129th clock rising edge, the SI pulse is clocked out of the shift register and the analog output AO assumes a high impedance state. Note that this 129th clock pulse is required to terminate the output of the 128th pixel, and return the internal logic to a known state. A subsequent SI pulse may be presented as early as the 130th clock pulse, thereby initiating another pixel output cycle.

AO is an op amp-type output that does not require an external pull-down resistor. This design allows a rail-to-rail output voltage swing. With V_{DD} = 5 V, the output is nominally 0 V for no light input, 2 V for normal white level, and 4.8 V for saturation light level. When the device is not in the output phase, AO is in a high-impedance state.

The voltage developed at analog output (AO) is given by:

$$V_{out} = V_{drk} + (R_e)(E_e)(t_{int})$$

where:

- V_{out} is the analog output voltage for white condition
- V_{drk} is the analog output voltage for dark condition
- R_e is the device responsivity for a given wavelength of light given in V/(μJ/cm^2)
- E_e is the incident irradiance in μW/cm^2
- t_{int} is integration time in seconds

A 0.1 μF bypass capacitor should be connected between V_{DD} and ground as close as possible to the device.

The TSL1401CS is intended for use in a wide variety of applications, including: image scanning, mark and code reading, optical character recognition (OCR) and contact imaging, edge detection and positioning, and optical linear and rotary encoding.

Absolute Maximum Ratings†

Supply voltage range, V_{DD} . . . . . -0.3 V to 6 V
Input voltage range, V_I . . . . . - 0.3 V to V_{DD} + 0.3V
Input clamp current, I_{IK} ($V_I < 0$) or ($V_I > V_{DD}$) . . . . . - 20 mA to 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$) . . . . . - 25 mA to 25 mA
Voltage range applied to any output in the high impedance or power-off state, V_O . . . - 0.3 V to V_{DD} + 0.3 V
Continuous output current, I_O (V_O = 0 to V_{DD}) . . . . . - 25 mA to 25 mA
Continuous current through V_{DD} or GND . . . . . - 40 mA to 40 mA
Analog output current range, I_O . . . . . - 25 mA to 25 mA
Maximum light exposure at 638 nm . . . . . 5 mJ/cm^2
Operating free-air temperature range, T_A . . . . . -40 °C to 100°C
Storage temperature range, T_{stg} . . . . . - 40°C to 100°C
Solder reflow temperature, case exposed for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions (see Figure 1 and Figure 2)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	5	5.5	V
Input voltage, V_I	0		V_{DD}	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	0		0.8	V
Wavelength of light source, λ	400		1000	nm
Clock frequency, f_{clock}	5		8000	kHz
Sensor integration time, t_{int} (see Note 1)	0.016		100	ms
Setup time, serial input, $t_{su(SI)}$	20			ns
Hold time, serial input, $t_{h(SI)}$ (see Note 2)	0			ns
Operating free-air temperature, T_A	-40		85	°C

NOTES: 1. This time does not include the 18 clock cycles for setup, which would consume an additional 0.002 mS of device integrate and read time.
2. SI must go low before the rising edge of the next clock pulse.

Electrical Characteristics at f_{clock} = 1 MHz, V_{DD} = 5 V, T_A = 25°C, λ_p = 640 nm, t_{int} = 5 ms, R_L = 330 Ω, E_e = 11 μW/cm² (unless otherwise noted) (see Note 3 and Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{out}	Analog output voltage (white, average over 128 pixels)		1.6	2	2.4	V
V_{drk}	Analog output voltage (dark, average over 128 pixels)	E_e = 0	0	0.1	0.2	V
PRNU	Pixel response nonuniformity	See Note 5		±4%	±10%	
	Nonlinearity of analog output voltage	See Note 6		±0.4%		FS
	Output noise voltage	See Note 7		1		mVrms
R_e	Responsivity	See Note 8	25	35	44	V/(μJ/cm²)
V_{sat}	Analog output saturation voltage	V_{DD} = 5 V, R_L = 330 Ω	4.5	4.8		V
		V_{DD} = 3 V, R_L = 330 Ω	2.5	2.8		
SE	Saturation exposure	V_{DD} = 5 V, See Note 9		136		nJ/cm²
		V_{DD} = 3 V, See Note 9		78		
DSNU	Dark signal nonuniformity	All pixels, E_e = 0 See Note 10		0.02	0.05	V
IL	Image lag	See Note 11		0.5%		
I_{DD}	Supply current	V_{DD} = 5 V, E_e = 0		2.8	4.5	mA
		V_{DD} = 3 V, E_e = 0		2.6	4.5	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input current	$V_I = V_{DD}$			1	μA
I_{IL}	Low-level input current	V_I = 0			1	μA
C_i	Input capacitance			5		pF

NOTES: 3. The array is uniformly illuminated with a diffused LED source having a peak wavelength of 640 nm.
4. All measurements made with a 0.1 μF capacitor connected between V_{DD} and ground.
5. PRNU is the maximum difference between the voltage from any single pixel and the average output voltage from all pixels of the device under test when the array is uniformly illuminated at the white irradiance level. PRNU includes DSNU.
6. Nonlinearity is defined as the maximum deviation from a best-fit straight line over the dark-to-white irradiance levels, as a percent of analog output voltage (white).
7. RMS noise is the standard deviation of a single-pixel output under constant illumination as observed over a 5-second period.
8. $R_{e(min)} = [V_{out(min)} - V_{drk(max)}] \div (E_e \times t_{int})$
9. $SE(min) = [V_{sat(min)} - V_{drk(min)}] \times \langle E_e \times t_{int}) \div [V_{out(max)} - V_{drk(min)}]$
10. DSNU is the difference between the maximum and minimum output voltage for all pixels in the absence of illumination.
11. Image lag is a residual signal left in a pixel from a previous exposure. It is defined as a percent of white-level signal remaining after a pixel is exposed to a white condition followed by a dark condition:

$$IL = \frac{V_{out\ (IL)} - V_{drk}}{V_{out\ (white)} - V_{drk}} \times 100$$

Timing Requirements (see Figure 1 and Figure 2)

		MIN	NOM	MAX	UNIT
$t_{su(SI)}$	Setup time, serial input (see Note 12)	20			ns
$t_{h(SI)}$	Hold time, serial input (see Note 11 and Note 13)	0			ns
t_w	Pulse duration, clock high or low	50			ns
t_r, t_f	Input transition (rise and fall) time	0		500	ns

NOTES: 12. Input pulses have the following characteristics: t_r = 6 ns, t_f = 6 ns.
13. SI must go low before the rising edge of the next clock pulse.

Dynamic Characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 3 and 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_s	Analog output settling time to ±1%	R_L = 330 Ω, C_L = 10 pF		120		ns

TYPICAL CHARACTERISTICS

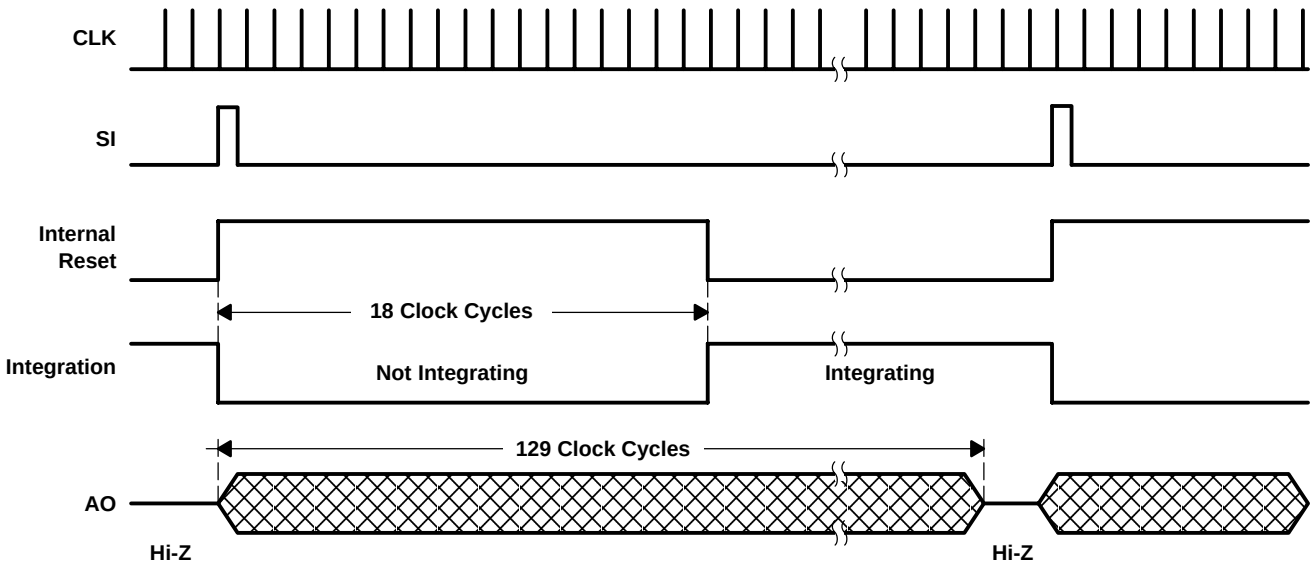


Figure 1. Timing Waveforms

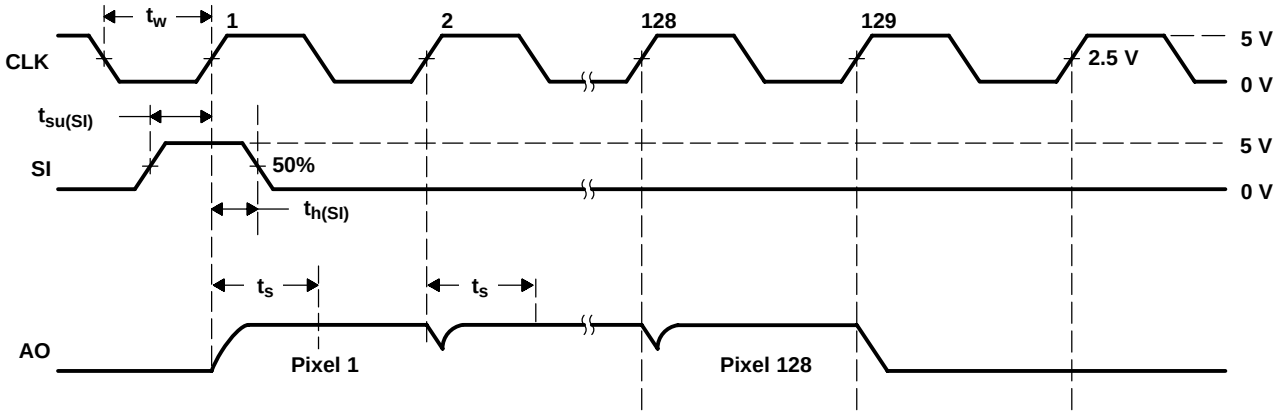


Figure 2. Operational Waveforms

TYPICAL CHARACTERISTICS

SETTLING TIME
vs.
LOAD

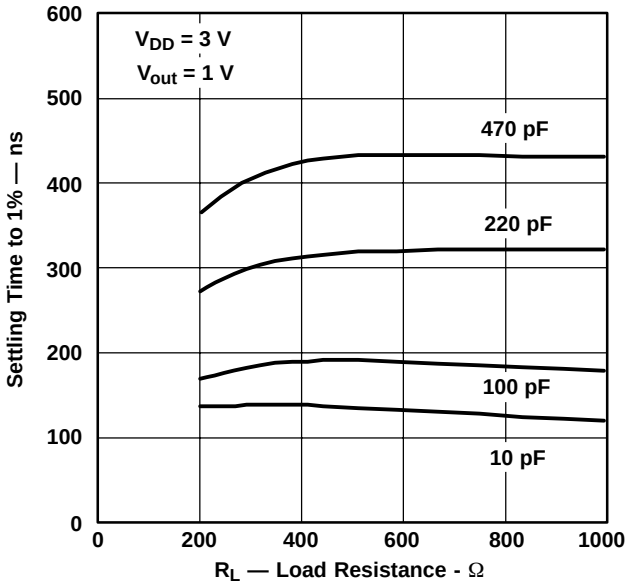


Figure 3

SETTLING TIME
vs.
LOAD

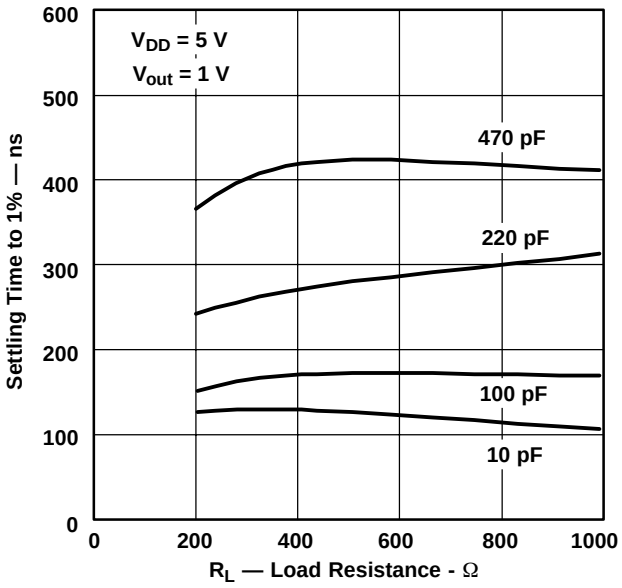


Figure 4

PHOTODIODE SPECTRAL RESPONSIVITY

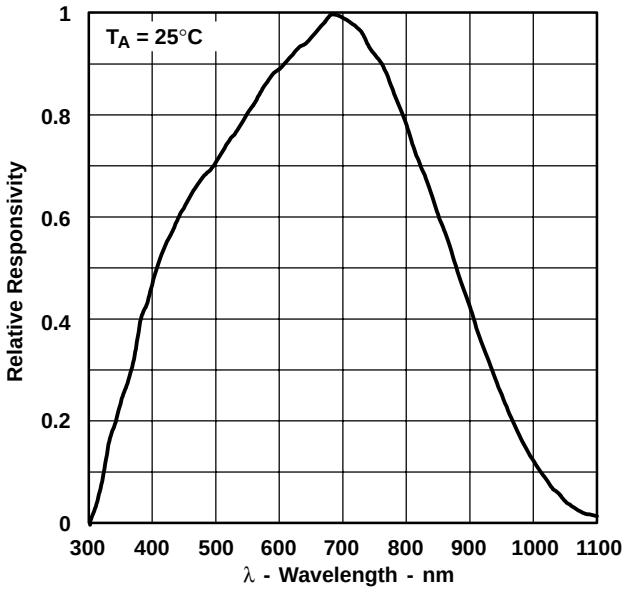


Figure 5

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

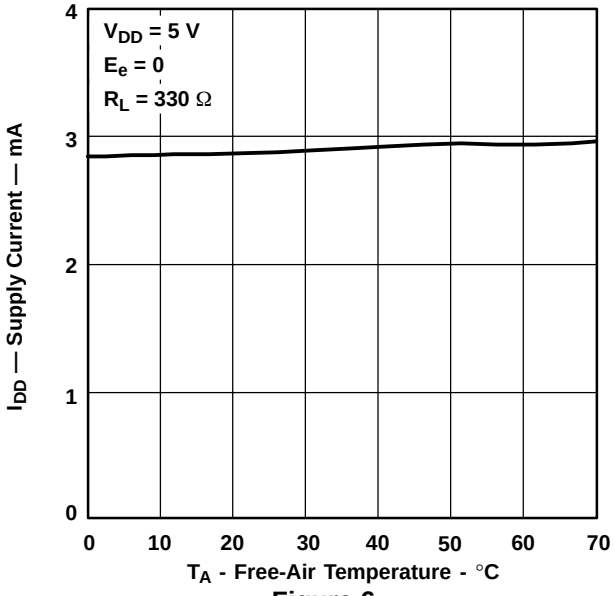


Figure 6

TYPICAL CHARACTERISTICS

WHITE OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

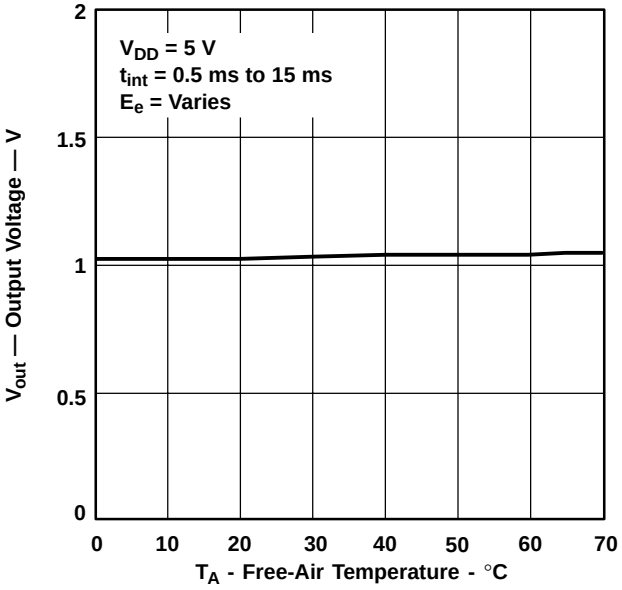


Figure 7

DARK OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

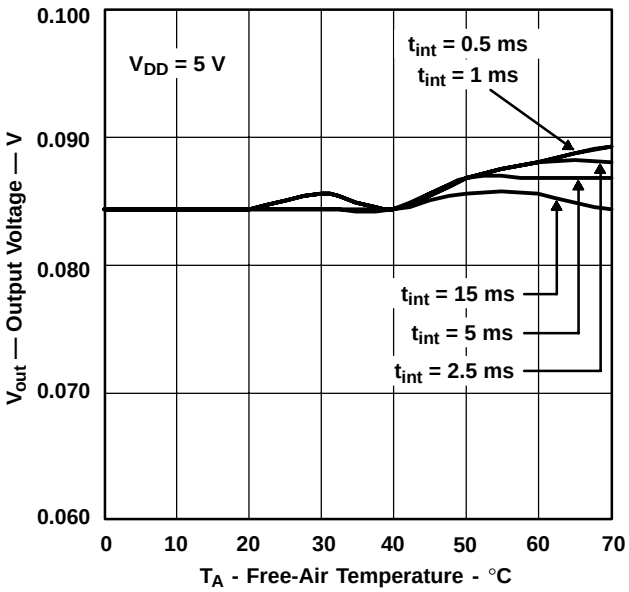


Figure 8

APPLICATION INFORMATION

A 0.1 μF bypass capacitor should be connected between V_{DD} and ground as close as possible to the device.

The HOLD pin on the device is normally connected to the SI pin in single-die operation. In multi-die operation of *n* die, the HOLD pin is used to provide a continuous scan across the *n* die. See Figure 9 for an example of this wiring configuration. Note that there is a single AO signal when used in this mode. Alternately, the individual die may be scanned all at once by connecting the individual SI and HOLD lines and reading the AO signals in parallel. See Figure 10 for an example of this wiring configuration.

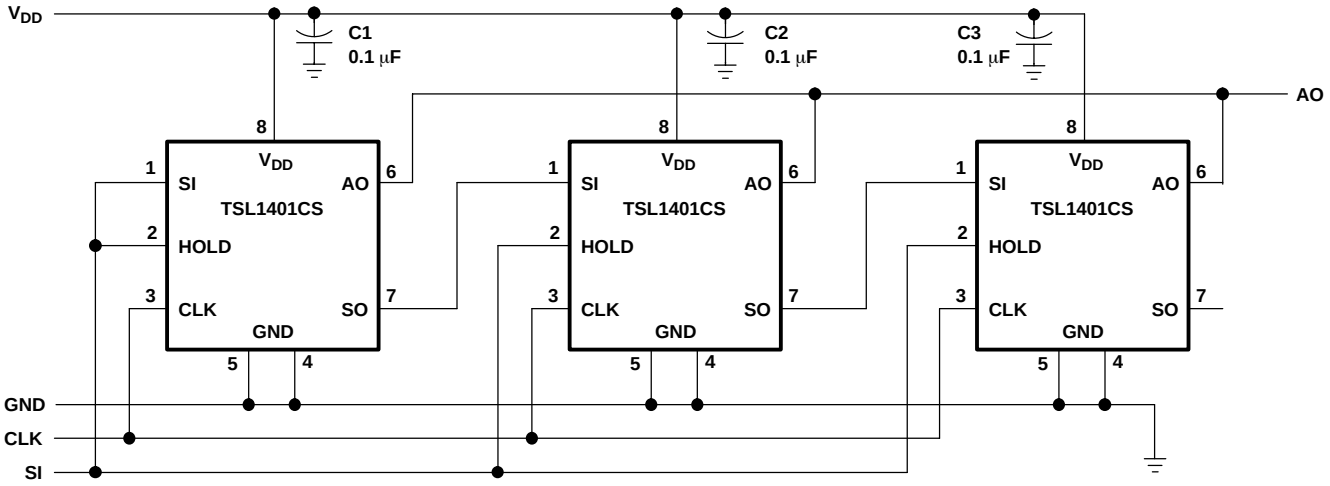


Figure 9. Multi-Die Continuous Scan

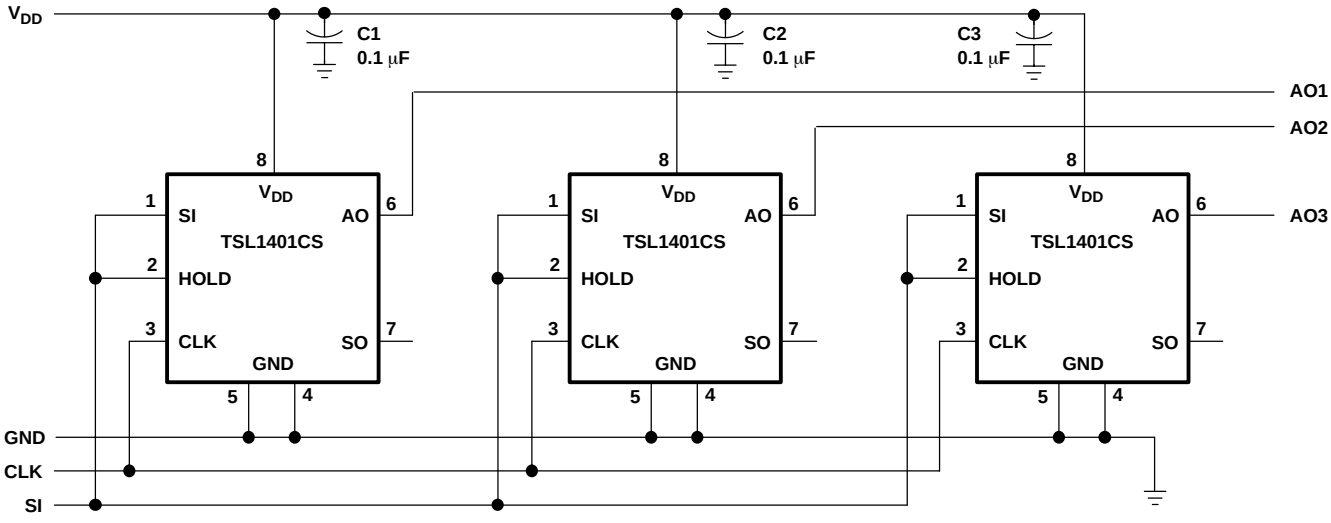
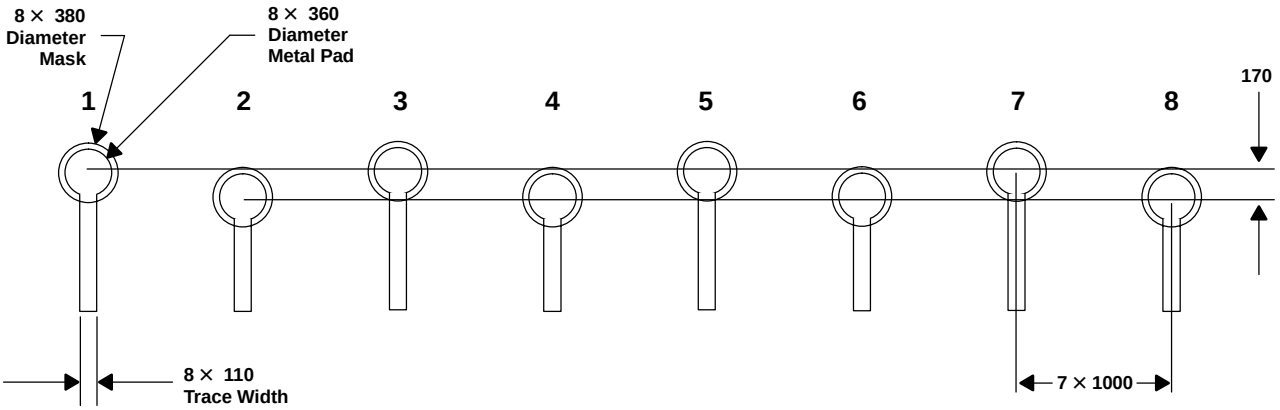


Figure 10. Multi-Die Individual Scan

APPLICATION INFORMATION

TOP **BOTTOM**

Figure 11. Device Pictorial

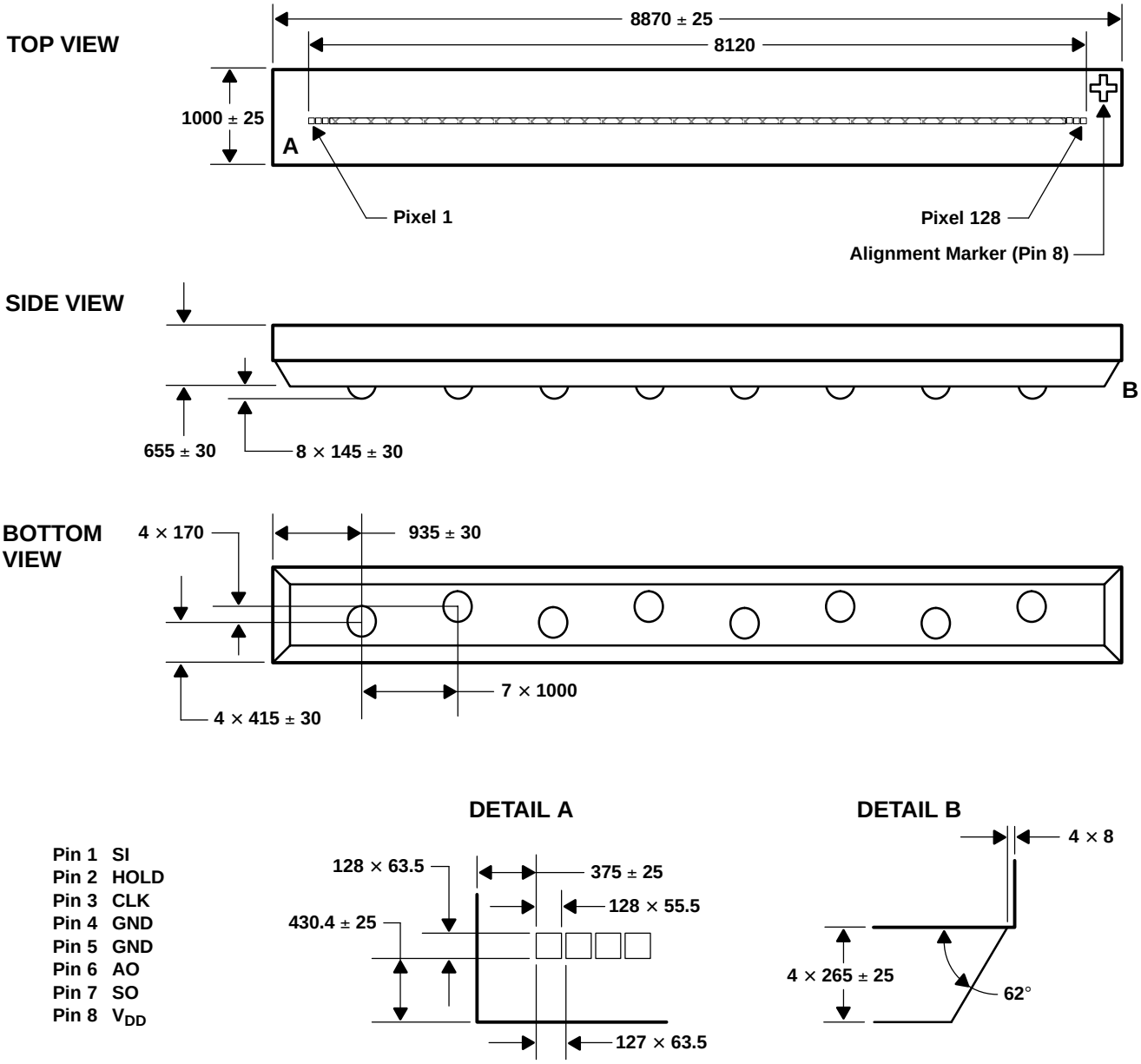


NOTES: A. All linear dimensions are in micrometers.
B. This drawing is subject to change without notice.

Figure 12. Suggested PCB Layout

MECHANICAL INFORMATION

The TSL1401CS is available in a solder bump linear array package, ready for surface mount manufacturing processes.

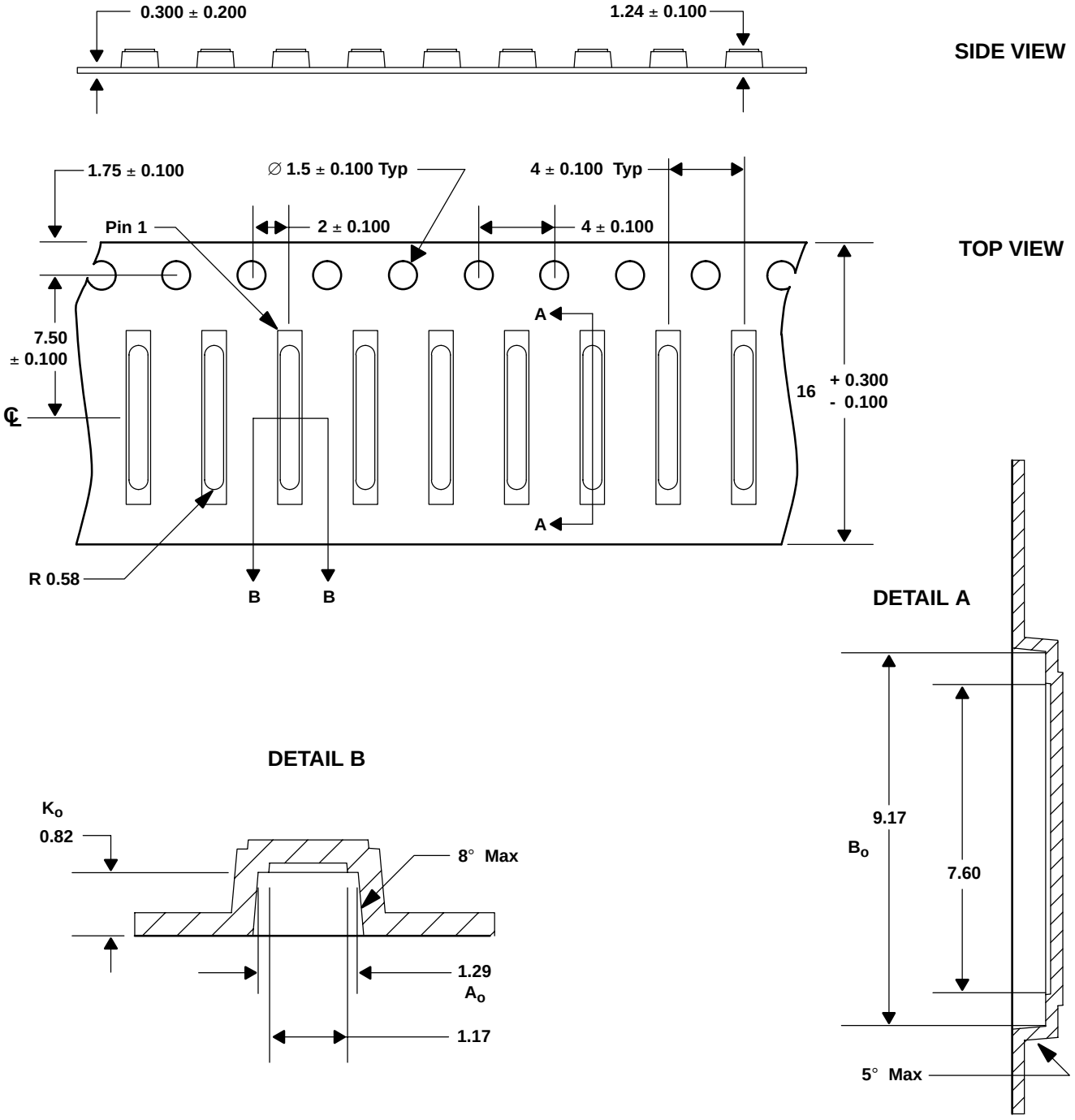


Pin 1	SI
Pin 2	HOLD
Pin 3	CLK
Pin 4	GND
Pin 5	GND
Pin 6	AO
Pin 7	SO
Pin 8	V_{DD}

NOTES: A. All linear dimensions are in micrometers.
B. Unless otherwise noted, all dimensions are ± 10.
C. This drawing is subject to change without notice.

Figure 13. Packaging Configuration

MECHANICAL INFORMATION



NOTES:
A. All linear dimensions are in millimeters.
B. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
C. Symbols on drawing A_o, B_o, and K_o are defined in ANSI EIA Standard 481-B 2001.
D. Each reel is 178 millimeters in diameter and contains 2800 parts.
E. TAOS packaging tape and reel conform to the requirements of EIA Standard 481-B.
F. This drawing is subject to change without notice.

Figure 14. TSL1401CS Carrier Tape

MANUFACTURING INFORMATION

This product has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The process, equipment, and materials used in these tests are detailed below.

Tooling Required

- Solder stencil (round aperture size 0.36 mm, stencil thickness of 152.4 μm)
- 20 × 20 frame for solder stencil

Process

1. Apply solder paste using stencil
2. Dispense adhesive dots
3. Place component
4. Reflow solder/cure
5. X-Ray verify

Placement of the TSL1401CS device onto the gold immersion substrate is accomplished using a standard surface mount manufacturing process. First, using the stencil with 0.36 mm square aperture, print solder paste onto the substrate. Next, dispense two 0.25 mm to 0.4 mm diameter dots of adhesive in opposing corners of the TSL1401CS mounting area. Machine place the TSL1401CS from the JEDEC waffle carrier onto the substrate. A suggested pick-up tool is the Siemens Vacuum Pickup tool nozzle number 912. This nozzle has a rubber tip with a diameter of approximately 0.75 mm. The part is picked up from the center of the body. Reflow the solder and cure the adhesive using the solder profile shown in Figure 15.

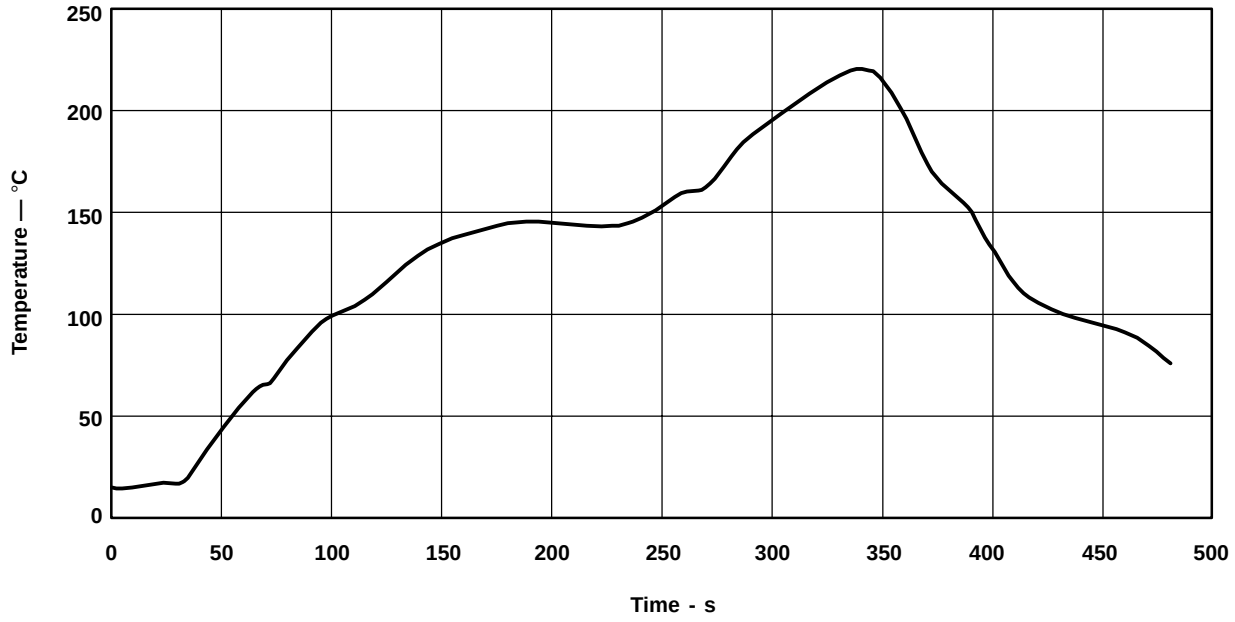


Figure 15. TSL1401CS Solder Profile

It is important to use a substrate that has an immersion plating surface. This may be immersion gold, silver, or white tin. Hot air solder leveled substrates (HASL) are not coplanar and should not be used.

MANUFACTURING INFORMATION

Qualified Equipment

- EKRA E5 — Stencil Printer
- ASYMTEC Century — Dispensing system
- SIEMENS F5 — Placement system
  - SIEMENS 912 — Vacuum Pickup Tool Nozzle
- VITRONICS 820 — Oven
- PHOENIX — Inspector X-Ray system

Qualified Materials

- OMG — Microbond solder paste
- Loctite 3621 — Adhesive

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