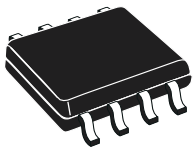
STS3C2F80

N-CHANNEL 80V - 0.069 Ω - 3A SO-8
P-CHANNEL 80V - 0.20 Ω - 2.3A SO-8
STripFET™ II POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STS3C2F80(N-Channel)	80 V	< 0.08 Ω	3 A
STS3C2F80(P-Channel)	80 V	< 0.25 Ω	2.3 A

- TYPICAL R_{DS}(on) (N-Channel) = 0.069 Ω
- TYPICAL R_{DS}(on) (P-Channel) = 0.20 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY



SO-8

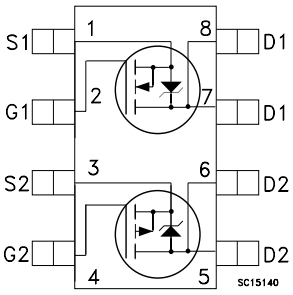
DESCRIPTION

This application specific Power MOSFET is the second generation of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC/DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN CELLULAR PHONES AND DISPLAY NEW GENERATION

INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STS3C2F80	S3C2F80	SO-8	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	N-CHANNEL	P-CHANNEL	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	80		V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	80		V
V_{GS}	Gate- source Voltage	± 20		V
I_D	Drain Current (continuous) at T_C = 25°C Single Operating	3	2.0	A
I_D	Drain Current (continuous) at T_C = 100°C Single Operating	1.5	1.3	A
I_{DM}(•)	Drain Current (pulsed)	12	8.0	A
P_{tot}	Total Dissipation at T_C = 25°C	2.5		W
T_{stg}	Storage Temperature	-55 to 150		°C
T_j	Max. Operating Junction Temperature	150		°C

(•) Pulse width limited by safe operating area.

Note: P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

TAB.1 THERMAL DATA

$Rthj\text{-}_{PCB}$(*)	Thermal Resistance Junction-PCB	62.5	°C/W

(*) When Mounted on 1 inch² FR-4 board, 2 oz of Cu and t [10 sec.

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

TAB.2 OFF

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0		80			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C				1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V				±100	nA

TAB.3 ON

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	n-ch p-ch	2 2	3 3	4 4	V V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 1.5 A V_{GS} = 10 V I_D = 1 A	n-ch p-ch		0.069 0.210	0.080 0.25	Ω Ω

TAB.4 DYNAMIC

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} = 15 V I_D= 1.5 A V_{DS} = 10 V I_D= 1 A	n-ch p-ch		4 4		S S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0	n-ch p-ch		510 739		pF pF
C_{oss}	Output Capacitance		n-ch p-ch		97 89.5		pF pF
C_{rss}	Reverse Transfer Capacitance		n-ch p-ch		40 31		pF pF

ELECTRICAL CHARACTERISTICS (continued)

TAB.5 SWITCHING ON

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	**N-CHANNEL** V_{DD} = 40 V I_D = 1.8A R_G = 4.7 Ω V_{GS} = 10 V	n-ch p-ch		7 13.5		ns ns
t_r	Rise Time	**P-CHANNEL** V_{DD} = 40 V I_D = 1 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 1)	n-ch p-ch		54 18		ns ns
Qg	Total Gate Charge	**N-CHANNEL** V_{DD}=64V I_D=1.8A V_{GS}=10V	n-ch p-ch		16 20		nC nC
Q_{gs}	Gate-Source Charge	**P-CHANNEL**	n-ch p-ch		3.2 2.5		nC nC
Q_{gd}	Gate-Drain Charge	V_{DD} = 64V I_D = 1A V_{GS} = 10V (see test circuit, Figure 2)	n-ch p-ch		16.3 4.9		nC nC

TAB.6 SWITCHING OFF

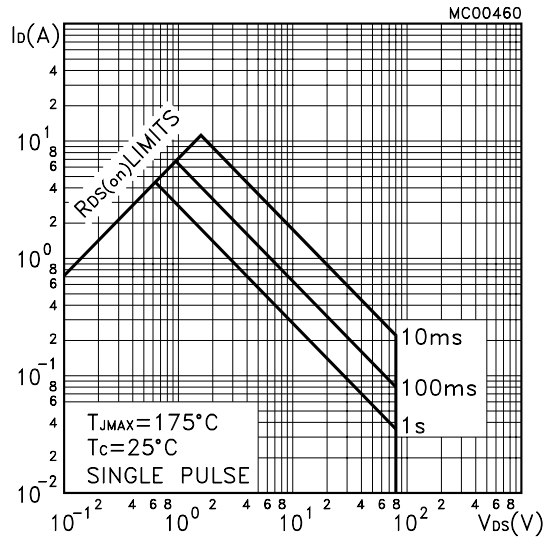
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	**N-CHANNEL** V_{DD} = 40 V I_D = 1.5 A R_G = 4.7 Ω V_{GS} = 10 V	n-ch p-ch		18 32		ns ns
t_f	Fall Time	**P-CHANNEL** V_{DD} = 40 V I_D = 1 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 1)	n-ch p-ch		14 13		ns ns

TAB.7 SOURCE DRAIN DIODE

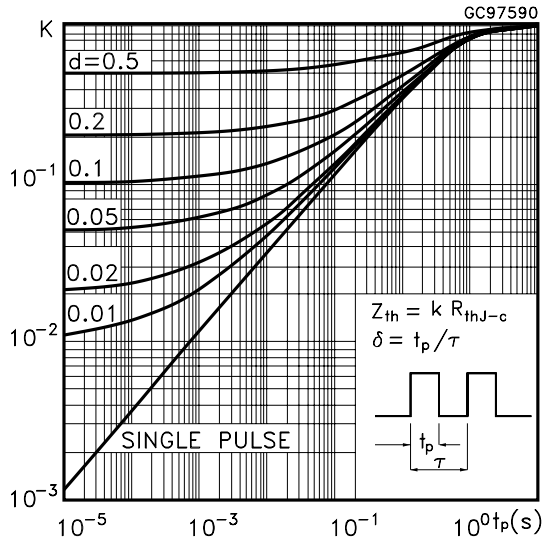
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current		n-ch p-ch			3 2.0	A A
I_{SDM} (•)	Source-drain Current (pulsed)		n-ch p-ch			12 8.0	A A
V_{SD}(*)	Forward On Voltage	I_{SD} = 3 A V_{GS} = 0 I_{SD} = 2 A V_{GS} = 0	n-ch p-ch			1.2 1.2	V V
t_{rr}	Reverse Recovery Time	**N-CHANNEL** I_{SD} = 3 A di/dt = 100A/µs V_{DD} = 29 V T_j =150 °C	n-ch p-ch		66.5 47		ns ns
Q_{rr}	Reverse Recovery Charge	**P-CHANNEL** I_{SD} = 2 A di/dt = 100A/µs	n-ch p-ch		149.6 87		nC nC
I_{RRM}	Reverse Recovery Current	V_{DD} = 40 V T_j =150 °C (see test circuit, Figure 3)	n-ch p-ch		4.5 3.7		A A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•) Pulse width limited by safe operating area.

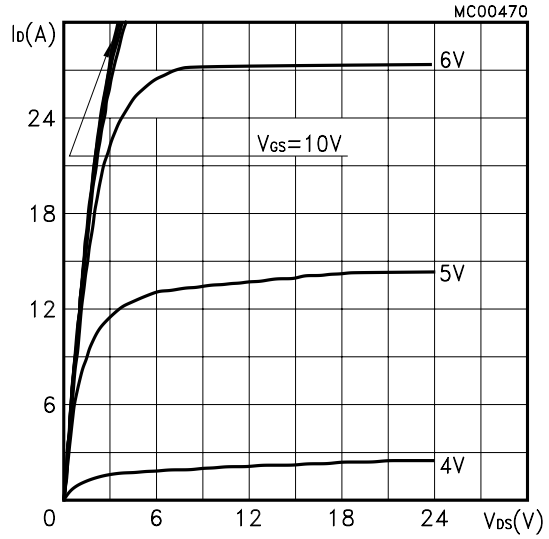
Safe Operating Area **n-ch**



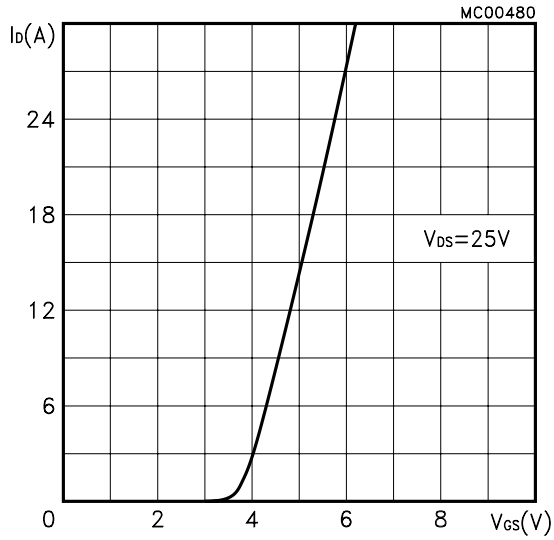
Thermal Impedance **n-ch**



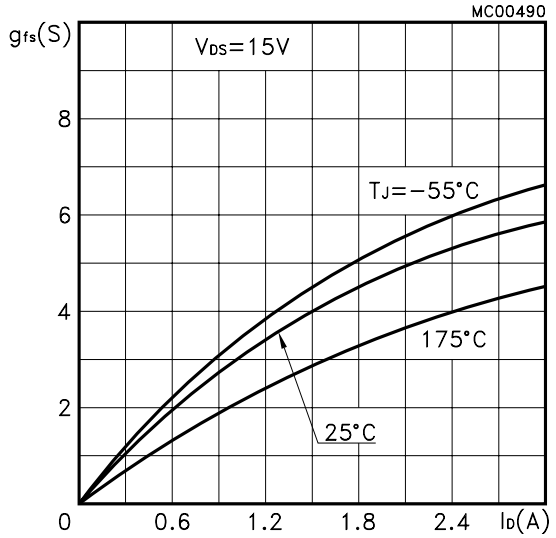
Output Characteristics **n-ch**



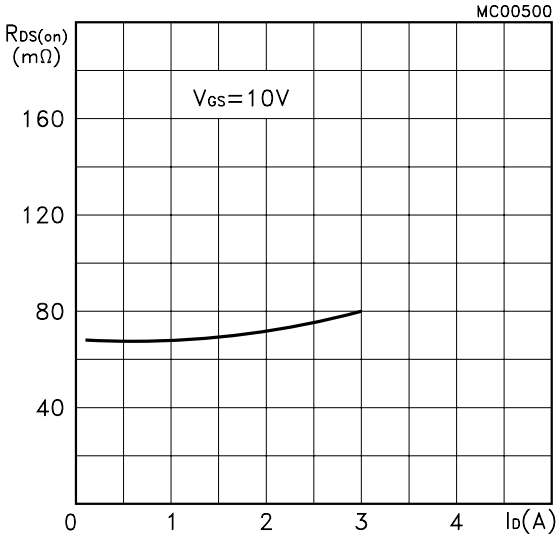
Transfer Characteristics **n-ch**



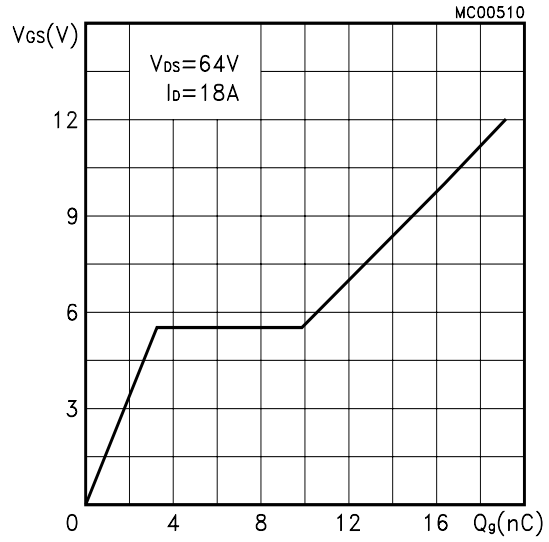
Transconductance **n-ch**



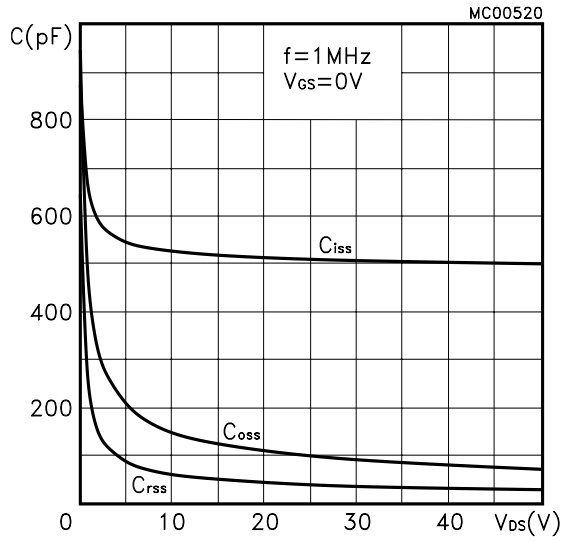
Static Drain-source On Resistance **n-ch**



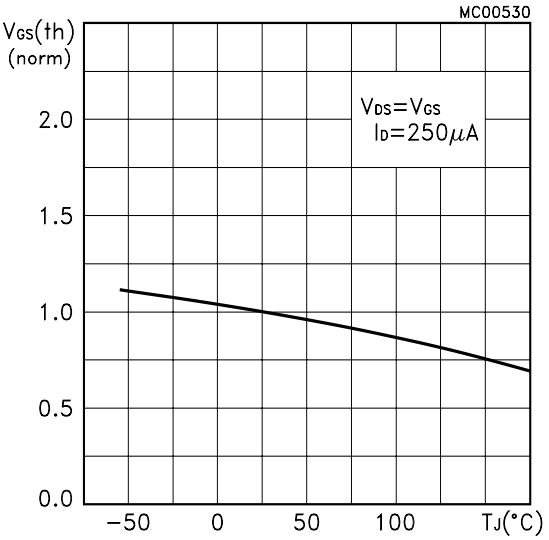
Gate Charge vs Gate-source Voltage **n-ch**



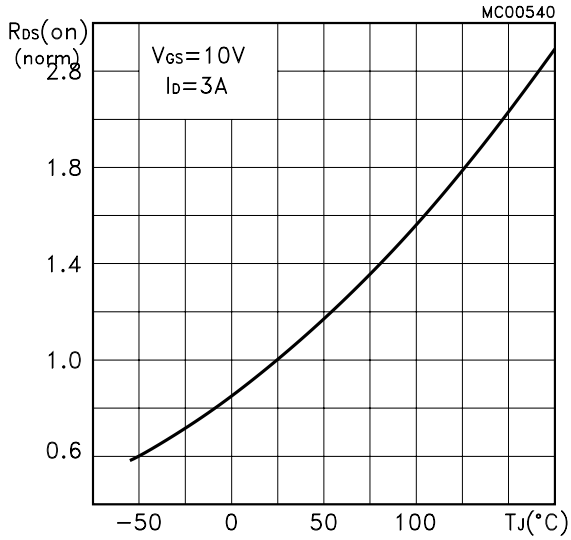
Capacitance Variations **n-ch**



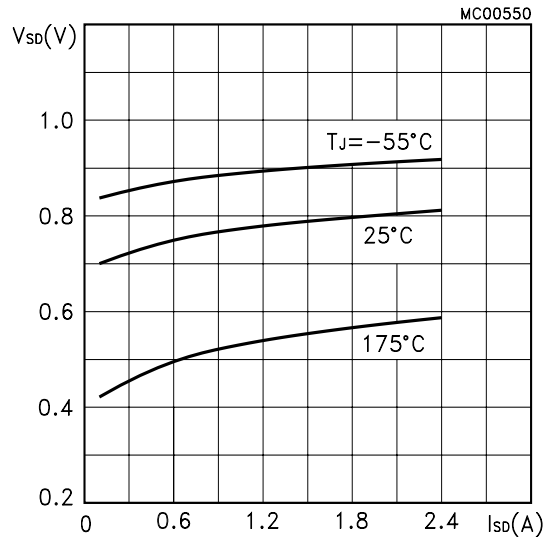
Normalized Gate Threshold Voltage vs Temperature **n-ch**



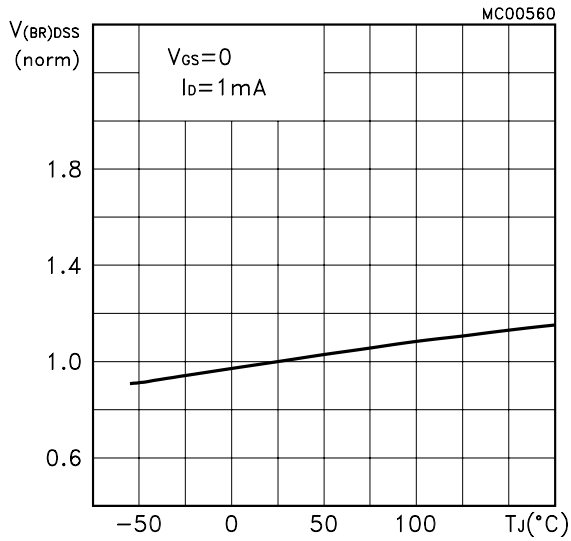
Normalized on Resistance vs Temperature **n-ch**



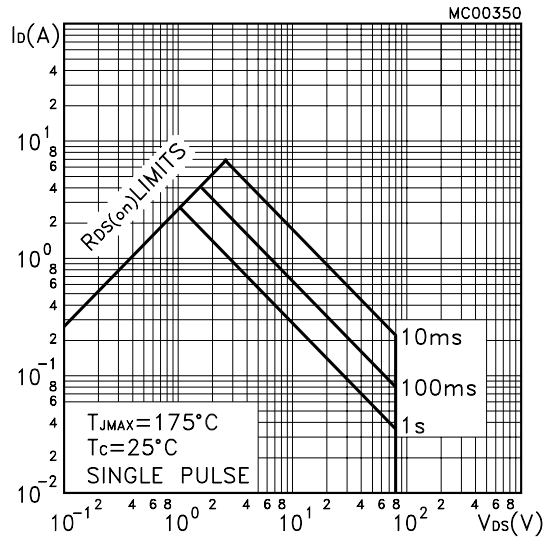
Source-drain Diode Forward Characteristics **n-ch**



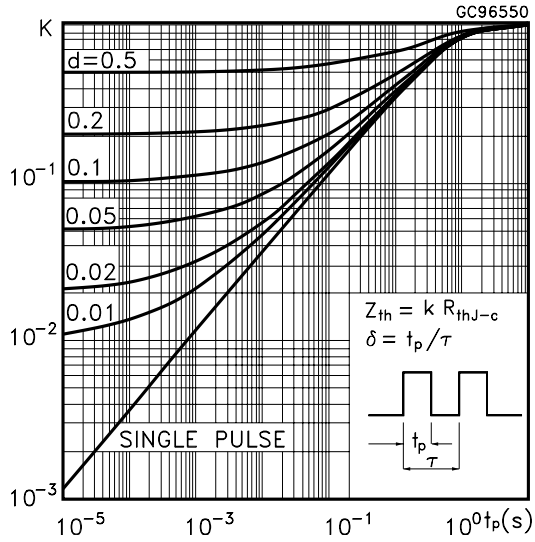
Normalized Breakdown Voltage Temperature **n-ch**



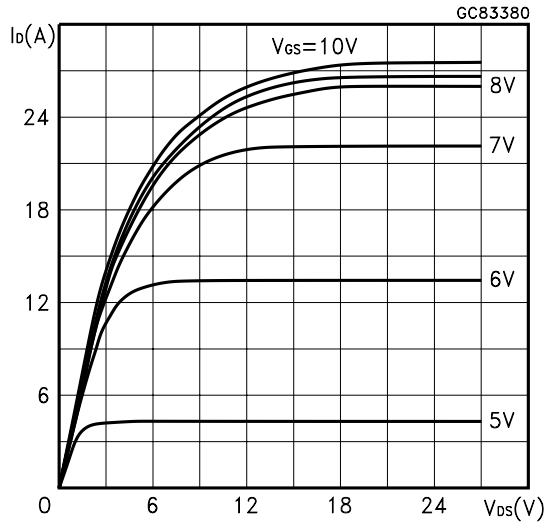
Safe Operating Area **p-ch**



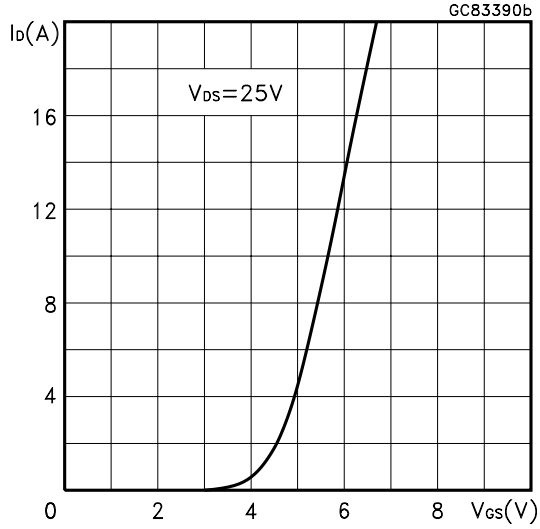
Thermal Impedance **p-ch**



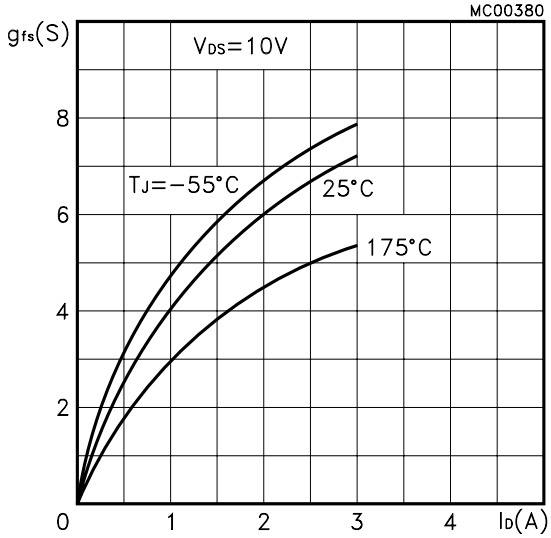
Output Characteristics **p-ch**



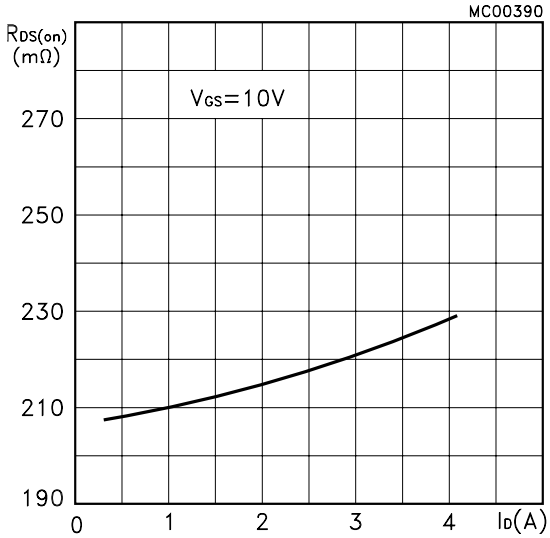
Transfer Characteristics **p-ch**



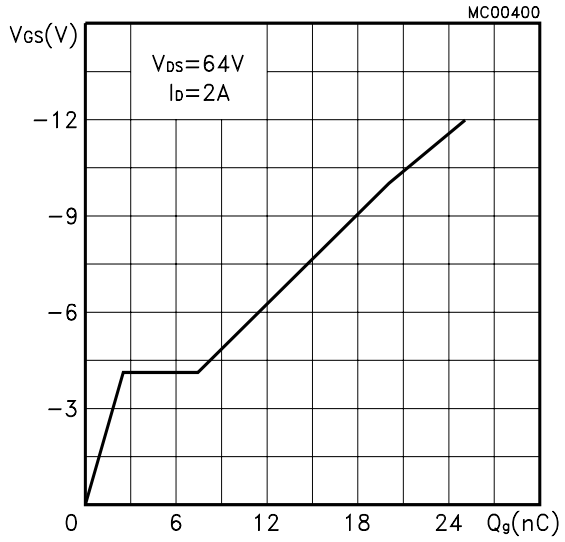
Transconductance **p-ch**



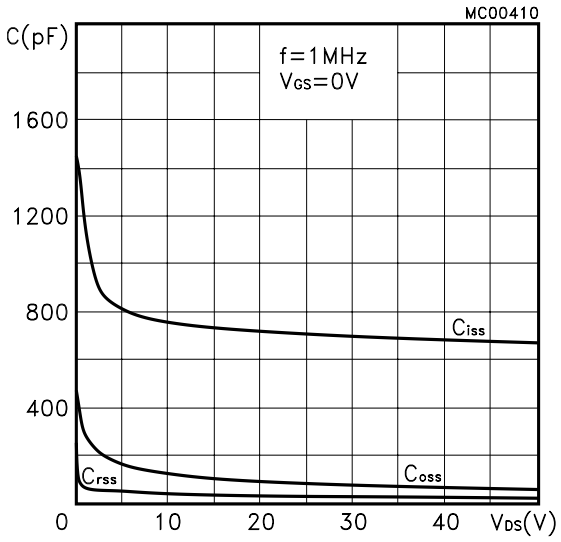
Static Drain-source On Resistance **p-ch**



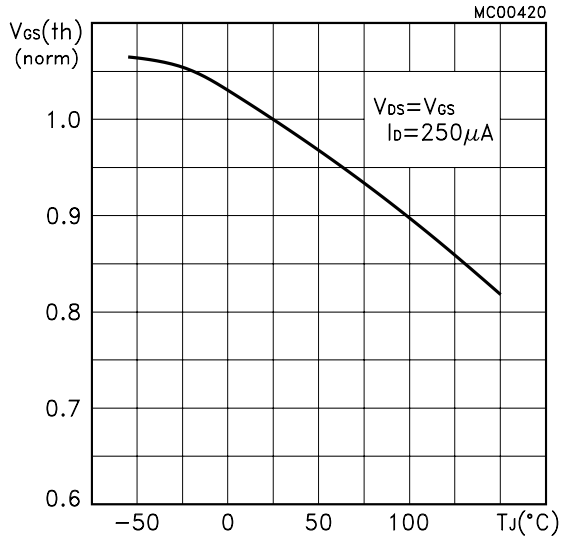
Gate Charge vs Gate-source Voltage **p-ch**



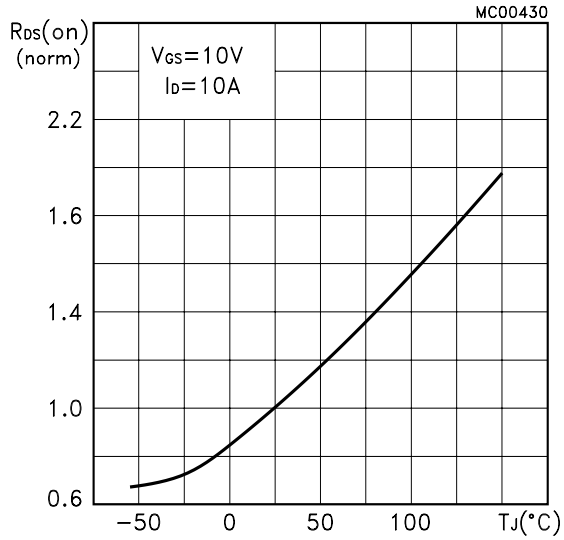
Capacitance Variations **p-ch**



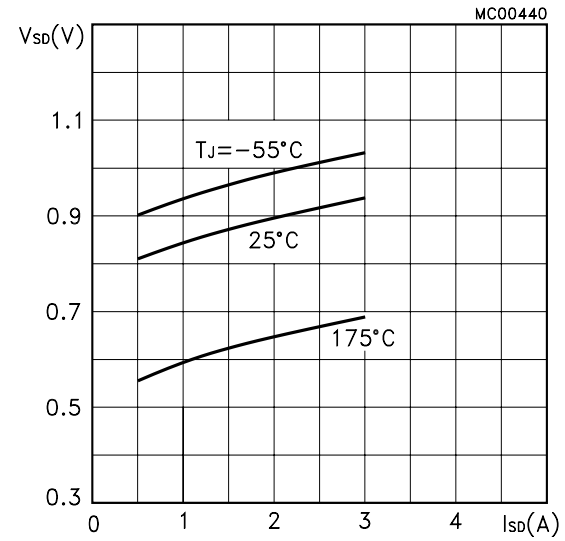
Normalized Gate Threshold Voltage vs Temperature **p-ch**



Normalized on Resistance vs Temperature **p-ch**



Source-drain Diode Forward Characteristics **p-ch**



Normalized Breakdown Voltage Temperature **p-ch**.

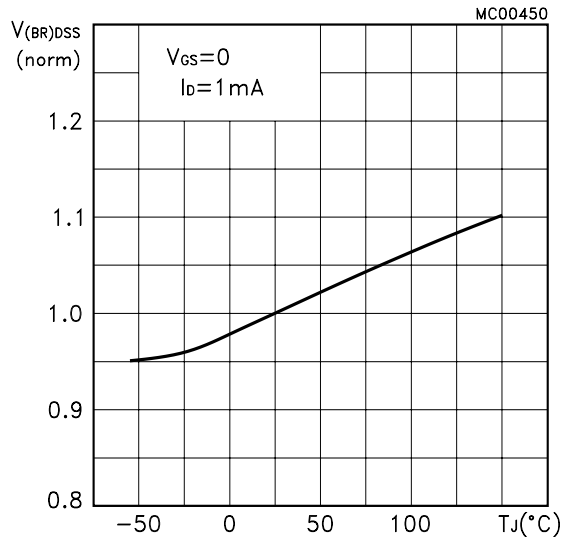


Fig. 1: Switching Times Test Circuits For Resistive Load

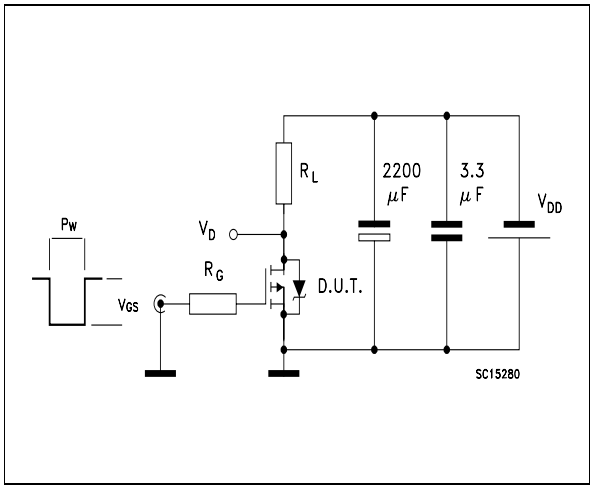


Fig. 2: Gate Charge test Circuit

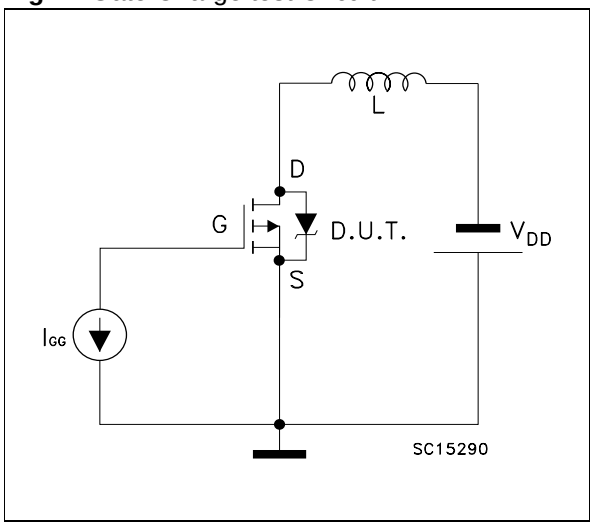
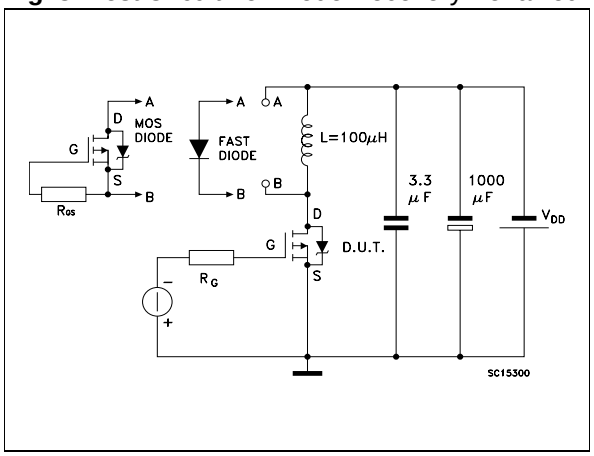
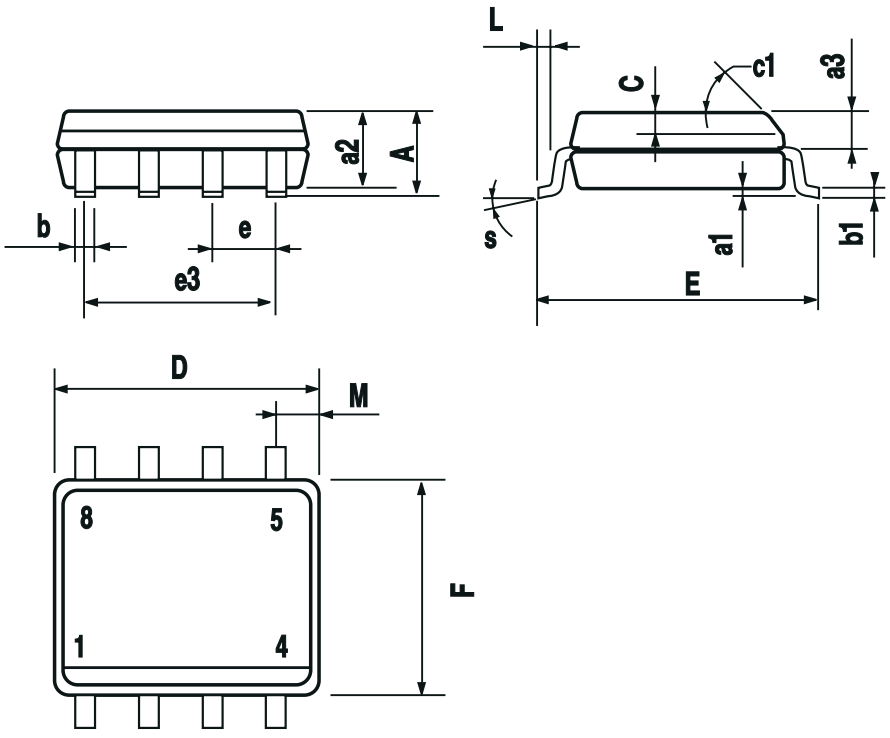


Fig. 3: Test Circuit For Diode Recovery Behaviour



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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Revision History

Date	Revision	Description of Changes
Tuesday 22 June 2004	0.1	FIRST ISSUE