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Interfacing Power MOSFETs to Logic Devices

Prepared by Ken Berringer
Motorola Discrete Applications

POWER MOSFET DRIVE CHARACTERISTICS

Power MOSFETs are commonly used in switching applications due to their fast switching speeds and low static losses. When driven with sufficient gate voltage, a power MOSFET will turn on and have a very low on-resistance. If the gate voltage is insufficient to bias the Power MOSFET fully on, or excessive drain currents are applied, the power MOSFET will operate in the saturation (pinch-off) region. In other words, a certain gate voltage will support only a limited amount of drain current.

Most of the current crop of fourth generation power MOSFETs require 10 volts of gate drive to support their maximum continuous drain current. This means that 5 volt logic will not provide enough voltage to drive a standard power MOSFET. A new family of Logic Level power MOSFETs are now available that can support their rated drain current with a gate voltage of 5 volts. With the proper considerations, these power MOSFETs may be easily interfaced to most logic families.

Design of the MOSFET's gate drive is dependent on the MOSFET's input capacitance, which is strongly affected by die size. Therefore, selecting the correct device for the application not only minimizes component cost, but it also optimizes switching performance. Static, or DC, losses are determined by the power MOSFET's on-resistance $R_{DS(on)}$, which is a function of junction temperature (T_J), gate voltage (V_{GS}), and drain current (I_D). $R_{DS(on)}$ is typically specified at I_D equal to half the rated drain current, a V_{GS} of 10 volts, and junction temperatures of 25 and 100°C.

The power MOSFET's static losses can be easily calculated in DC or pulsed applications. First, correct the rated $R_{DS(on)}$ for your drain current and estimated operating temperature with the help of the manufacturers' data sheet curves. Then multiply this value times the RMS load current squared [$P_{static} = I_{rms}^2 R_{DS(on)}$]. You should choose a power MOSFET with a current rating (I_D) and voltage rating (V_{DSS}) well above your worst case load conditions. A good rule of thumb is to select a device with twice your worst case RMS drain current and a voltage rating 25% above your worst case drain voltage.

In high frequency applications switching losses are often more significant than static losses. To minimize switching losses you must decrease the switching times. When a power MOSFET is used in switching applications, the gate cannot be modeled as a simple capacitor due to sizable displacement currents in C_{rss}, the drain-to-gate capacitor, brought on by large swings in drain-to-gate voltage. As a result, the total input capacitance, C_{iss}, varies greatly over the power MOSFET's operating range. C_{iss} can be piecewise modeled as a linear capacitor in order to find first order approximations of switching times.

A better method of calculating switching times is to use gate charge data from the manufacturers' data sheet. Although a power MOSFET is usually thought of as a voltage controlled device, it can be accurately modeled as a charge controlled device. The charge required for a power MOSFET to handle a given current is relatively constant even though its drain-to-gate capacitance (C_{rss}) varies drastically with drain-to-gate voltage. The value of C_{rss} may increase 1000% or more over the operating range.

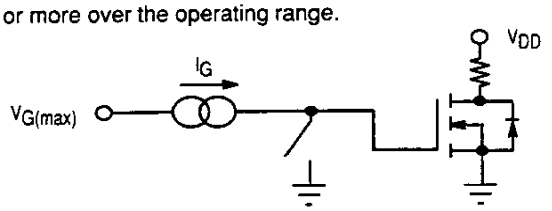

Figure 1. Driving a Power MOSFET with a Constant Current Source

When a power MOSFET is driven by a current source as in Figure 1, its gate voltage will be nearly piecewise linear as shown in Figure 2. The three distinct regions are turn on delay (t_0 to t_1), rise time (t_1 to t_2), and excess charge time (t_2 to t_3). At the end of the turn on delay (t_1) the power MOSFET begins to conduct but the drain current is still very small. During the rise time the power MOSFET actually turns on and the drain voltage drops to almost zero. The resistive switching rise time t_{rise} is actually measured as the time it takes for the drain voltage to drop from 90% to 10% of its highest value. It is called rise time referring to the drain current rise time although the voltage is what's usually measured. This time corresponds to the time that V_{GS} remains in the plateau region of Figure 2.

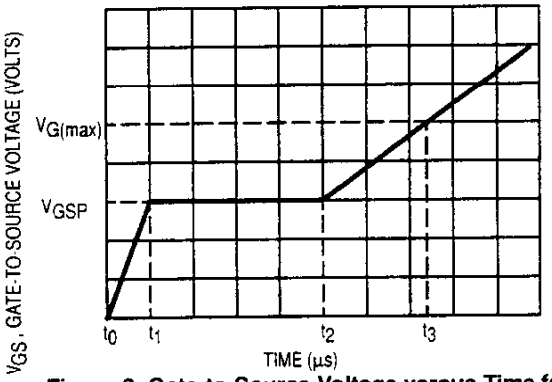

Figure 2. Gate-to-Source Voltage versus Time for a Current Source Turning On a Power MOSFET

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During the excess charge time (t_2 to t_3) $R_{DS(on)}$ continues to decrease. This excess charge must be removed during the turn off delay, so driving the gate to an unnecessarily high voltage will increase the total turn off time.

Unlike bipolar transistors, power MOSFETs are majority carrier devices. Without minority injection, power MOSFETs can be turned off just as easily as they are turned on. For identical gate drive currents, rise time will equal fall time. The turn off waveform for a constant gate current will be a mirror image of Figure 2. Note that the turn off delay does not equal turn on delay, it instead corresponds to the turn on excess charge time.

Since the gate current in Figure 2 is constant and equal to the charge per unit time, the horizontal axis can be labeled time or charge. Gate charge data is usually measured using a 1 mA current source which means it will provide 1 nC (nano-Coloumb) of charge in 1 µs. Manufacturers' data sheets usually include a gate charge chart of V_{GS} vs Q_g with Q_g labeled in nC as in Figure 3. It is important to note that the value of V_{GS} during rise time, also called the plateau voltage, increases with I_D and therefore so does the turn on delay. Also, the amount of charge needed for rise time will vary with the drain supply voltage. This is usually indicated on the gate charge chart by multiple lines for the excess charge region labeled with the corresponding V_{DS}.

To determine the switching times using a current source to drive a Power MOSFET, find the charge required for each region using the gate charge chart, Figure 3, and then use the simple equation:

$$t = Q_g/I_G. \quad (1)$$

First find the charge required during the turn on delay region, $Q_{d(on)}$, by drawing a line down from the first inflection point to the horizontal axis of Figure 3. This is the gate charge for the rated or tested I_D. If your actual drain current is different than the rated current you may improve accuracy by linearly scaling $Q_{d(on)}$. Now calculate the turn on delay using Equation 1. Next find the gate charge required for rise time (Q_{rise}) from the gate charge chart as the distance between the first inflection point and the intersection of the plateau with the line for your expected V_{DS}. A typical value is sometimes listed as Q_{gd}. This value may be used to calculate both rise and fall times. Next find the intersection point of your maximum V_{GS} and the line corresponding to your V_{DS}. This is the total gate charge $Q_{g(total)}$. To find the charge required for turn off delay $Q_{d(off)}$ (and turn on excess charge), subtract $Q_{d(on)}$ and Q_{rise} from $Q_{g(total)}$. A maximum total gate charge $Q_{g(max)}$ is often specified to facilitate worst case design, however this figure sometimes includes a substantial guard-band.

When driving a power MOSFET with a voltage source with a series resistance (Thevenin source), the calculations are a little more complex. During the rise and fall times V_{GS} is relatively constant since all the gate current is used to charge the gate-to-drain capacitor. By Ohm's law, I_G is therefore also constant and the gate charge chart can be used with Equation 1 to find rise and fall times. During turn on the voltage across the series resistance is the effective source voltage (usually the supply voltage) minus the gate-to-source plateau voltage, V_{GSP}. During turn off the voltage across the resistor is the plateau voltage minus the effective sink voltage (usually ground). Rise and fall times will therefore typically be different.

Using this information with Equation 1, we can obtain equations for rise and fall time.

$$t_{rise} = \frac{Q_g}{I_G} = \frac{Q_{gd}\, R_{eff(ON)}}{V_{SOURCE}-V_{GSP}} \quad (2)$$

and fall time:

$$t_{fall} = \frac{Q_g}{I_G} = \frac{Q_{gd}\, R_{eff(OFF)}}{V_{GSP}-V_{SINK}} \quad (3)$$

V_{GSP} is the Power MOSFET's gate-to-source plateau voltage, V_{source} is the gate driver's effective source voltage, V_{sink} is the gate driver's effective sink voltage, and R_{eff} is the gate driver's effective resistance (output resistance). During turn off V_{sink} may be near zero volts or even a negative voltage.

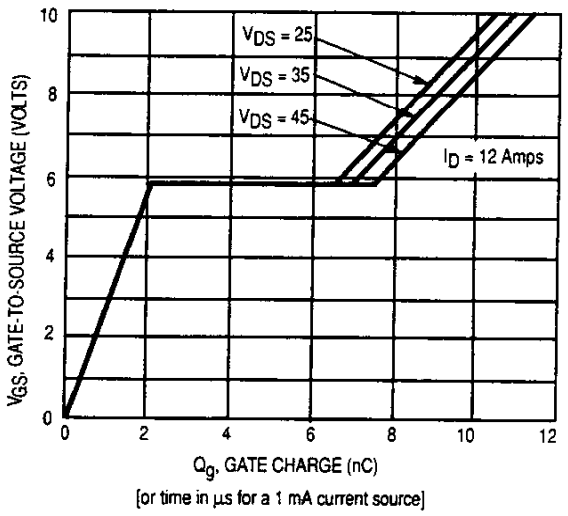


Figure 3. Gate Charge Chart for the MTP3055E

During the turn on and turn off delays gate current is not constant and gate charge data cannot be used to determine switching speeds. The series resistance and the gate capacitance form a simple RC network; however, the capacitance varies greatly over the operating range. To find the switching times you must determine the capacitance for each region from a capacitance chart like Figure 4. During the turn on delay V_{DS} is near its maximum value, V_{GS} is near zero, and the input capacitance is low. Find the value of C_{iss} in the capacitance curve for your maximum value of V_{DS} and use this capacitance, Point A in Figure 4, to calculate the turn on delay. You can use Equation 4 to approximate the turn on delay time.

$$t_{d(ON)} = R_{eff(ON)}\, C_{iss(MIN)}\, \ln\left[\frac{V_{SOURCE}}{V_{SOURCE}-V_{GSP}}\right] \quad (4)$$

During the turn off delay V_{DS} will be low and C_{iss} will have a larger value. Find the value of C_{iss} corresponding to minimum V_{DS} and maximum V_{GS}, Point B on the capacitance chart. Then use Equation 5 to approximate turn off delay time.

$$t_{d(OFF)} = R_{eff(OFF)}\, C_{iss(MAX)}\, \ln\left[\frac{V_{G(MAX)}-V_{SINK}}{V_{GSP}-V_{SINK}}\right] \quad (5)$$

$V_{G(max)}$ is the initial gate voltage prior to turn off (usually the supply voltage), $R_{eff(off)}$ is the effective series resistance during turn off, and V_{sink} is the effective sink voltage. If V_{sink} is at ground, then the V_{sink} terms will drop out of Equation 5.

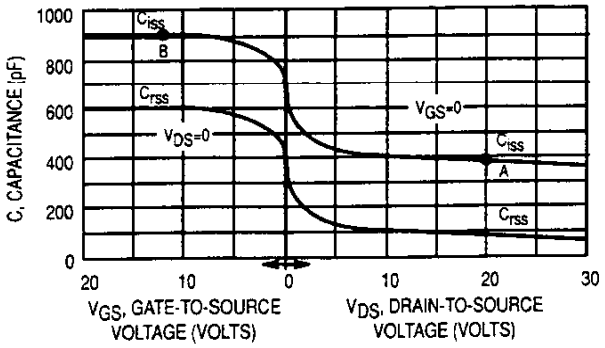


Figure 4. Capacitance Chart for the MTP3055E

Note that the gate charge chart and capacitance curves are related. The slope of the line in the gate charge chart is in volts per nano-Coloumb. A Farad of capacitance is equal to a Coloumb per volt.

$$I(coulomb/sec) = C\ dV/dt(Farad\text{-}volts/sec).$$

From this equation, you find that

$$Farad = coulomb/volt.$$

Therefore, the reciprocal of the slope is the input capacitance in nano-Farads (1000 pF). However, you should use both charts. The gate charge chart is most useful when the input capacitance varies and the gate current is constant (rise and fall times). The capacitance curve is most useful when the input capacitance is constant and the gate current varies (delay times).

DIRECT INTERFACE TO STANDARD POWER MOSFETs

Standard power MOSFETs can be interfaced directly with standard CMOS devices, such as the MC14000 family. This family uses complementary N and P channel FETs for the output stage. Although standard outputs are rated at ±10 mA and buffer outputs are rated at ±45 mA, saturation currents for short circuit conditions are much higher. While a CMOS gate should not be short circuited for long periods of time, it may be safely operated in the saturation region when switching large capacitive loads. A 14049UB inverter buffer can typically source 30 mA and sink 120 mA using a 12 volt supply. If the output current is not limited, the CMOS gate's output will act like a current source. If the output current is limited to less than the saturation currents, the CMOS gate's output will act like a voltage source with a finite output resistance. The MC14000 series family will operate from 3 to 18 volts. The common 12 or 15 volt V_{DD} supply will drive Power MOSFETs nicely.

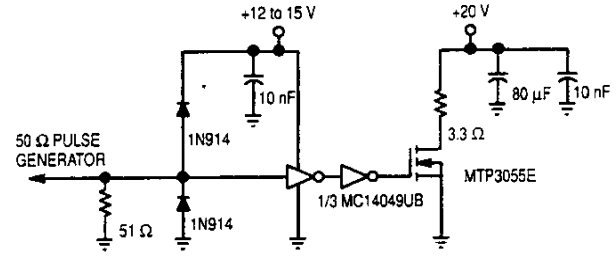


Figure 5. Standard CMOS Interface Circuit

The 14049UB can be connected directly to a standard power MOSFET such as the MTP3055E as in Figure 5. The MTP3055E is a rugged 12 amp, 60 volt power MOSFET that is very popular in the industry. The gate drive current is not limited by a series resistor and therefore the gate drive current will be equal to the 14049's output saturation currents of +30/–120 mA. Using the gate charge data with Equation 1, we can predict the following switching times.

$$t_{d(ON)} = 2\ nC/30\ mA = 67\ nsec$$

$$t_{rise} = 4\ nC/30\ mA = 133\ nsec$$

$$t_{d(OFF)} = 6\ nC/120\ mA = 50\ nsec$$

$$t_{fall} = 4\ nC/120\ mA = 33\ nsec$$

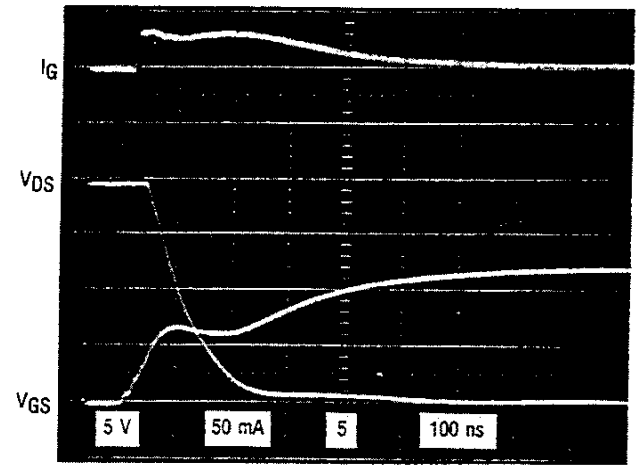
The switching times were measured using the circuit in Figure 5. The actual scope waveforms are shown in Figure 6, and the measured switching times are shown in Table 1.

Table 1. Switching Times for Standard CMOS Devices Driving an MTP3055E
I_D = 6 Amps One gate used unless noted

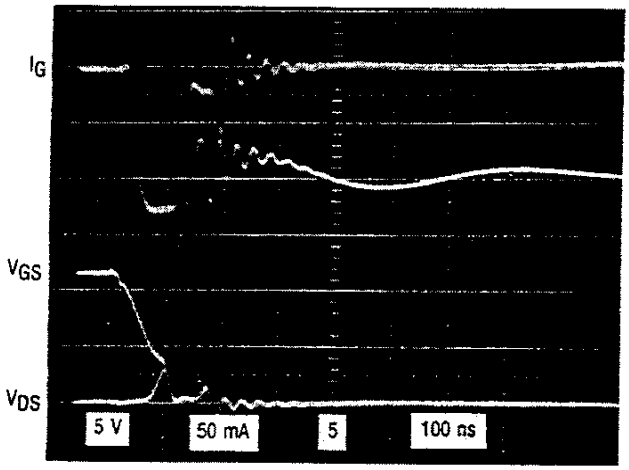
Driver	V_{CC} (Volts)	R_G (Ω)	$t_{d(on)}$ (ns)	t_{rise} (ns)	$t_{d(off)}$ (ns)	t_{fall} (ns)
4049UB	12	0	50	150	60	50
4049UB	12	220	60	300	200	150
4049UB	12	470	100	400	400	300
4049UB	15	0	40	100	70	40
4049UB	15	220	50	200	280	120
4049UB	15	470	75	330	500	420
4050B	12	0	50	150	60	50
4050B	12	220	60	300	200	150
4050B	12	470	100	400	400	300
4069UB	12	0	100	350	340	250
4069UB	12	220	115	500	380	370
4069UB	12	470	150	680	530	580
4069UB x2	12	0	70	260	170	130

The calculated values were fairly accurate for first order approximations considering that the speeds are high enough that circuit parasitics can affect performance. The saturation currents of the '4049 vary from device to device and with the supply voltage V_{DD} and junction temperature. Driving directly from the logic IC will provide the quickest rise and fall times, but these times will vary greatly.

By adding a resistor between the CMOS buffer's output and the gate of the power MOSFET in Figure 5 we can control switching times by limiting gate drive current. However, increasing the gate resistor also increases the power MOSFET's susceptibility to noise and accidental dv/dt turn on. A rapid change in the power MOSFET's drain voltage will cause a voltage to appear on the gate, which may be sufficient to turn



TURN-ON



TURN-OFF

Figure 6. Scope Waveforms for an MC14049 Driving an MTP3055E

it on. Keeping the driver impedance low will minimize or eliminate this phenomenon.

To find the switching times using a gate resistor, use Equations 2 and 3 to find rise and fall times. Then use Equations 4 and 5 to find the delay times. Here $R_{eff(on/off)}$ equals the gate resistor, R_g, plus the CMOS buffer's output resistance, R_o. The approximate output resistance of the '4049 is 200 Ω for turn on and 50 Ω for turn off. Let V_{source} equal V_{DD} and V_{sink} equal zero. Switching times for several gate resistors are summarized in Table 1.

The UB in the MC14049UB stands for "un-buffered". This means that it consists of a single complementary inverter. The additional gate in Figure 5 is used to ensure the power MOSFET driver is itself driven to V_{DD}. The input voltage will greatly affect saturation currents and therefore switching times. The MC14050B is a "buffered" non-inverting buffer and consists of two cascaded inverters. It therefore does not invert the signal, and is less susceptible to soft drive conditions. The diodes on the input in Figure 5 clamp the input voltage to ground and V_{DD}. Excessive voltage applied to a CMOS input may damage it's internal static protection diodes. Voltage in excess of the supply voltage, V_{DD}, applied to the output of a CMOS device may cause it to latch-up and destroy itself. Remember to decouple the logic device, as it is drawing substantial currents.

Open collector TTL gates can also be used to drive standard power MOSFETs. However, most open collector output stages were designed for 5 volt operation. Low power Schottky (LS) gates such as the 74LS05 typically have a collector-emitter breakdown voltage of 10 to 15 volts. This makes them unsuitable for operation using a 12 or 15 volt supply. They can be operated from an 8 to 10 volt supply or with an 8 to 10 volt zener clamp on the output; however, long-term reliability of the logic device will suffer.

The 74LS26 was designed to interface to 15 volt logic and has a tested CE breakdown greater than 15 volts. This Quad NAND gate can be used to drive a power MOSFET with a single pull-up resistor, as in Figure 7. Using a 1.5KΩ pull-up with a 12 volt supply will limit the steady state sink current to 8 mA. This is necessary to guarantee the 'LS26's rated output low voltage V_{OL} of 0.5 volts. Using a smaller pull-up resistor would increase the V_{OL} of the 'LS26, and consequently increase the drain-to-source leakage current of the power MOSFET in the off state.

During turn on, current is supplied by the pull-up resistor. During turn off the 'LS26 must sink both the gate current and the pull-up resistor current. The pull-down transistor of an LS output will typically sink about 30 mA. Turn on times can be calculated using Equations 2 and 4 with $R_{eff(on)}=R_p$ and $V_{source}=V_p$, where R_p is the pull-up resistor and V_p is the pull-up's supply voltage. Turn off times can be calculated using Equations 3 and 5 with $R_{eff(off)}=R_p$ and $V_{sink}=V_p-I_{sink}R_p$ (V_{sink} may be negative). The equations for $R_{eff(off)}$ and V_{sink} are the Thevenin equivalent of an ideal constant current source working against a pull-up resistor. The V_{sink} equation is only valid when the pull-down transistor may be approximated as a current source. During the turn off delay and fall times, the pull-down transistor provides a nearly constant sink current, since the pull-down transistor's collector-emitter voltage exceeds it's $V_{CE(sat)}$ and the base drive current is relatively constant.

The 'LS26 with a 1.5KΩ pull-up was used to drive a MTP3055E as in Figure 7. Oscilloscope waveforms are shown in Figure 8, and the switching times are summarized in Table 2.

This configuration provides minimum rise and fall times; however, fall times will vary greatly, since the 'LS26's sink current will vary with temperature and from device to device. A series gate resistor can be used to slow and control turn off. Switching times can again be calculated using Equations 2 through 5. For large gate resistors you may use the following approximations: $R_{eff(on)}=R_p+R_g$, $V_{source}=V_p$, $R_{eff(off)}=R_g$, and $V_{sink}=0.5$ volts. Switching times for several gate resistors are summarized in Table 2.

Table 2. Switching Times for the 74LS26 Driving an MTP3055E
I_D = 6 Amps Only one gate used

V_{CC} (Volts)	R_G (Ω)	R_P (Ω)	$t_{d(on)}$ (ns)	t_{rise} (ns)	$t_{d(off)}$ (ns)	t_{fall} (ns)
12	0	1500	200	850	240	175
15	0	1800	200	750	300	175
12	1500	1500	450	2000	1300	1450
12	3000	3000	930	3900	2500	2900

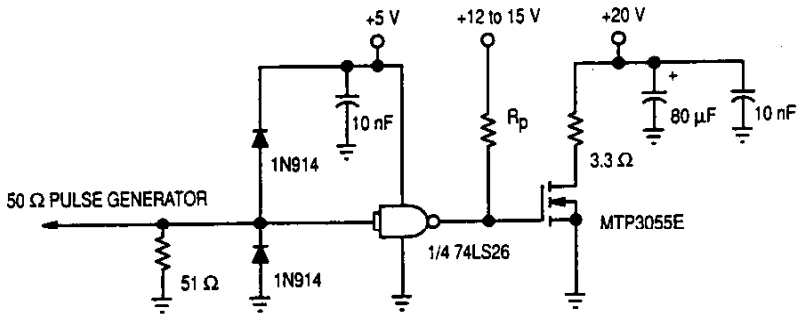
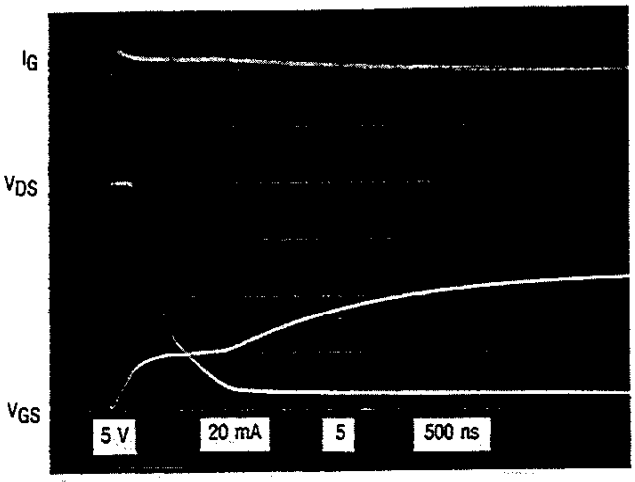
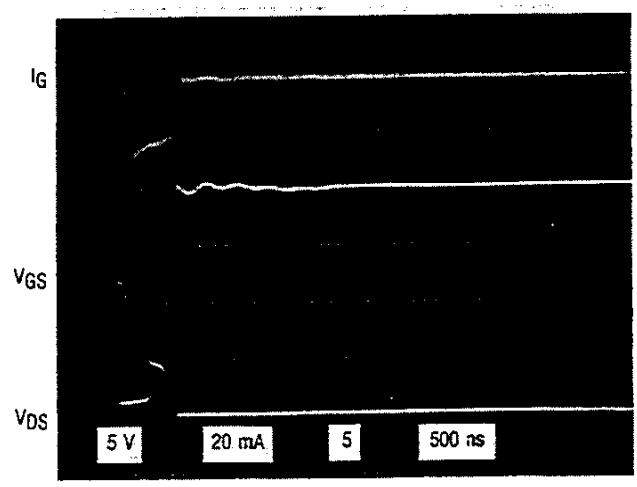


Figure 7. Low Power Schottky Interface Circuit



TURN-ON



TURN-OFF

Figure 8. Scope Waveforms for a 74LS26 Driving an MTP3055E
V_{CC} = 5 Volts, V_P = 12 Volts, Rp = 1.5KΩ

DIRECT INTERFACE TO LOGIC LEVEL POWER MOSFETs

Logic level Power MOSFETs are designed to be easily interfaced to 5 volt logic devices. They have a larger transconductance and a lower threshold voltage than their conventional counterparts. More importantly, $R_{DS(on)}$ is specified at V_{GS}=5 volts. Unfortunately most 5 volt logic families do not have 5 volt high output (V_{OH}) capability. Fast Schottky (FAST) and Low power Schottky (LS) logic have a minimum rated V_{OH} of 2.7 volts. This means that a pull-up resistor to 5 volts is required to drive Logic Level Power MOSFETs. High speed CMOS (HC) has a V_{OH} rating of 4.95 volts, and therefore does not need a pull-up resistor.

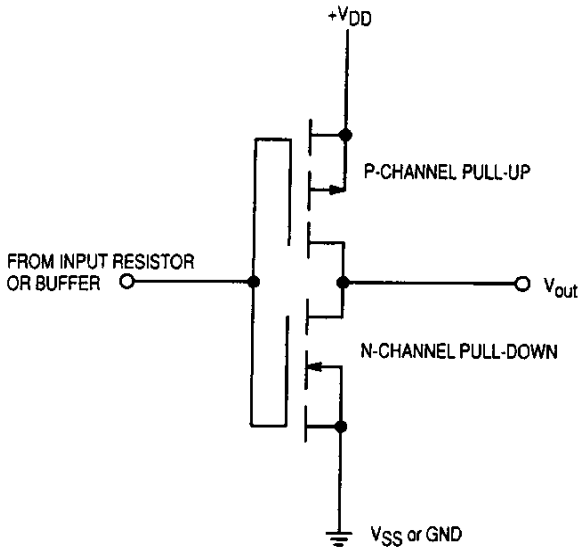
Figure 9 shows the output stages of HC and LS logic devices. The HC output stage in Figure 9a is identical to the standard CMOS output stage, except that the complementary MOSFETs have been optimized for 5 volt operation. Most HC devices are buffered by additional complementary stages. The LS output stage in Figure 9b uses a totem pole output. The pull-down transistor is biased on by about 500 µA and has a current gain of about 60. This means it can sink a maximum of 30 mA. The 110 Ω resistor limits the pull-up transistor's sink current to about 30 mA when the output is shorted.

Figure 10 shows how to interface HC, LS, and FAST logic to Logic Level Power MOSFETs. Note the input termination and protection circuitry. This is necessary to drive the logic devices with a pulse generator. It is best to drive the Logic Level Power MOSFET driver with a device from the same logic family. When connecting an HC (or any CMOS) device to a off board connector, the diodes should be used for ESD protection.

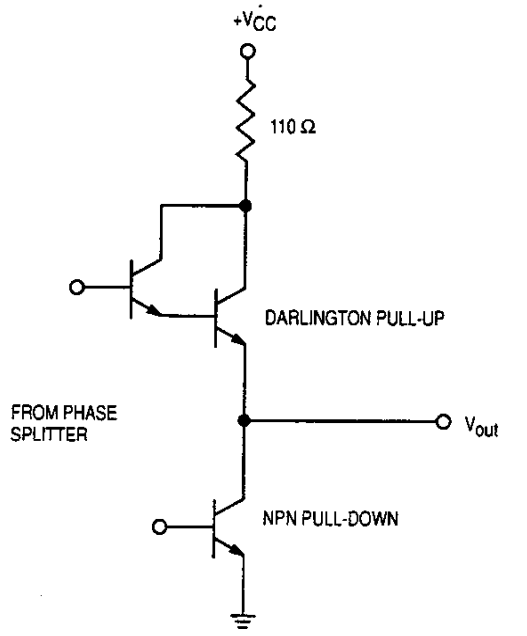
Figure 11 shows the switching waveforms for the three logic families driving a Logic Level Power MOSFET using the circuits in Figure 10. The measured switching times are in Table 3.

Table 3. Switching Times for Logic Devices Driving a Logic Level MTP3055EL
I_D = 6 Amps unless noted. One gate used unless noted.

Driver	Rp (Ω)	$t_{d(on)}$ (ns)	t_{rise} (ns)	$t_{d(off)}$ (ns)	t_{fall} (ns)	Comment
74HC04		25	120	85	75	
74LS04	560	45	450	120	130	
74F04	220	15	170	18	21	
74HC04		10	65	30	30	2 gates
74HC04		10	125	35	45	12A 50°C



(a) CMOS Output Stage



(b) LS TTL Output Stage

Figure 9. Logic Output Stages

A 74HC04 hex inverter can be connected directly to a Logic Level Power MOSFET. The switching times can be calculated the same way as the CMOS inverter buffer. The 'HC04 will source and sink about 50 mA with a 5 volt supply.

The HC family has an operating supply range of 2 to 6 volts. An HC device will drive the Logic Level Power MOSFETs gate to within 50 mV of V_{DD}. However, if the V_{DD} supply falls below 5 volts the switching times and $R_{DS(on)}$ will increase dramatically. A 10% reduction in V_{DD} (to 4.5 volts) will increase the rise time by about 50% and fall time roughly 15%. $R_{DS(on)}$ will increase from 10 to 100% or more depending on the drain current and junction temperature. If low voltage operation is a real possibility you should choose the Logic Level Power MOSFET and heatsink to handle this worst case condition. Examine the curves for "On-region Characteristics", "$R_{DS(on)}$ versus I_D", and "$R_{DS(on)}$ versus Temperature" in the manufacturers' data sheet. You may need to use a device with a current rating much larger than your expected load current to attain the desired $R_{DS(on)}$ under low supply conditions. Manufactures are now developing 4 volt logic level power MOSFETs with $R_{DS(on)}$ rated at 4 volts. These devices may be easily interfaced to HC logic devices and operated down to 4 volts. However, the lower threshold voltage makes them more susceptible to noise and increases leakage currents.

The 74LS04 in Figure 10 must have a pull-up resistor to 5 volts. A minimum pull-up resistor of 560 Ω will guarantee the logic device's output low voltage, V_{OL}, of 0.5 volts. During turn on, gate drive current is supplied by the pull-up resistor and the 'LS04's internal pull-up transistor. During turn off the 'LS04 must sink both the gate drive current and the pull-up resistor current. A larger R_p will increase turn on time and decrease turn off time. A smaller R_p would increase the V_{OL} of the 'LS04, increasing the power MOSFET's leakage current. The lower threshold voltage of logic level power MOSFETs makes the V_{OL} rating critical. The threshold voltage of a power MOSFET decreases as temperature increases. Therefore, the V_{OL} of the logic device must be less than the logic level power MOSFET's threshold voltage $V_{GS(th)}$ at its maximum expected junction temperature. For this reason 4 volt logic level power MOSFETs may be incompatible with TTL logic devices.

Switching times can again be estimated by using the Thevenin equivalents of the drive circuit with Equations 2 through 5. During turn on delay, current is supplied by the Darlington pull-up transistor of the 74LS04, and the external pull-up resistor. The Darlington is in saturation with a $V_{CE(sat)}$ of about 1.5 Volts. The 74LS04's output current is then limited by the internal 110 Ω resistor. To calculate turn on delay time, you may use Equation 4 with $V_{source} = V_{CC}$ $[1.5R_p/(R_p + 110\Omega)]$ and $R_{eff(on)} = R_p||110\,\Omega$. During rise time nearly all the current is supplied by the pull-up resistor, since V_{GSP} is usually above the V_{OH} of the 'LS04. You may therefore use Equation 2 with $V_{source} = V_{CC}$ and $R_{eff(on)} = R_p$ to estimate rise time.

During turn off the pull-down transistor must sink both the gate current and the pull-up resistor current, just like the open collector 74LS26 in Figure 7. To calculate turn off times, use $V_{sink} = V_{CC} - I_{sink}R_p$ and $R_{eff(off)} = R_p$ with Equations 3 and 5. The pull-down transistor's maximum sink current, I_{sink}, is typically about 30 mA.

The 74LS family's specified supply voltage (V_{CC}) range is from 4.75 to 5.25 volts. The rise time will vary greatly with supply voltage while the fall time only varies by about 5%. The rise time will vary from about +80% to –40% for V_{CC} equals 4.75 and 5.25 volts respectively. This is due to supply voltage affecting both the pull-up resistor current and the pull-up transistor current. Since the operating supply range of LS is less than that of HC logic, $R_{DS(on)}$ will not vary as much, but must be considered.

The FAST logic family can source and sink much more current than the LS family. The 74F04 can source about 50 mA and sink about 200 mA. A minimum pull-up resistor of 220 Ω will guarantee the logic device's output low voltage V_{OL} of

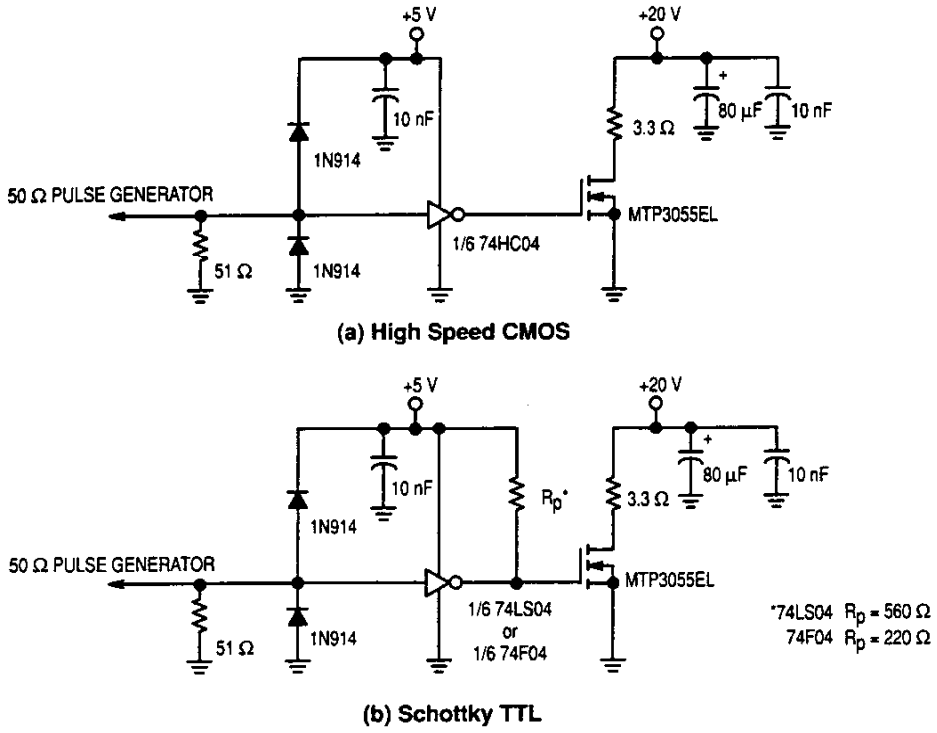


Figure 10. Logic Level Power MOSFET Interface Circuits

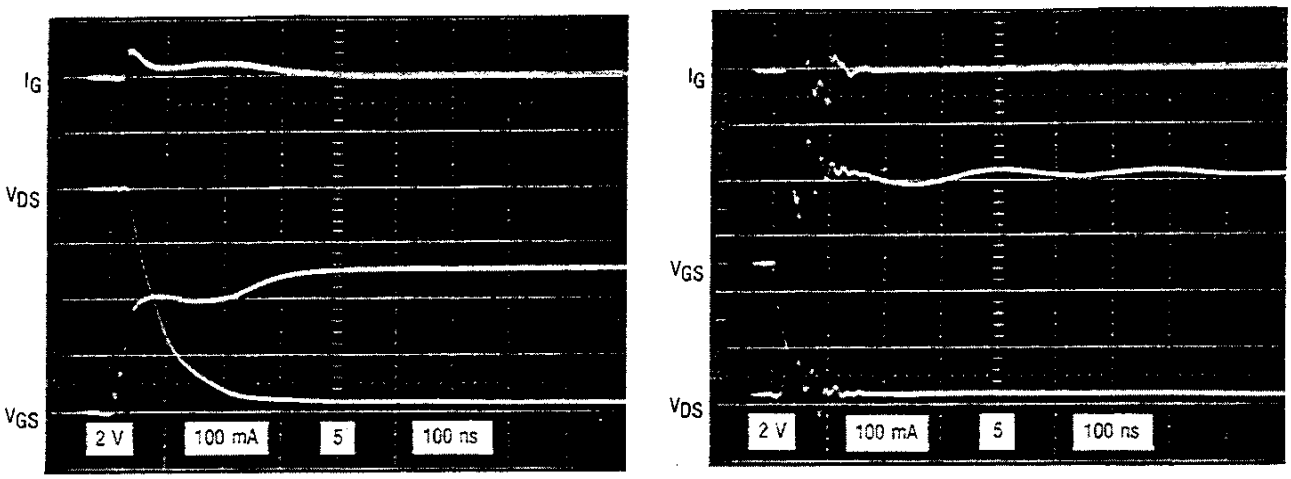
0.5 volts. A larger R_p will increase turn on time and decrease turn off time. The switching times can be calculated as in the LS family. The 74F04 uses an internal 35 Ω resistor to limit the pull-up Darlington's output current, instead of the 110 Ω resistor. The same supply voltage considerations for LS family also apply to the FAST family.

A series gate resistor may be used with any of the circuits in Figure 10 to slow and control switching times. The switching times for large gate resistors (greater than 200 Ω for HC, 5KΩ for LS, and 2KΩ for FAST) can be estimated using $R_{eff(on/off)} = R_g$ with the Equations 2 through 5. When switching loads even slightly inductive, the inductive kick-back during turn off may cause the drain voltage to rise above the load supply. Slowing down the turn off with a gate resistor will reduce this voltage. If this voltage is large enough and sufficient energy is present it may destroy the Power MOSFET. A new family of rugged Power MOSFETs can handle considerable energy under these conditions. You may also want to choose a large R_g value in order to reduce Electromagnetic Interference (EMI). When driving a lamp, you may want to use a very large resistor to limit in-rush current. Long-term reliability of the logic device will also be improved by using a gate resistor and/or a larger pull-up resistor. The gate resistor dissipates most the gate drive power losses, instead of the logic device, reducing stress on the logic output devices. A larger pull-up resistor limits the steady state on current in the pull-down transistors, thereby decreasing their power dissipation. However, using a large gate resistor will also increase the power MOSFET's susceptibility to noise and dv/dt turn on.

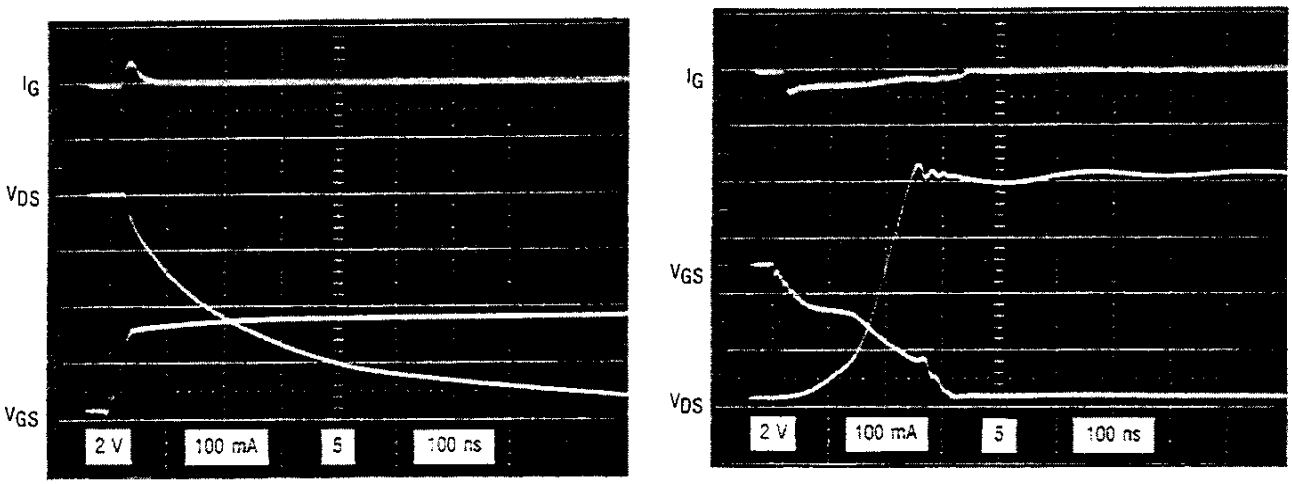
Logic gates on the same chip may be paralleled to increase switching speeds. The output current capability will increase in proportion to the number of gates used. If no gate resistor is used, the switching times will decrease in proportion to the number of gates used. If a gate resistor is used it may be safely decreased, in proportion to the number of gates, to decrease switching times. Paralleling logic gates will not change the total logic package power dissipation, since the output current increases and switching times decrease. When many gates are used, switching times may decrease to the point where they are limited by the stray inductance in the load and in the lay-out. Logic gates on different chips or from different families should not be paralleled because the different propagation delays may cause excessive shoot-through currents which might damage the logic devices.

Spare gates left over from a digital circuit may be used to drive a Logic Level power MOSFET. However, the large currents being used by the driver may cause large amounts of noise on the supply rail. This noise may cause data errors in the other gates on the same IC. Limiting the current with a large gate resistor and carefully decoupling the logic device will reduce the power supply noise. Also the driving logic device must be grounded at same point as the source of the power MOSFET to avoid ground shift problems caused by the large drain currents. If separate logic and analog grounds are used they should be connected only at the source of the power MOSFET.

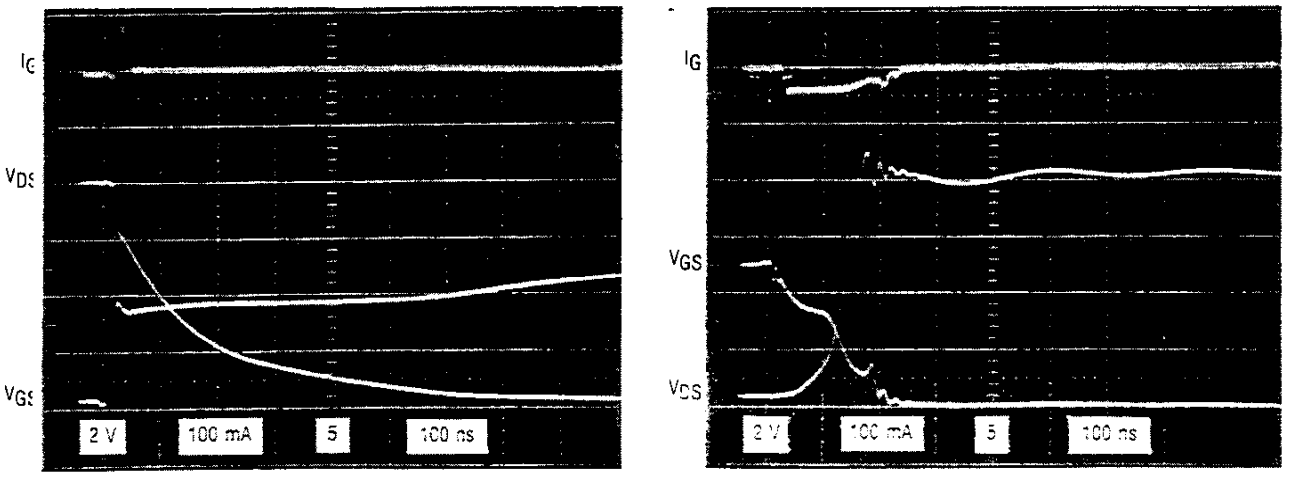
Pay close attention to the power supply scheme. The gate of a power MOSFET should never be left floating with voltage



(a) 74HC04



(b) 74LS04 Rp = 560 Ω



(c) 74F04 Rp = 220 Ω

Figure 11. Logic Devices Driving an MTP3055EL

applied to the drain. When this happens the power MOSFET may turn on and destroy itself if the current is not limited. If separate supplies are used for the load and the logic IC, the logic supply should be powered up first and powered down last. If this is not possible, consider what happens to the logic device output when power is removed. The pull-up resistors in the LS and FAST circuits of Figure 10 will pull the power MOSFET's gate down to V_{CC} when it is low, turning the power MOSFET off. The HC inverter's output, however, will be in a high impedance state when the logic supply voltage is low, allowing the power MOSFET's gate to float. A large resistor to the logic supply voltage or ground, or using a small signal diode to clamp the output to below the logic supply voltage, will solve this problem. Low logic supply voltage may also cause power MOSFET failure due to insufficient gate drive. When a power MOSFET fails the drain voltage will usually appear at it's gate, which may take out the entire logic circuit. A gate resistor will also limit the current under this power MOSFET failure condition.

INTERFACING TO A MICROPROCESSOR

Microprocessors can be easily interfaced to a Power MOSFET. Any of the circuits in Figure 10 can be used as a buffer between a microprocessor port and a Logic Level power MOSFET. If you want to use a standard power MOSFET, you will have to use the 'LS26 circuit in Figure 7 or a level shifter. The MC14504B hex level shifter can be used to interface HC, LS, or FAST to standard CMOS. This level shifter can be used to drive the Power MOSFET directly or with a buffer like the MC14049UB in Figure 5 to decrease switching times. The MC14504B has selectable TTL/CMOS level inputs and standard CMOS outputs. It can source and sink a maximum of about 20 mA using a 12 volt supply.

Be very careful when using bus drivers and latches which have tri-state outputs, like the 74LS240-74HC240 and 74LS373-74HC373, to drive a power MOSFET. The LS tri-state devices require a pull-up resistor to drive the power MOSFET to 5 volts, and will therefore leave the power MOSFET on when the outputs are disabled. The HC devices with tri-state outputs will let the gate float when the outputs are disabled, possibly damaging the power MOSFET. Tri-state devices can be used provided the output enable pin is tied true, low for negative logic enable inputs. HC tri-state devices do not require a pull-up resistor to drive a logic level power MOSFET, and may therefore be used with a pull-down resistor to ground. Note that tri-state outputs should never be pulled above the supply rail or below ground.

When simplicity is important, a single chip microcomputer like the 68HC11 can be used to drive a power MOSFET directly. This microcomputer may be used to perform functions like Pulse Width Modulation, complex motor speed control, and controlling multiple power MOSFETs for bridge applications. When the microcomputer is used in the single chip mode, any one of the 8 pins of parallel output port B can be used to drive a Logic Level power MOSFET. A large gate series resistor should be used to minimize power dissipation and noise on the chip. This means that switching times will be fairly slow. This arrangement also exposes the microprocessor to possible harm from power MOSFET failure. Although all the outputs of port B will be reset to zero on a Power-On Reset (POR), a pull down to ground should be used to ensure the power MOSFET will be off during power down. In some applications it may be necessary to initialize the power MOSFET gate drive via software before power is supplied to the power MOSFET.

Port B may also be used in a strobed mode by using the STRB signal from the control port D. The STRB signal will go high after the data on port B is valid and may be used to latch or enable a logic device driving a power MOSFET. This mode may be useful when exact synchronization is desired between the microprocessor controlled devices.

When used in the extended memory mode, ports B and C are used for address and data busses. The 68HC24 port replacement unit will replace port B in a software transparent fashion. Thus, a system can be developed using the 68HC11 with a 68HC24 and external memory, while the final product will use only the 68HC11.

CONCLUSION

We have seen that standard Power MOSFETs can be interfaced directly to standard CMOS logic with very good performance, about 50 ns rise and fall times for the MC14049UB driving a 12 Amp power MOSFET. Standard Power MOSFETs may also be interfaced to 5 volt logic using a special interface device such as the 74LS26 open collector NAND gate or the MC14504B hex level shifter. The 74LS26 driving a 12 Amp standard Power MOSFET gives turn on times of about 1 μs and fast turn off times of less than 200 ns. Switching times may be easily estimated using four simple equations and a series resistor may be selected to give the desired rise and fall times.

Logic Level Power MOSFETs can be driven directly with HC logic, and by LS logic with the addition of a pull-up resistor. Switching speeds using an HC device are very fast, less than 150 ns per gate when driving a 12 Amp power MOSFET. Using an LS device, turn on speed is good, about 0.5 μs, and turn off speed is excellent, less than 150 ns. Again, switching speeds may be easily estimated and a series resistor may be selected to give the desired performance.

Logic power supply variations are the most important aspect affecting Logic Level Power MOSFET performance. Power supply sequencing and under-voltage protection is necessary to ensure system integrity. Circuit lay-out and power supply decoupling are also important at high speeds.

Finally a Logic Level Power MOSFET may be interfaced directly to a dedicated microprocessor output port when microprocessor control is desired.

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