FUJITSU SEMICONDUCTOR
DATA SHEET

DS501-00007-0v01-E

Memory FRAM

256 K (32 K × 8) Bit SPI

MB85RS256A

■ DESCRIPTION

MB85RS256A is a FRAM (Ferroelectric Random Access Memory) chip in a configuration of 32,768 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the non-volatile memory cells.
MB85RS256A adopts the Serial Peripheral Interface (SPI).
The MB85RS256A is able to retain data without using a back-up battery, as is needed for SRAM.
The memory cells used in the MB85RS256A can be used for 10^{10} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E^2PROM.
MB85RS256A does not take long time to write data unlike Flash memories nor E^2PROM, and MB85RS256A takes no wait time.

■ FEATURES

- Bit configuration : 32,768 words × 8 bits
- Operating power supply voltage : 3.0 V to 3.6 V
- Operating frequency : 25 MHz (Max)
- Serial Peripheral Interface : SPI (Serial Peripheral Interface)
  Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating temperature range : –40 °C to +85 °C
- Data retention : 10 years (+55 °C)
- High endurance : 10 Billion Read/writes
- Package : 8-pin plastic SOP (FPT-8P-M02)

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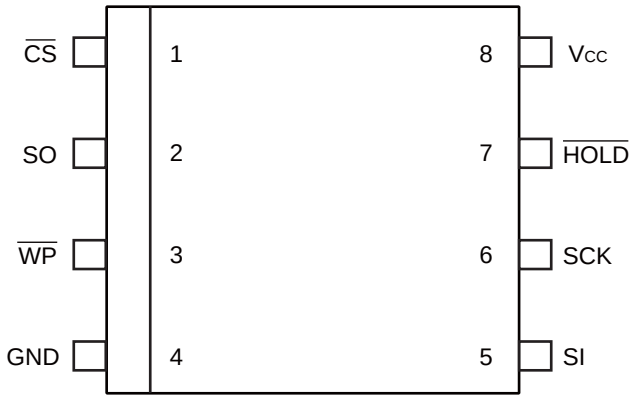
■ PIN ASSIGNMENT

(TOP VIEW)

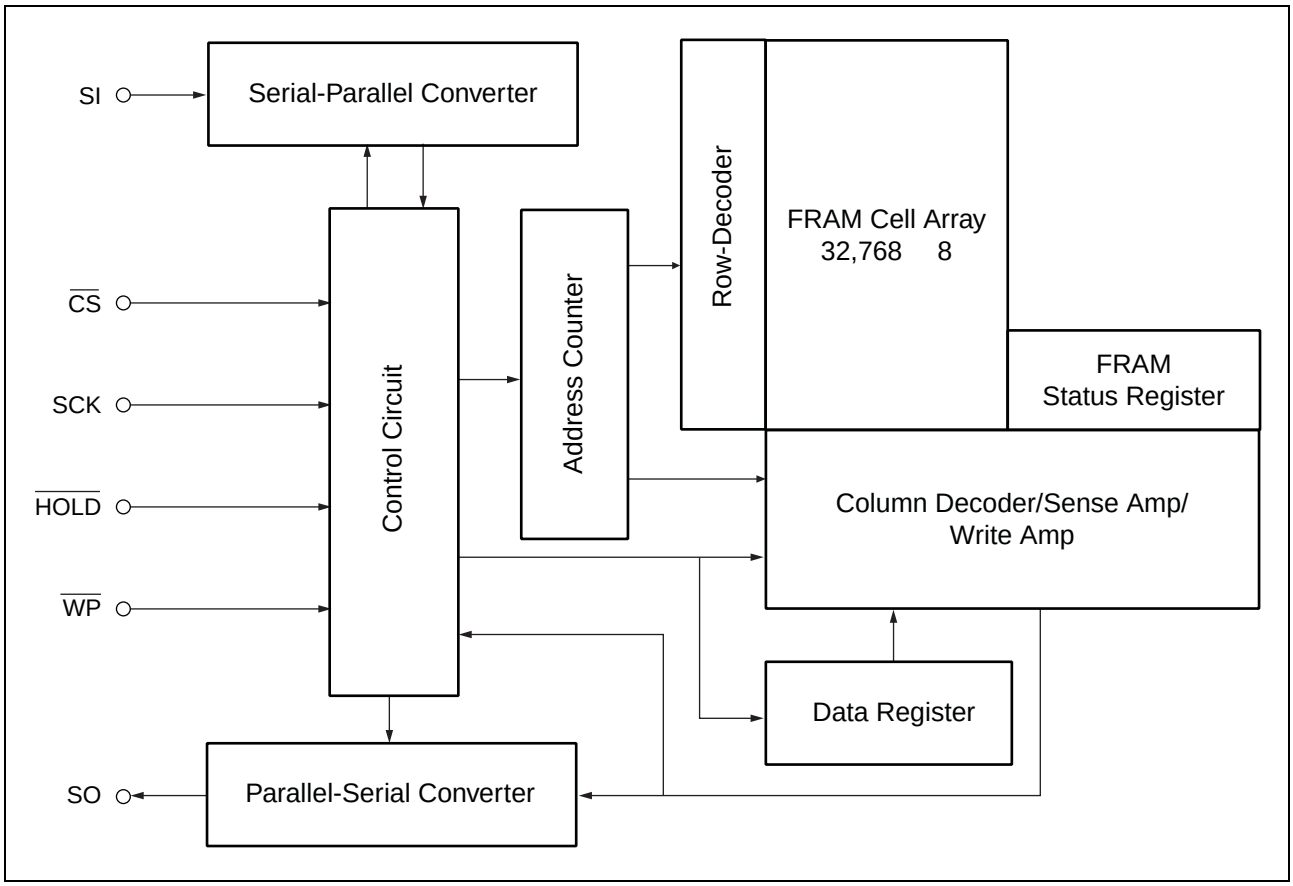


(FPT-8P-M02)

■ PIN FUNCTIONAL DESCRIPTIONS

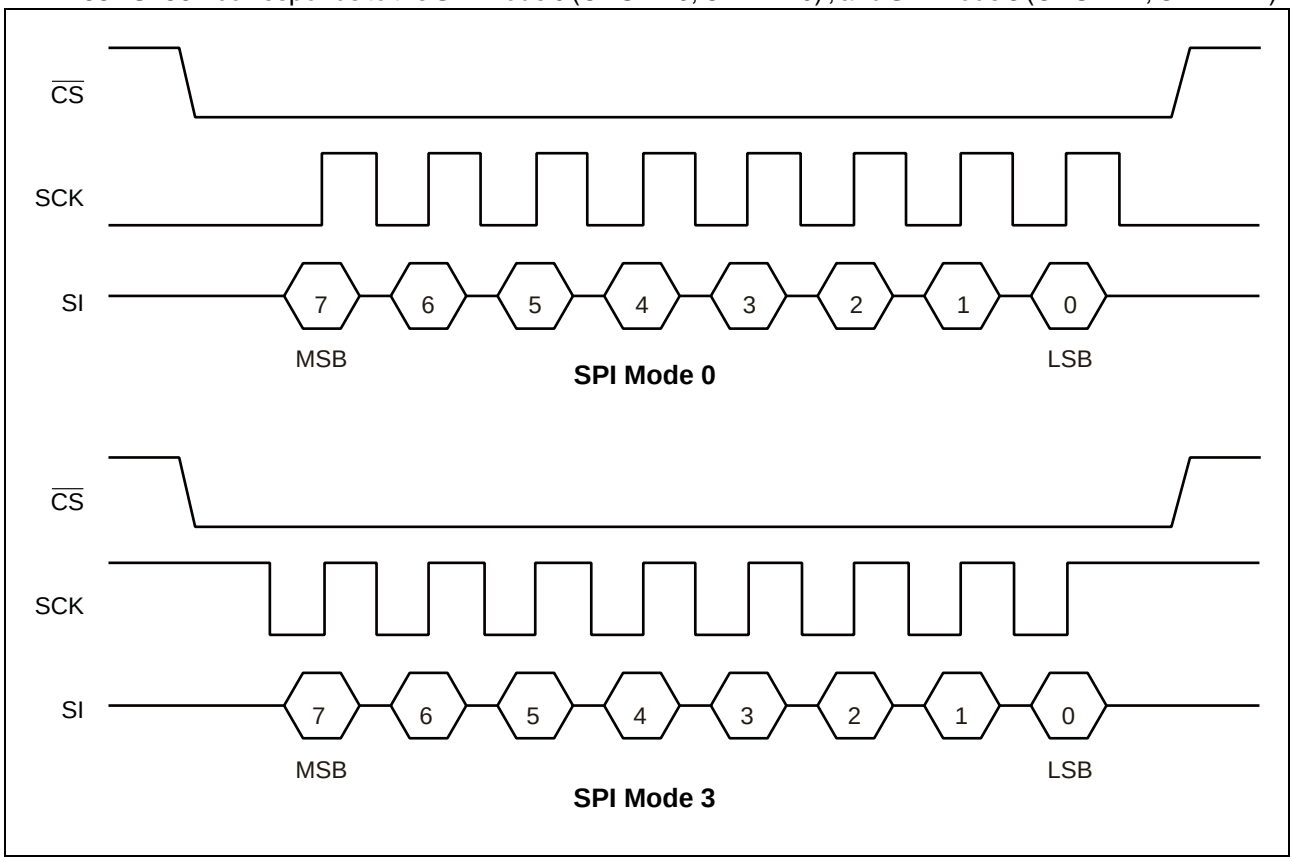
Pin No.	Pin Name	Functional description
1	$\overline{CS}$	Chip Select This is an input pin to make chips select. When $\overline{CS}$ is “H”, device is in deselect (standby) status as long as device is not write status internally, and SO becomes High-Z. Other inputs from pins are ignored for this time. When $\overline{CS}$ is “L”, device is in select (active) status. $\overline{CS}$ has to be “L” before inputting op-code.
3	$\overline{WP}$	Write Protect This is a pin to control writing to a status register. When $\overline{WP}$ is “L”, writing to a status register is not operated.
7	$\overline{HOLD}$	Hold This pin is used to interrupt serial input/output without making chips deselect. When $\overline{HOLD}$ is “L”, hold operation is activated, SO becomes High-Z, SCK and SI become don’t care. While the hold operation, $\overline{CS}$ has to be retained “L”.
6	SCK	Serial Clock This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output This is an output pin of serial data. Reading data of FRAM memory cell array and status register data are output. This is High-Z during standby.
8	V_{CC}	Supply Voltage
4	GND	Ground

■ BLOCK DIAGRAM



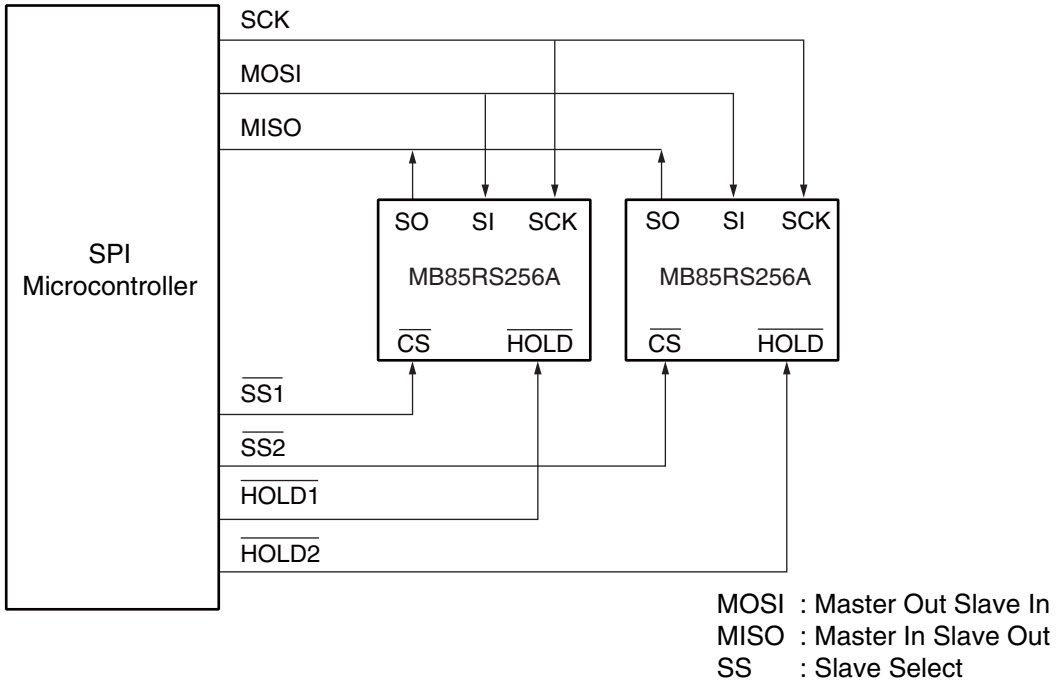
■ SPI MODE

MB85RS256A corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0) , and SPI mode 3 (CPOL = 1, CPHA = 1) .

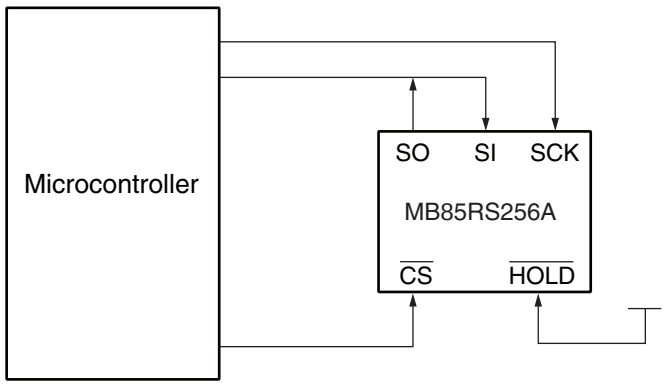


■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS256A works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.



System Configuration with SPI Port



System Configuration without SPI Port

STATUS REGISTER

Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FRAM). WPEN is related to $\overline{WP}$ input to protect writing to a status register (refer to " WRITING PROTECT"). Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4		Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible, and "000" is written before shipment. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory (FRAM). This defines block size for writing protect with the WRITE command (refer to " BLOCK PROTECT"). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This indicates FRAM memory and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. The time when power is up. The time when the WRDI command is input. The time when the WRSR command is input. The time when the WRITE command is input.
0	0	This is a bit fixed to "0".

OP-CODE

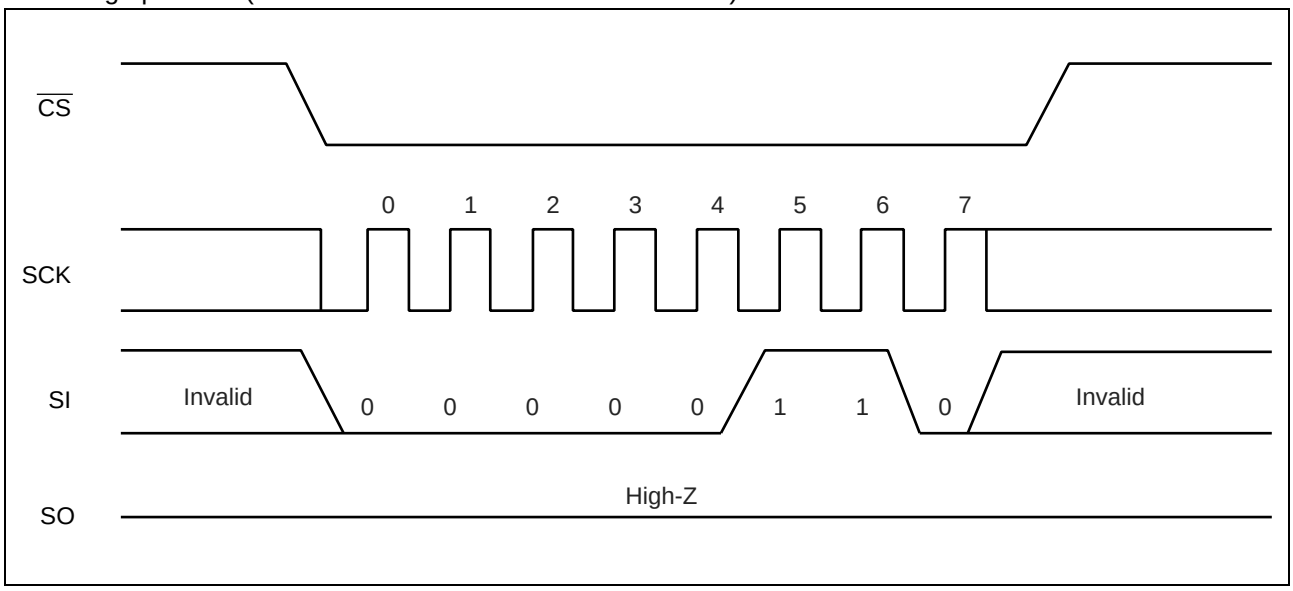
MB85RS256A accepts 6 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If $\overline{CS}$ is risen while inputting op-code, the command are not performed.

Name	Description	Op-code
WREN	Set Write Enable Latch	$0000\ 0110_B$
WRDI	Reset Write Enable Latch	$0000\ 0100_B$
RDSR	Read Status Register	$0000\ 0101_B$
WRSR	Write Status Register	$0000\ 0001_B$
READ	Read Memory Code	$0000\ 0011_B$
WRITE	Write Memory Code	$0000\ 0010_B$

COMMAND

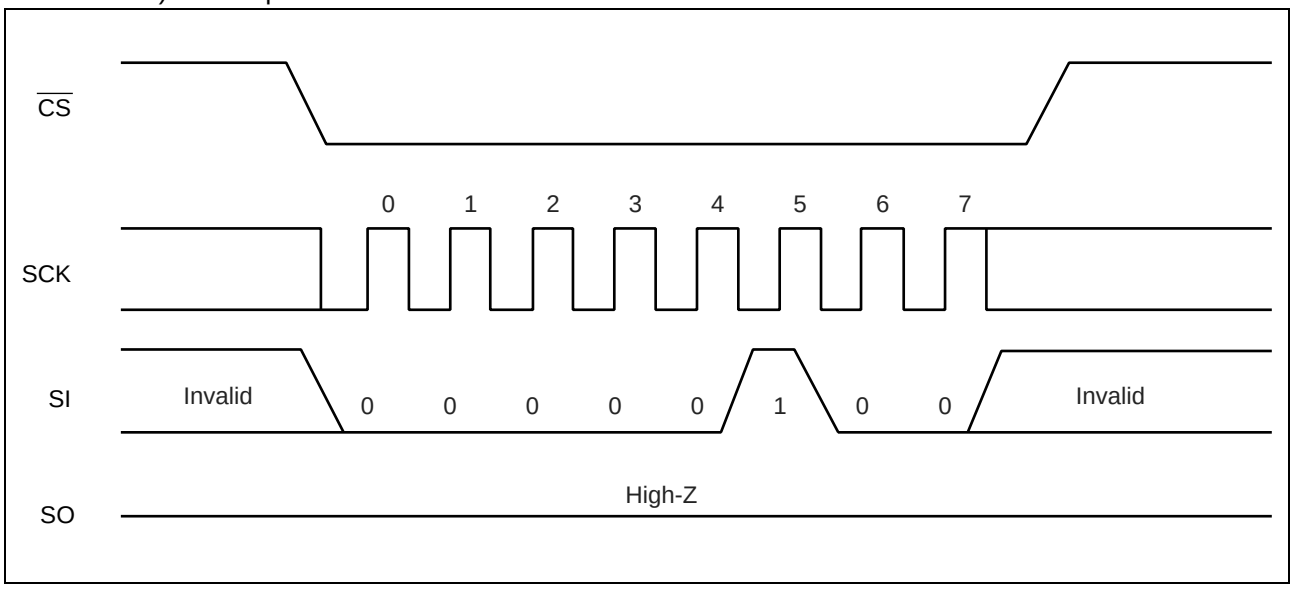
€ WREN

The WREN command sets WEL (Write Enable Latch) . WEL has to be set with the WREN command before writing operation (WRSR command and WRITE command) .



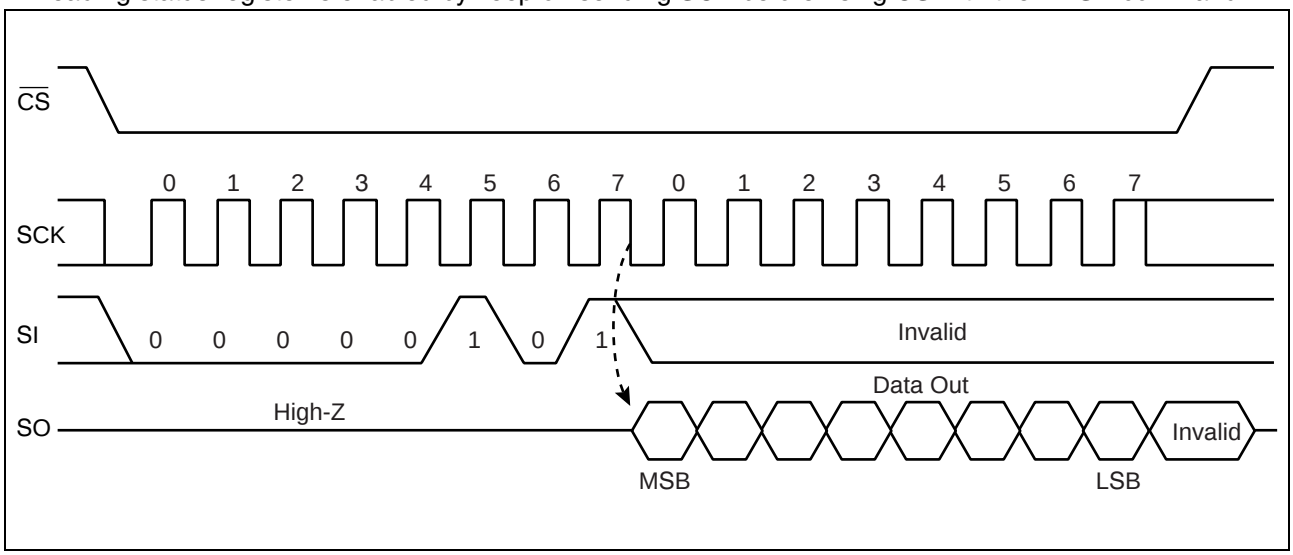
€ WRDI

The WRDI command resets WEL (Write Enable Latch) . Writing operation (WRITE command and WRSR command) are not performed when WEL is reset.



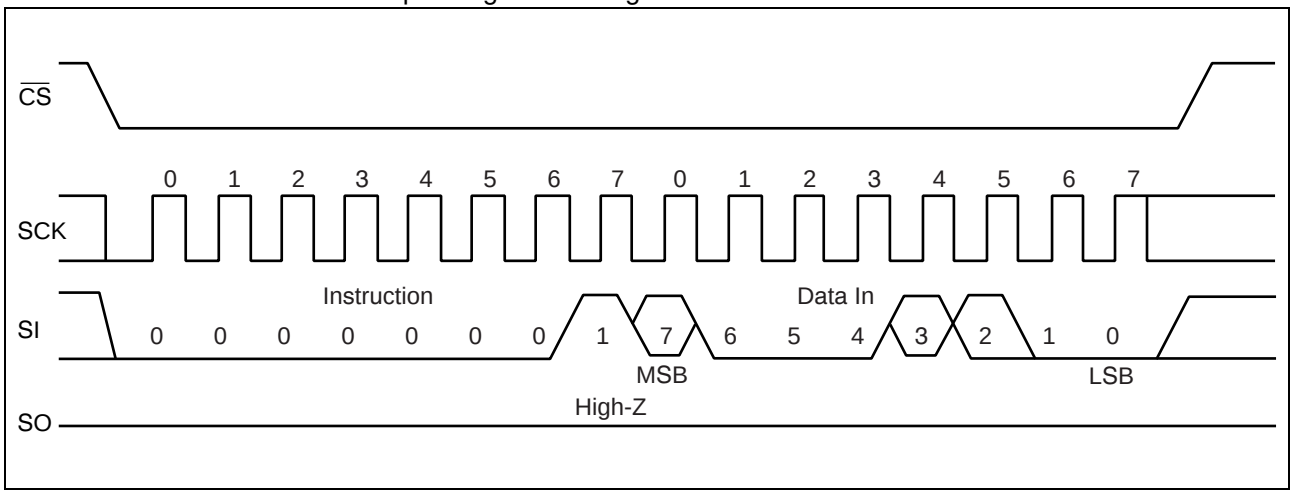
• **RDSR**

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. Continuously reading status register is enabled by keep on sending SCK before rising $\overline{CS}$ with the RDSR command.



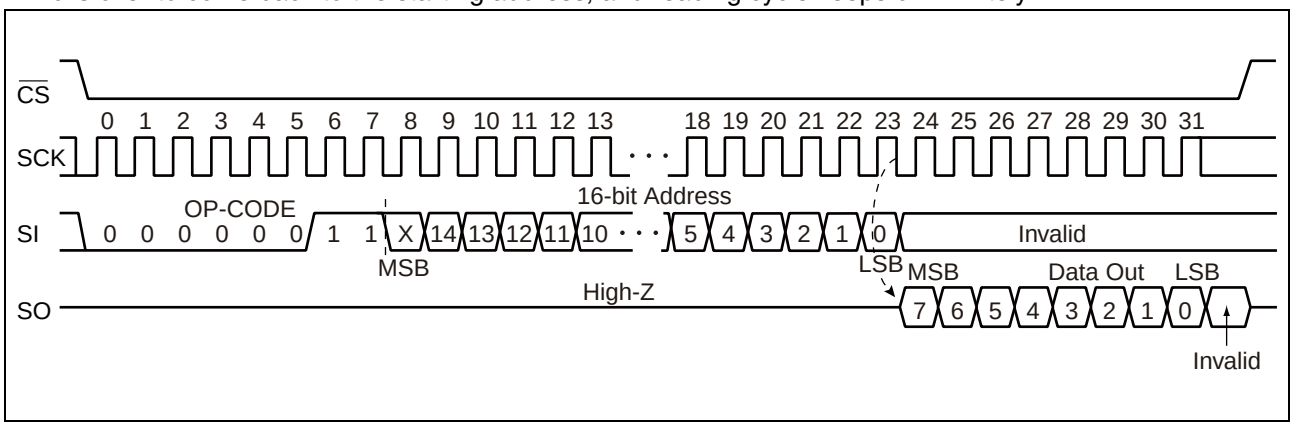
• **WRSR**

The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. a SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to “0” and cannot be written. The SI value corresponding to bit 0 is ignored.



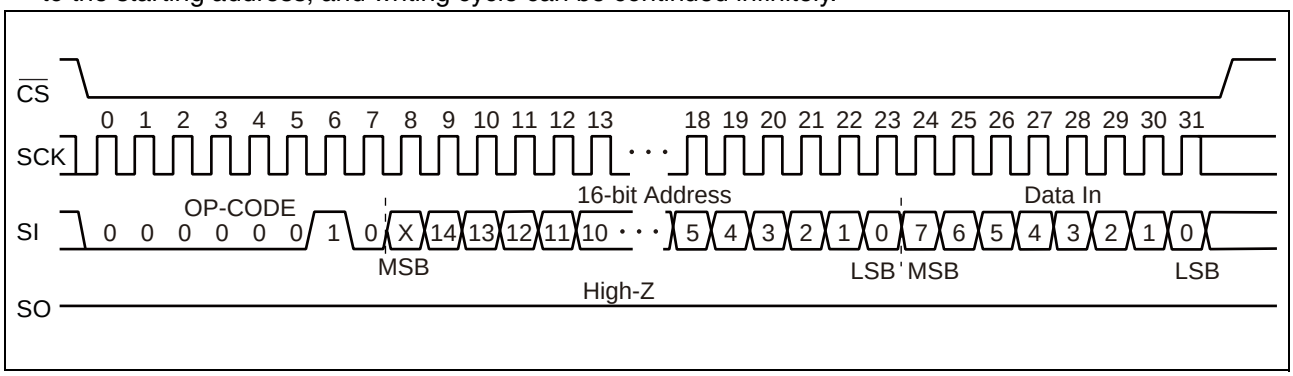
• **READ**

The READ command reads FRAM memory cell array data. Arbitrary 16 bits address and op-code of READ are input to SI. The most significant address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{CS}$ is risen, the READ command is completed, but keep on reading address with automatic increment is enabled by continuously sending clock for 8 cycles each to SCK before $\overline{CS}$ is risen. When it reaches the most significant address, it rolls over to come back to the starting address, and reading cycle keeps on infinitely.



• **WRITE**

The WRITE command writes data to FRAM memory cell array. WRITE op-code, arbitrary 16 bits of address and 8 bits of writing data are input to SI. The most significant address bit is invalid. When 8 bits of writing data is input, data is written to FRAM memory cell array. Risen $\overline{CS}$ will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before $\overline{CS}$ is risen, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over, comes back to the starting address, and writing cycle can be continued infinitely.



■ BLOCK PROTECT

Writing protect block is configured by the WRITE command with BP1, BP0 value of the status register.

BP1	BP0	Protected Block
0	0	None
0	1	6000_H to $7FFF_H$ (upper 1/4)
1	0	4000_H to $7FFF_H$ (upper 1/2)
1	1	0000_H to $7FFF_H$ (all)

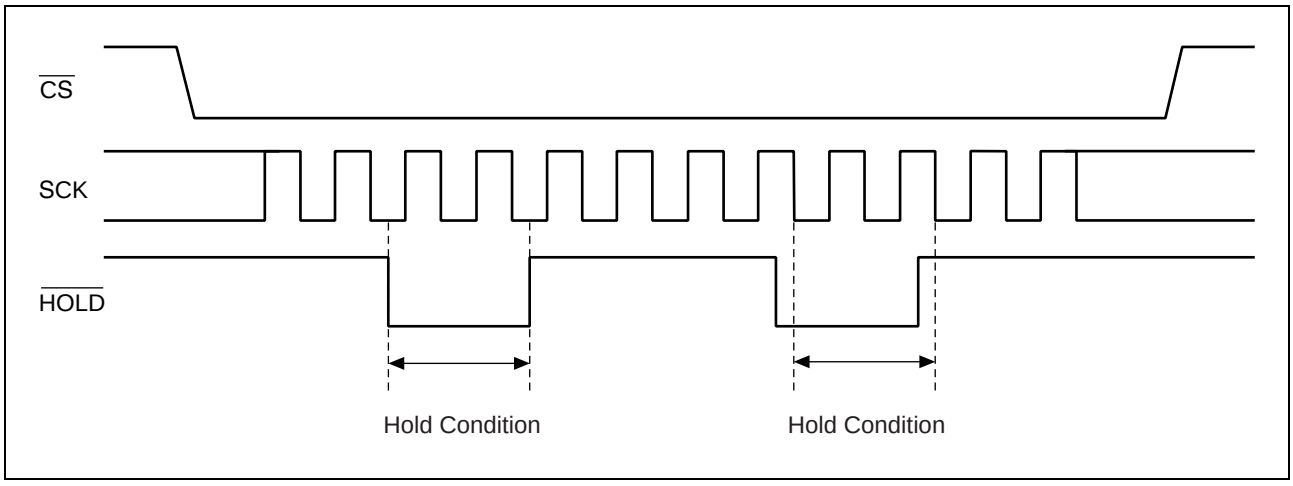
■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, $\overline{WP}$ as shown in the table.

WEL	WPEN	$\overline{WP}$	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

■ HOLD OPERATION

Hold status is retained without aborting a command if $\overline{HOLD}$ is “L” while $\overline{CS}$ is “L”. The timing for starting and ending hold status depends on the SCK to be “H” or “L” when a $\overline{HOLD}$ pin input is transited as shown in the diagram below. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become don’t care. And, SO becomes High-Z while reading command (RDSR, READ) . If $\overline{CS}$ is risen with hold status, a command is aborted and device is reset.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{CC}	− 0.5	+ 4.0	V
Input voltage*	V_{IN}	− 0.5	V_{CC} + 0.5	V
Output voltage*	V_{OUT}	− 0.5	V_{CC} + 0.5	V
Operating temperature	T_A	− 40	+ 85	°C
Storage temperature	Tstg	− 40	+ 125	°C

*:These parameters are based on the condition that V_{SS} is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*	V_{CC}	3.0	3.3	3.6	V
Input high voltage*	V_{IH}	$V_{CC} \times 0.8$	—	V_{CC} + 0.5	V
Input low voltage*	V_{IL}	− 0.5	—	+ 0.6	V
Operating temperature	T_A	− 40	—	+ 85	°C

*:These parameters are based on the condition that V_{SS} is 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	—	—	10	µA
Output leakage current	I_{LO}	V_{OUT} = 0 V to V_{CC}	—	—	10	µA
Operating power supply current	I_{CC}	SCK = 25 MHz	—	5	10	mA
Standby current	I_{SB}	All inputs V_{SS} or SCK = SI = $\overline{CS}$ = V_{CC}	—	3	50	µA
Output high voltage	V_{OH}	I_{OH} = –2 mA	$V_{CC} \times 0.8$	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V

2. AC Characteristics

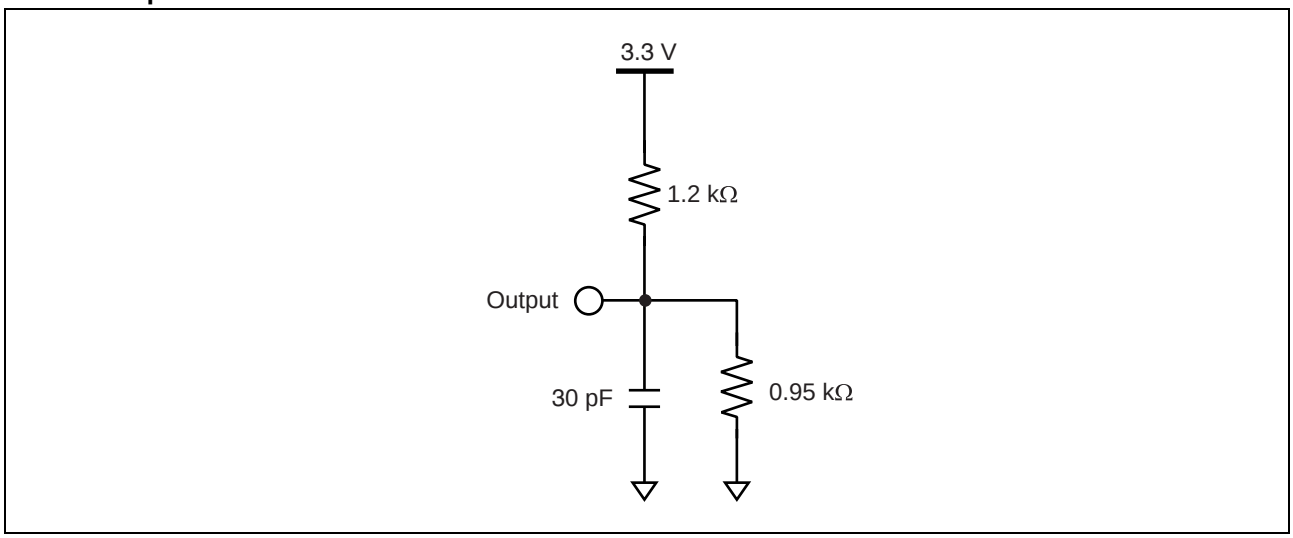
(within recommended operating conditions)

Parameter	Symbol	Value		Unit
		Min	Max	
SCK clock frequency	f_{CK}	0	25	MHz
Clock high time	t_{CH}	20	—	ns
Clock low time	t_{CL}	20	—	ns
Chip select set up time	t_{CSU}	10	—	ns
Chip select hold time	t_{CSH}	10	—	ns
Output disable time	t_{OD}	—	20	ns
Output data valid time	t_{ODV}	—	18	ns
Output hold time	t_{OH}	0	—	ns
Deselect time	t_{D}	60	—	ns
Data in rise time	t_{R}	—	50	ns
Data fall time	t_{F}	—	50	ns
Data set up time	t_{SU}	5	—	ns
Data hold time	t_{H}	5	—	ns
$\overline{\text{HOLD}}$ set up time	t_{HS}	10	—	ns
$\overline{\text{HOLD}}$ hold time	t_{HH}	10	—	ns
$\overline{\text{HOLD}}$ output floating time	t_{HZ}	—	20	ns
$\overline{\text{HOLD}}$ output active time	t_{LZ}	—	20	ns

AC Test Condition

Power supply voltage : 3.0 V to 3.6 V
Operation temperature : − 40 °C to + 85 °C
Input voltage magnitude : 0.3 V to 2.7 V
Input rising time : 5 ns
Input falling time : 5 ns
Input judge level : $V_{CC}/2$
Output judge level : $V_{CC}/2$

AC Load Equivalent Circuit

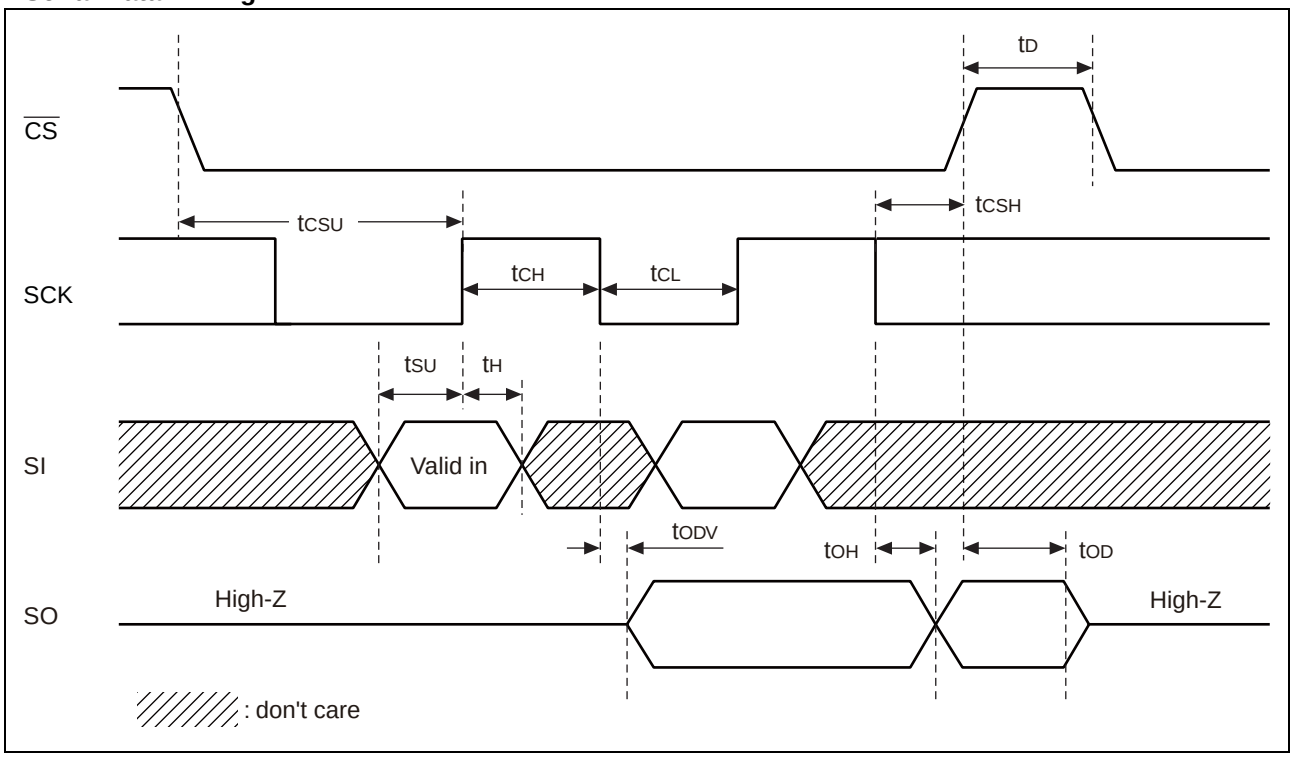


3. Pin Capacitance

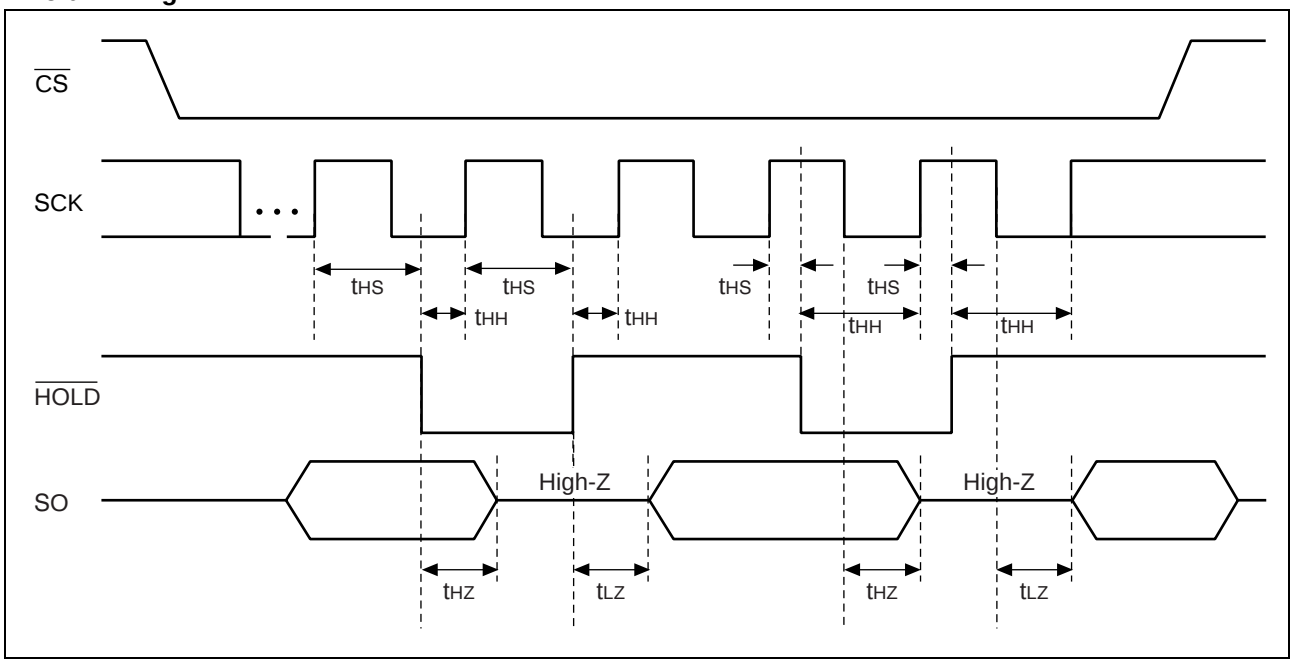
Parameter	Symbol	Value		Unit
		Min	Max	
Output capacitance	C_O	—	10	pF
Input capacitance	C_I	—	10	pF

■ TIMING DIAGRAM

• Serial Data Timing



• Hold Timing



■ ORDERING INFORMATION

Part number	Package	Remarks
TBD	8-pin plastic SOP (FPT-8P-M02)	
TBD	8-pin plastic SOP (FPT-8P-M02)	Embossed Carrier tape

Note : Please confirm the ordering information with the sales representatives.

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