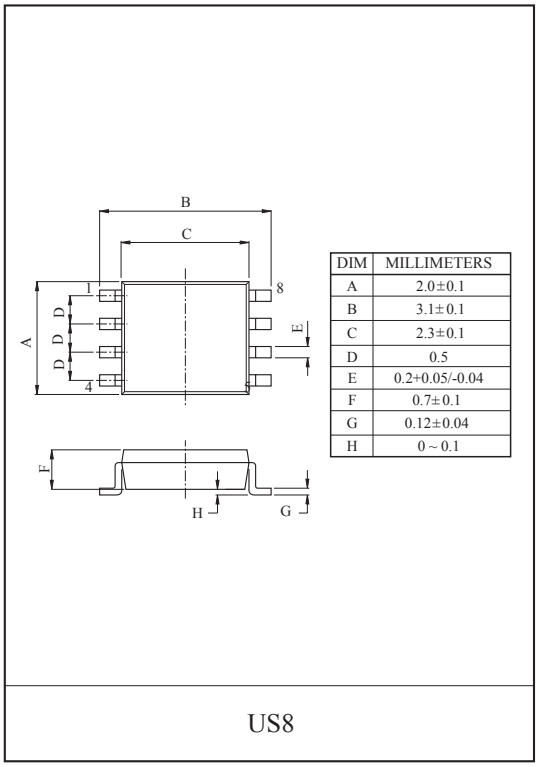
KIC7WZ125FK

SILICON MONOLITHIC CMOS DIGITAL INTEGRATED CIRCUIT

DUAL BUS BUFFER

FEATURES

- Super High Speed : t_{PD}=2.6ns(Typ.) into 50pF at V_{CC}=5V.
- High Output Driver : ±24mA at V_{CC}=3V.
- Power Down High Impedance inputs/outputs.
- Outputs are Overvoltage Tolerant is 3-STATE mode.
- Wide Operating Voltage Range : $V_{CC(opr)}$=1.65~5.5V.



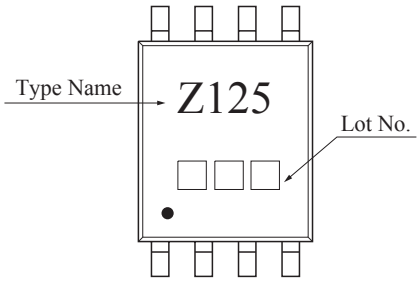
DIM	MILLIMETERS
A	2.0±0.1
B	3.1±0.1
C	2.3±0.1
D	0.5
E	0.2+0.05/-0.04
F	0.7±0.1
G	0.12±0.04
H	0 ~ 0.1

US8

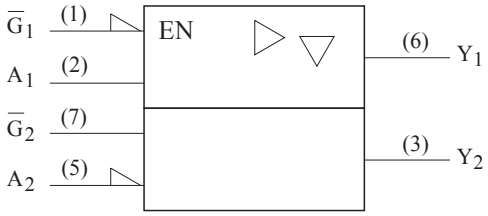
MAXIMUM RATINGS (Ta=25℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~7	V
DC Output Voltage	V_{OUT}	-0.5~7	V
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	-50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	200	mW
Storage Temperature Range	T_{stg}	-65 ~ 150	℃
Lead Temperature (10s)	T_L	260	℃

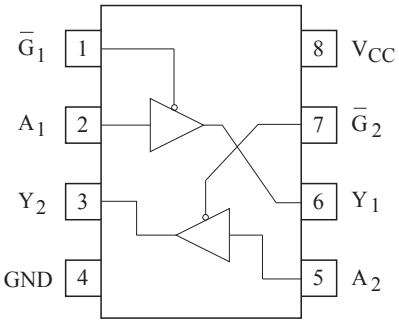
MARKING



Logic Diagram



PIN CONNECTION(TOP VIEW)



Truth Table

INPUTS		OUTPUTS
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

X : Don t Care

Z : High Impedance

Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	1.65~5.5	V
		1.5~5.5 (Note1)	
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC} (Note2)	V
		0~5.5 (Note3)	
Operating Temperature	T_{opr}	-40~85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 20 (V_{CC}=1.8±0.15V, 2.5±0.2V) 0 ~ 10 (V_{CC}=3.3V±0.3V) 0 ~ 5 (V_{CC}=5.0V±0.5V)	ns/V

Note1 : Data retention only. Note2 : Active State. Note3 : 3-STATE

ELECTRICAL CHARACTERISTICS (DC Characteristics)

CHARACTERISTIC		SYMBOL	TEST CONDITION			Ta=25℃			Ta=-40~85℃		UNIT
					V_{CC}(V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Input Voltage	High Level	V_{IH}	-		1.65~1.95	0.75× V_{CC}	-	-	0.75× V_{CC}	-	V
					2.3~5.5	0.7×V_{CC}	-	-	0.7×V_{CC}	-	
	Low Level	V_{IL}	-		1.65~1.95	-	-	0.25× V_{CC}	-	0.25× V_{CC}	
					2.3~5.5	-	-	0.3×V_{CC}	-	0.3×V_{CC}	
Output Voltage	High Level	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-100μA	1.65	1.55	1.65	-	1.55	-	V
					2.3	2.2	2.3	-	2.2	-	
					3.0	2.9	3.0	-	2.9	-	
					4.5	4.4	4.5	-	4.4	-	
				I_{OH}=-4mA	1.65	1.29	1.52	-	1.29	-	
				I_{OH}=-8mA	2.3	1.9	2.15	-	1.9	-	
				I_{OH}=-16mA	3.0	2.4	2.80	-	2.4	-	
				I_{OH}=-24mA	3.0	2.3	3.68	-	2.3	-	
				I_{OH}=-32mA	4.5	3.8	4.20	-	3.8	-	
	Low Level	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=100μA	1.65	-	0	0.1	-	0.1	V
					2.3	-	0	0.1	-	0.1	
					3.0	-	0	0.1	-	0.1	
					4.5	-	0	0.1	-	0.1	
				I_{OL}=4mA	1.65	-	0.08	0.24	-	0.24	
				I_{OL}=8mA	2.3	-	0.10	0.30	-	0.30	
				I_{OL}=16mA	3.0	-	0.15	0.40	-	0.40	
				I_{OL}=24mA	3.0	-	0.22	0.55	-	0.55	
				I_{OL}=32mA	4.5	-	0.22	0.55	-	0.55	
Input Leakage Current		I_{IN}	V_{IN}=5.5V or GND		0~5.5	-	-	±0.1	-	±1	μA
3-STATE Output Leakage		I_{OZ}	V_{IN}=V_{IH} or V_{IL} 0≤V_{OUT}≤5.5V		1.65~5.5	-	-	±0.5	-	±5	μA
Power Off Leakage Current		I_{OFF}	V_{IN} or V_{OUT}=5.5V		0.0	-	-	1	-	10	μA
Quiescent Supply Current		I_{CC}	V_{IN}=5.5V or GND		1.65~5.5	-	-	1	-	10	μA

Noise Characteristics

CHARACTERISTIC	SYMBOL	TEST CONDITION		Ta=-25℃		UNIT
			V_{CC}(V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP} (Note 1)	C_L=50pF	5.0	-	1.0	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV} (Note 1)	C_L=50pF	5.0	-	1.0	V
Quiet Output Minimum Dynamic V_{OH}	V_{OHV} (Note 1)	C_L=50pF	5.0	-	4.0	V
Minimum HIGH Level Dynamic Input Voltage	V_{IHD} (Note 1)	C_L=50pF	5.0	-	3.5	V
Maximum LOW Level Dynamic Input Voltage	V_{ILD} (Note 1)	C_L=50pF	5.0	-	1.5	V

Note 1 : Characteristic guaranteed by design.

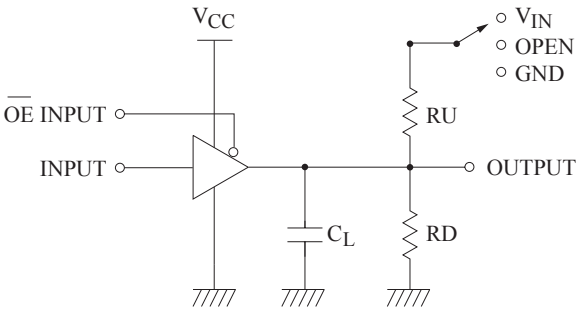
AC Characteristics

CHARACTERISTIC	SYMBOL	TEST CONDITION		Ta=25℃			Ta=-40~85℃		UNIT
			V_{CC}(V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay A_N to Y_N (Figures 1,3)	t_{PLH} t_{PHL}	C_L=15pF, R_D=1MΩ S1=Open	1.8±0.15	2.0	-	12.0	2.0	13.0	ns
			2.5±0.2	1.0	-	7.5	1.0	8.0	
			3.3±0.3	0.8	-	5.2	0.8	5.5	
			5.0±0.5	0.5	-	4.5	0.5	4.8	
	t_{PLH} t_{PHL}	C_L=50pF, R_D=500Ω S1=Open	3.3±0.3	1.2	-	5.7	1.2	6.0	ns
			5.0±0.5	0.8	-	5.0	0.8	5.3	
Output to Output Skew (Figures 1,3) (Note 2)	t_{OSLH} t_{OSHL}	C_L=50pF, R_D=500Ω S1=Open	3.3±0.3	-	-	1.0	-	1.0	ns
			5.0±0.5	-	-	0.8	-	0.8	
Output Enable Time (Figures 1,3)	t_{PZL} t_{PZH}	C_L=50pF, R_D, R_U=500Ω S1=GND for t_{PZH} S1=V_1 for t_{PZL} V_1=2×V_{CC}	1.8±0.15	3.0	-	14.0	3.0	15.0	ns
			2.5±0.2	1.8	-	8.5	1.8	9.0	
			3.3±0.3	1.2	-	6.2	1.2	6.5	
			5.0±0.5	0.8	-	5.5	0.8	5.8	
Output Disable Time (Figures 1,3)	t_{PLZ} t_{PHZ}	C_L=50pF, R_D, R_U=500Ω S1=GND for t_{PZH} S1=V_1 for t_{PZL} V_1=2×V_{CC}	1.8±0.15	2.5	-	12.0	2.5	13.0	ns
			2.5±0.2	1.5	-	8.0	1.5	8.5	
			3.3±0.3	0.8	-	5.7	0.8	6.0	
			5.0±0.5	0.3	-	4.7	0.3	5.0	
Input Capacitance	C_{IN}		0	-	2.5	-	-	-	pF
Output Capacitance	C_{OUT}		5.0	-	4	-	-	-	pF
Power Dissipation Capacitance (Figure 2)	C_{PD}	(Note 3)	3.3	-	10	-	-	-	pF
			5.0	-	12	-	-	-	

Note 2 : Characteristic guaranteed by design. t_{OSLH}=|t_{PLHmax}-t_{PLHmin}| ; t_{OSHL}=|t_{PHLmax}-t_{PHLmin}|.

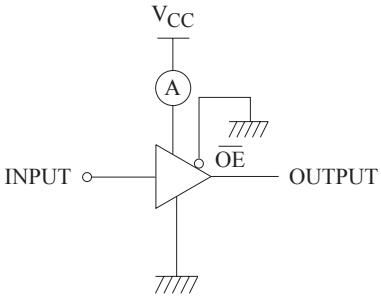
Note 3 : C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the exprssion : I_{CCD}=C_{PD} · V_{CC} · f_{IN}+I_{CC}

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR=1.0MHz ; t_W =500ns

FIGURE 1. AC Test Circuit



Input=AC Waveform ; t_r=t_f=1.8ns;
PRR=10MHz ; Duty Cycle=50%

FIGURE 2. I_{CCD} Test Circuit

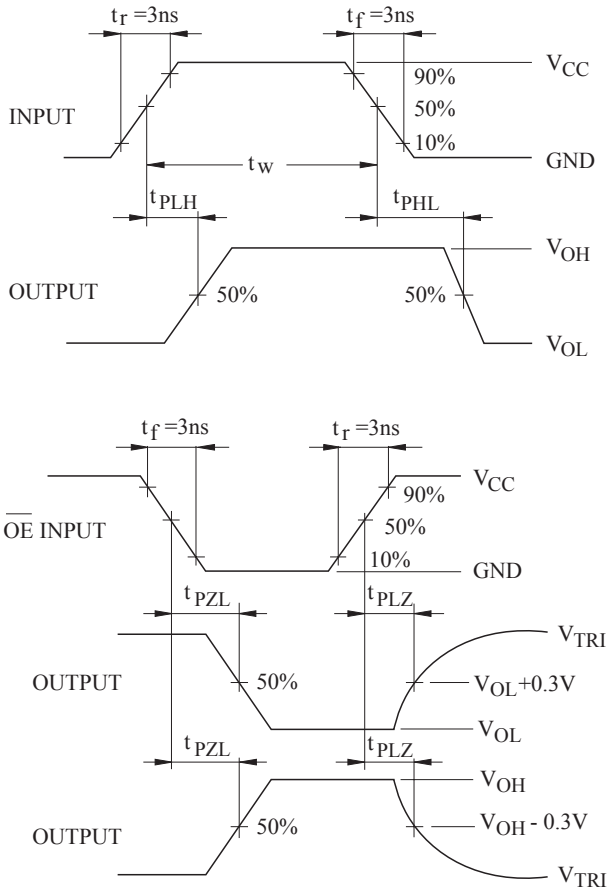


FIGURE 3. AC Waveforms