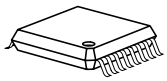
GaAs MMIC

CGY 360

Data Sheet

- WLL receive downconverter IC for 3.5 GHz
- Fully Integrated Two-Stage Preamplifier, Mixer, LO-Buffer, IF Amplifier and two Switched Attenuators
- Very high Input-*IP3* of typical + 5 dBm at max. gain and + 28 dBm at min. gain
- Very low LO-Power demand of typ. – 5 to 0 dBm
- High Conversion Gain: typ. 19 dB
- Minimum of external components and easy matching
- Total Current Consumption: typ. 90 mA @ 5 V
- Temperature Range: – 40 °C to + 85 °C



MW-16

ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precautions!

Type	**Marking**	**Ordering Code** (tape and reel)	**Package**
CGY 360	CGY 360	Q62702-G98	MW-16

Maximum Ratings	**Port**	**Symbol**	**Limit Values**		**Unit**
			min.	**max.**	
Positive Supply Voltage	3, 4, 11, 15	V_{DLO}, V_{DRF2}, V_{DRF1}, V_{DIF}	0	+ 6	V
Negative Supply Voltage	13	V_G	0	–	V
Voltage at Step Attenuators	6, 7, 9, 10	A, A bar, B bar, B	0	+ 6	V
Power into RF Input	8	RF	–	10	dBm
Power into LO Input	1	LO	–	10	dBm
Channel Temperature	–	T_{Ch}	–	150	°C
Storage Temperature	–	T_{stg}	– 55	150	°C

Thermal Resistance	Symbol	Value	Unit
Channel to Soldering Point (GND)	R_{thChS}	t.b.d.	K/W

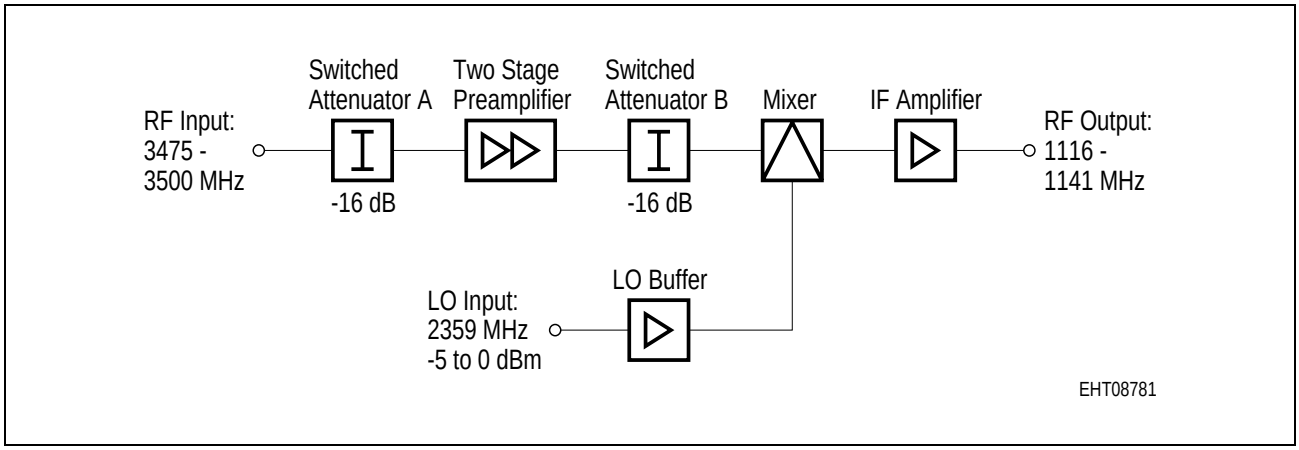


Figure 1 RF Block Diagram

Electrical Characteristics

T_A = 25 °C; V_{DD} = 5 V, V_{GG} = – 5 V; f_{RF} = 3475 - 3500 MHz; f_{LO} = 2359 MHz; P_{LO} = 0 dBm; P_{RF} = – 20 dBm; f_{IF} = 1116 - 1141 MHz, attenuators “OUT” or “IN”.

Characteristics	Symbol	Limit Values			Unit
		min.	typ.	max.	
Operating Drain Current	I_{op}	–	90	–	mA
Operating Drain Current LO Buffer only (P_{LO} = 0 dBm)	I_{LO}	–	10	–	mA
Operating Gate Current	I_g	–	0.7	–	mA

Electrical Characteristics

As above, but attenuators “OUT” (for further information about the attenuators see “Attenuator State” on **Page 5**).

Characteristics	Symbol	Limit Values			Unit
		min.	typ.	max.	
Conversion Gain	G_c	–	19.0	–	dB
SSB Noise Figure	F_{ssb}	–	6.0	–	dB
3rd Order Input Intercept Point at max. gain	$IP3_{in}$	–	+ 5	–	dBm

Electrical Characteristics (cont'd)
As above, but attenuators "OUT" (for further information about the attenuators see "Attenuator State" on **Page 5**).

Characteristics	Symbol	Limit Values			Unit
		min.	typ.	max.	
LO Leakage at RF-Port with 0 dBm LO Input	P_{LO}	–	– 28	–	dBm
LO Leakage at IF-Port with 0 dBm LO Input	P_{LO}	–	– 19	–	dBm
Return Loss RF Port[1)]	S_{11}	–	14	–	dB
Return Loss IF Port[1)]	S_{22}	–	11	–	dB
Return Loss LO Port[1)]	S_{11}	–	9	–	dB

1) Configuration as shown on application board.

As above, but attenuator A "OUT" and attenuator B "IN" or attenuator A "IN" and attenuator B "OUT" (for further information about the attenuators see "Attenuator State" on **Page 5**).

Characteristics	Symbol	Limit Values			Unit
		min.	typ.	max.	
Conversion Gain	G_c	–	3.0	–	dB
SSB Noise Figure (A "IN", B "OUT")	F_{ssb}	–	16.0	–	dB
3rd Order Input Intercept Point (A "IN", B "OUT")	$IP3_{in}$	–	+ 18	–	dBm

As above, but attenuator A "IN" and attenuator B "IN" (for further information about the attenuators see "Attenuator State" on **Page 5**).

Characteristics	Symbol	Limit Values			Unit
		min.	typ.	max.	
Conversion Gain	G_c	–	– 13.0	–	dB
SSB Noise Figure	F_{ssb}	–	35.0	–	dB
3rd Order Input Intercept Point at min. gain	$IP3_{in}$	–	+ 28	–	dBm

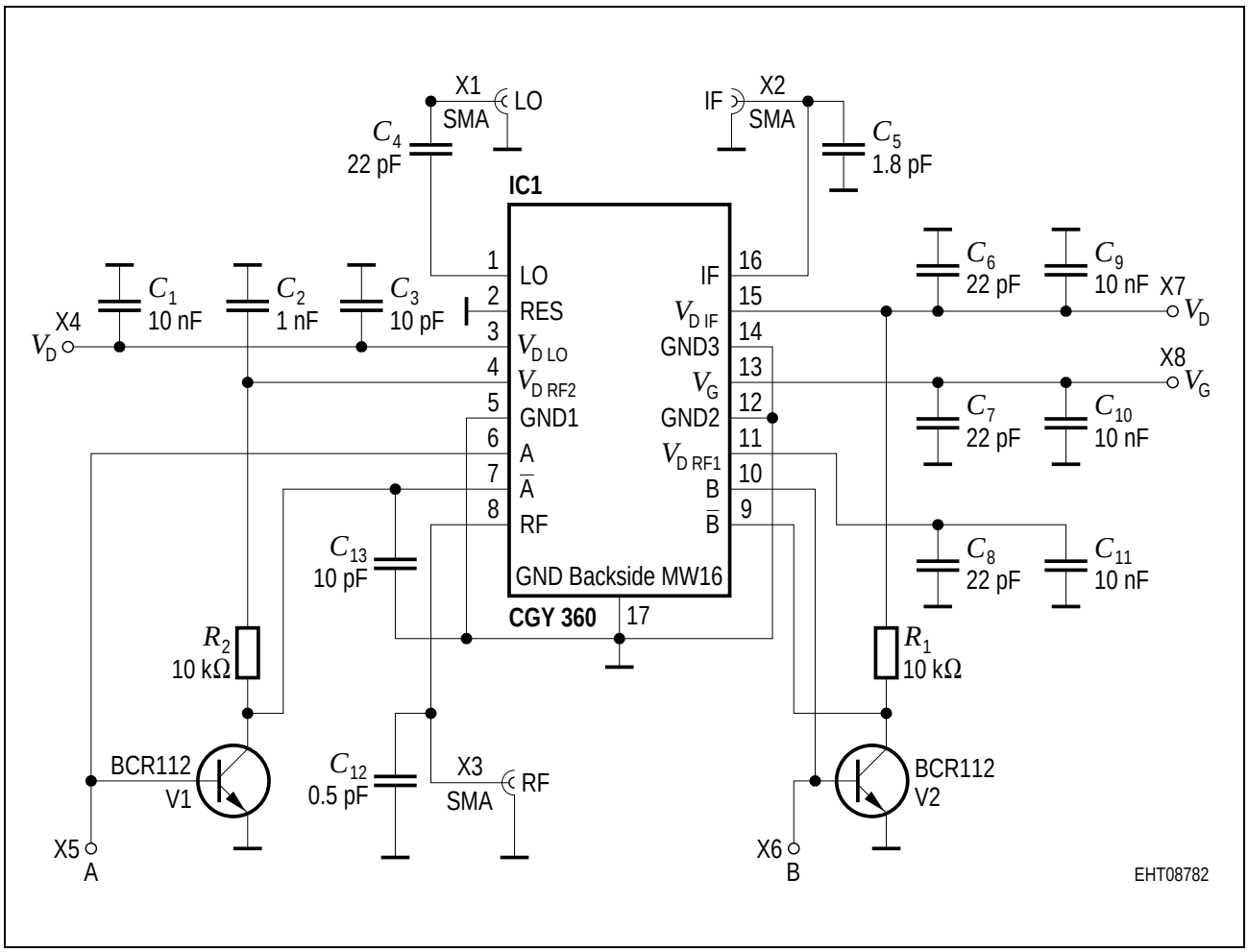


Figure 2 Application Circuit

Notes

Package of capacitor C_{12}: 0402.

Package of all other capacitors and of all resistors: 0603.

The attenuators A and B are “OUT” without supplying the ports A and B (for further information about the attenuators see “Attenuator State” on **Page 5**).

Pin Definitions and Functions

Pin No.	Symbol	Function	Bias Voltage
1	LO	LO Input	–
2	Res	Reserved	Leave open
3	VDLO	Mixer Drain Bias	+ 5 V
4	VDRF2	2nd RF Amp Drain Bias	+ 5 V
5	GND1	GND	0 V
6	A	1st Attenuator Control	+ 5 V, 0 V
7	A bar	1st Attenuator Control bar	0 V, + 5 V
8	RF	RF Input	–
9	B bar	2nd Attenuator Control bar	+ 5 V, 0 V
10	B	2nd Attenuator Control	0 V, + 5 V
11	VDRF1	1st RF Amp Drain Bias	+ 5 V
12	GND2	GND	0 V
13	VG	Amplifier Gate Bias	– 5 V
14	GND3	GND	0 V
15	VDIF	IF Amp Drain Bias	+ 5 V
16	IF	IF Output	–
MW-16 Heatsink Slug	GND	OWP Ground	0 V

Attenuator State

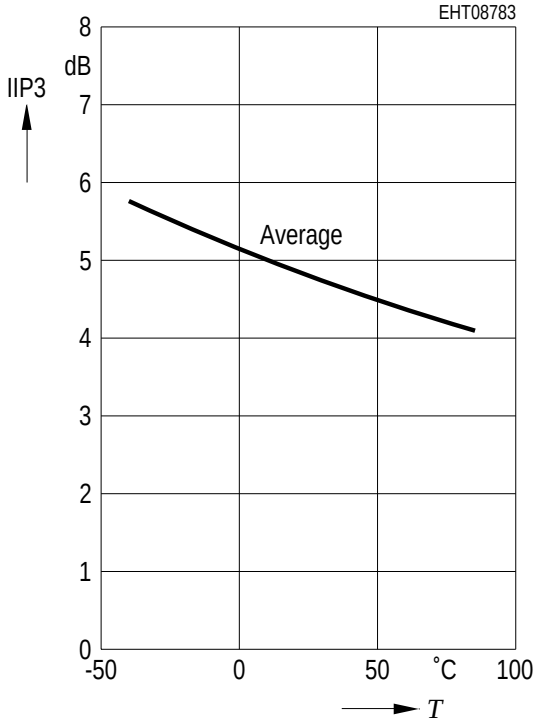
Attenuator A	“IN”	Pin 6 = High, Pin 7 = Low
	“OUT”	Pin 6 = Low, Pin 7 = High
Attenuator B	“IN”	Pin 9 = Low, Pin 10 = High
	“OUT”	Pin 9 = High, Pin 10 = Low
Logic level High	–	$V_{High} > V_D$ – 0.15 V
Logic level Low	–	$V_{Low} <$ + 0.5 V

Note
Attenuator “OUT” is defined as maximum gain state.
Attenuator “IN” is defined as minimum gain state.

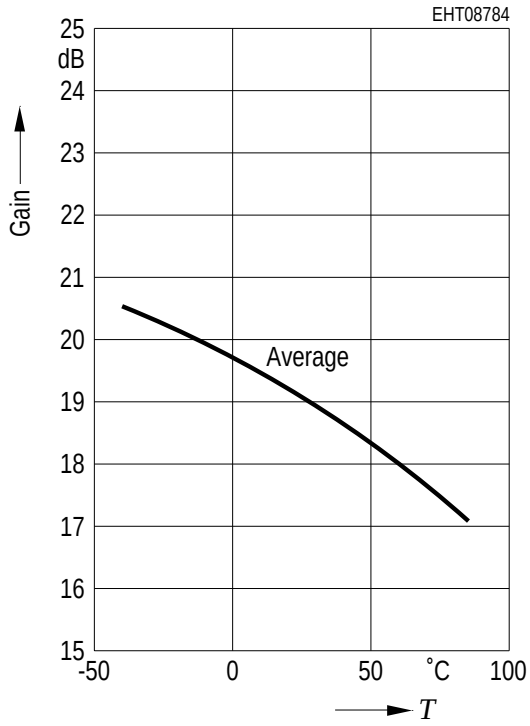
Electrical Characteristics versus Temperature

V_{DD} = 5 V, V_{GG} = – 5 V; f_{RF} = 3475 - 3500 MHz; P_{RF} = – 20 dBm; f_{LO} = 2359 MHz; P_{LO} = 0 dBm; f_{IF} = 1116 - 1141 MHz, both attenuators “OUT” (for further information about the attenuators see “Attenuator State” on **Page 5**).

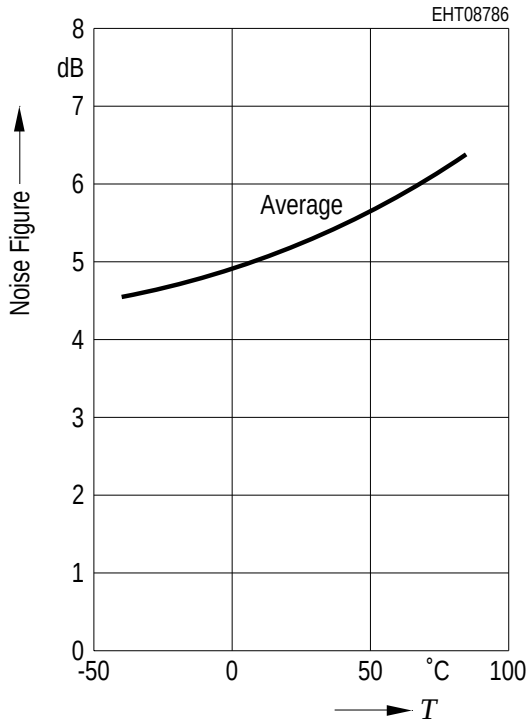
RXIC *IP3*



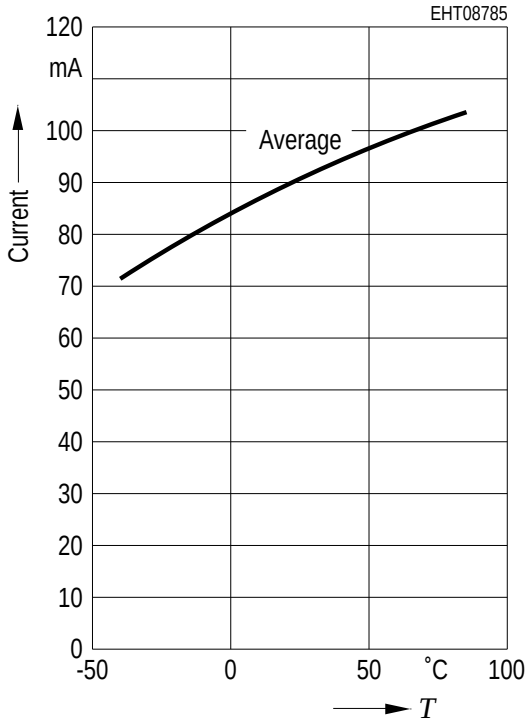
RXIC Max. Gain



RXIC Noise Figure

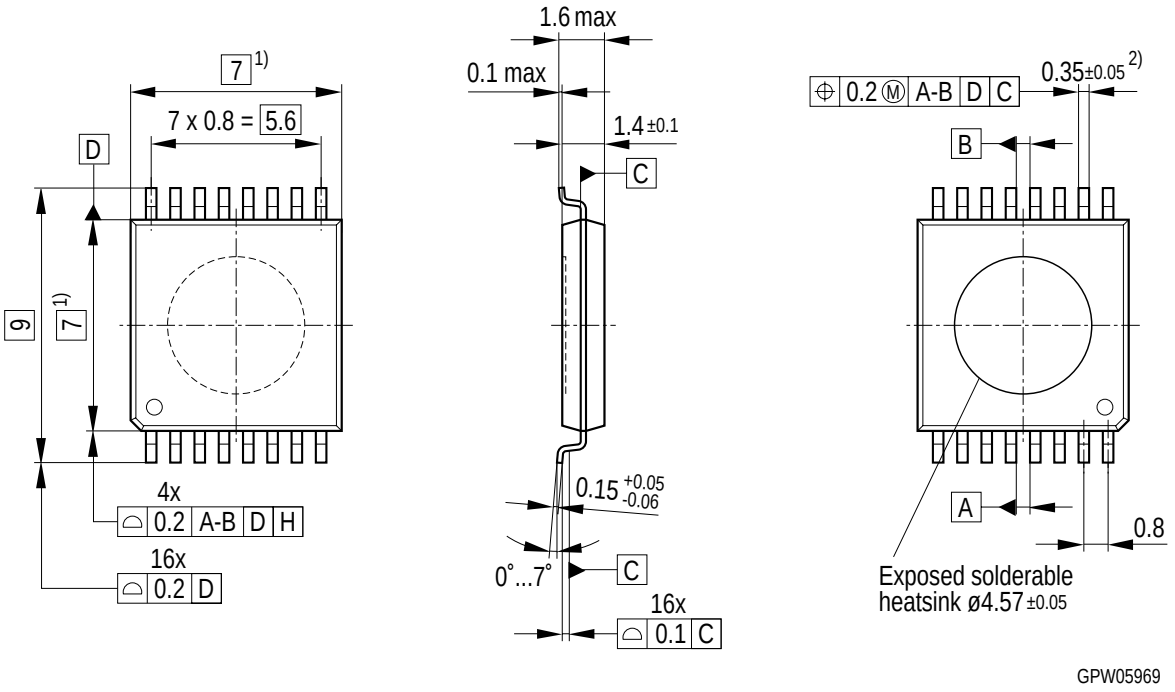


RXIC DC Current Consumption



Package Outlines

MW-16
(Special Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm