

### General Description

The AON7423 combines advanced trench MOSFET technology with a low resistance package to provide extremely low  $R_{DS(ON)}$ . This device is ideal for load switch and battery protection applications.

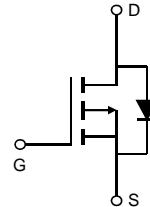
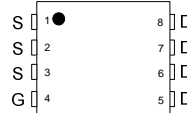
### Product Summary

$V_{DS}$	-20V
$I_D$ (at $V_{GS}=-4.5V$ )	-50A
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$ )	< 5m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=-2.5V$ )	< 6.5m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=-1.8V$ )	< 8.5m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=-1.5V$ )	< 11m $\Omega$

100% UIS Tested  
100%  $R_g$  Tested



Top View



#### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ C$	-50
		$T_C=100^\circ C$	-39
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	-200	A
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ C$	-28
		$T_A=70^\circ C$	-22.5
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	60	A
Avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AS}, E_{AR}$	180	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ C$	83
		$T_C=100^\circ C$	33
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ C$	6.2
		$T_A=70^\circ C$	4
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ C$

Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$t \leq 10s$	$R_{\theta JA}$	16	20	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>	Steady-State		45	55	$^\circ C/W$
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	1.1	1.5	$^\circ C/W$

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-20			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±8V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.2	-0.5	-0.9	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-5V	-200			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-20A T <sub>J</sub> =125°C		3.95	5	mΩ
				5.7	7.2	
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-20A		4.9	6.5	mΩ
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-20A		6.1	8.5	mΩ
		V <sub>GS</sub> =-1.5V, I <sub>D</sub> =-20A		7.7	11	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-20A		110		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.5	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				-50	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-10V, f=1MHz		5626		pF
C <sub>oss</sub>	Output Capacitance			928		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			716		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		3	6	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-10V, I <sub>D</sub> =-20A		70	100	nC
Q <sub>gs</sub>	Gate Source Charge			9.2		nC
Q <sub>gd</sub>	Gate Drain Charge			18.4		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-10V, R <sub>L</sub> =0.5Ω, R <sub>GEN</sub> =3Ω		18		ns
t <sub>r</sub>	Turn-On Rise Time			52		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			285		ns
t <sub>f</sub>	Turn-Off Fall Time			123		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-20A, di/dt=500A/μs		78		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-20A, di/dt=500A/μs		495		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> t ≤ 10s value and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

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### TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

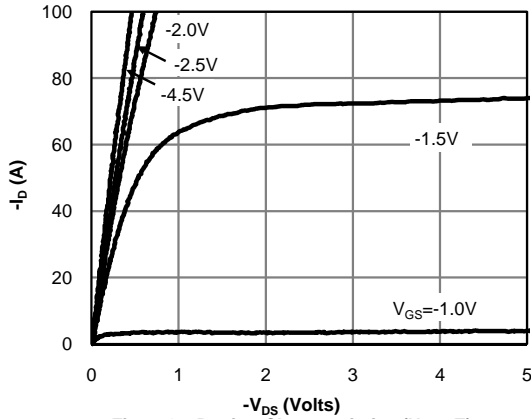


Fig 1: On-Region Characteristics (Note E)

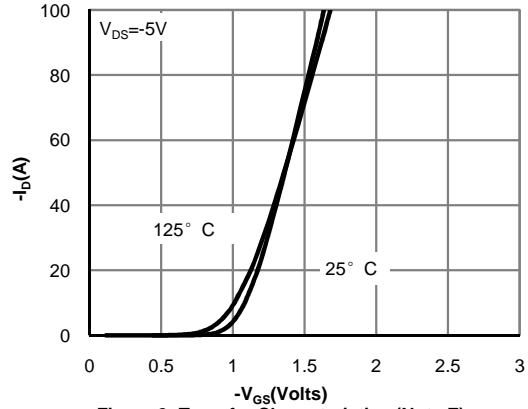


Figure 2: Transfer Characteristics (Note E)

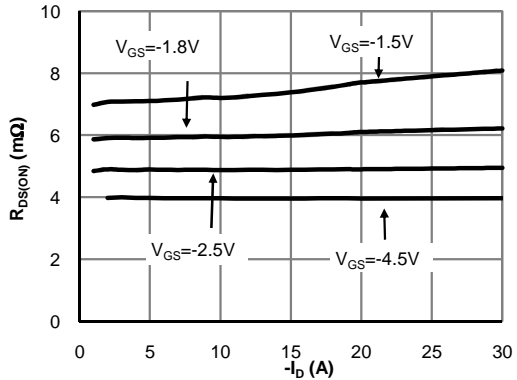


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

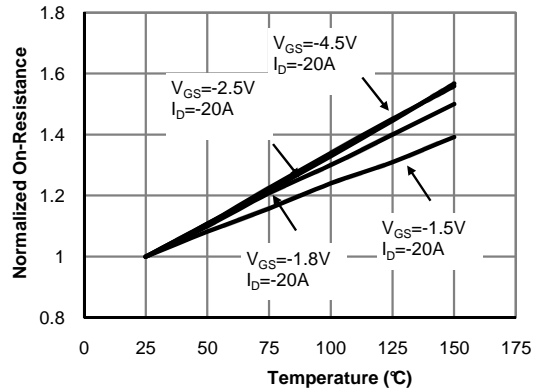


Figure 4: On-Resistance vs. Junction Temperature (Note E)

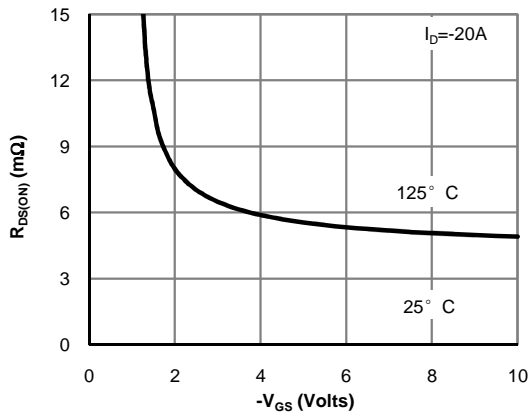


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

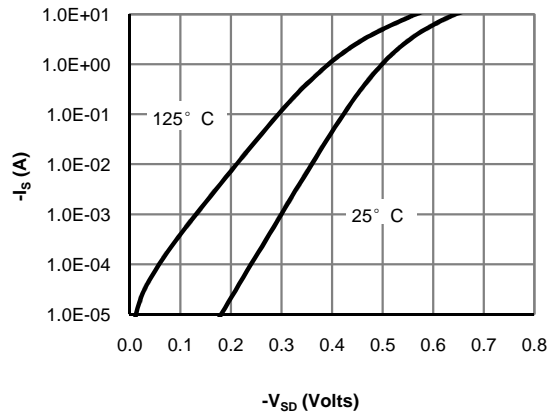


Figure 6: Body-Diode Characteristics (Note E)

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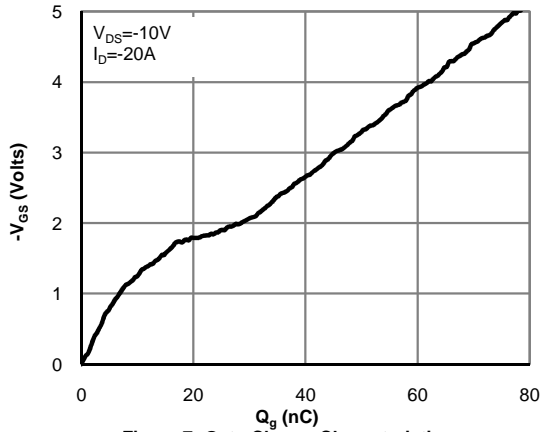


Figure 7: Gate-Charge Characteristics

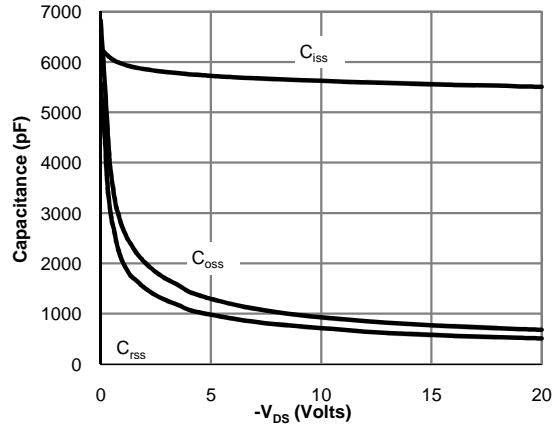


Figure 8: Capacitance Characteristics

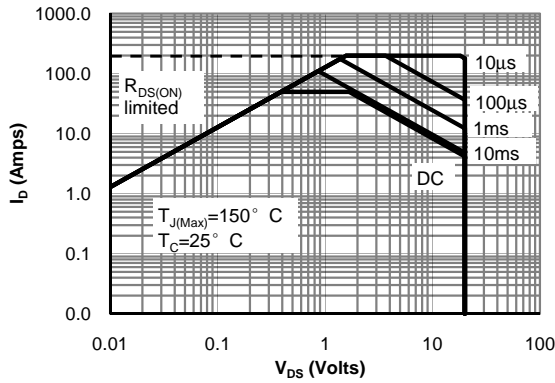


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

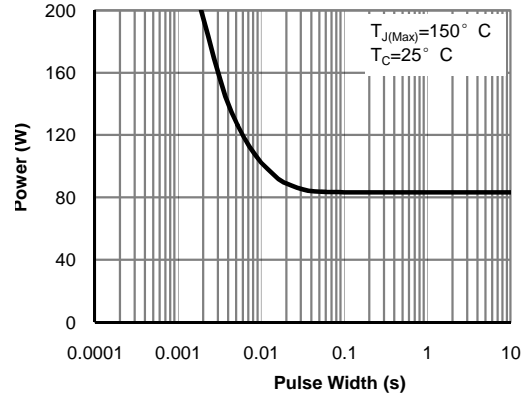


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

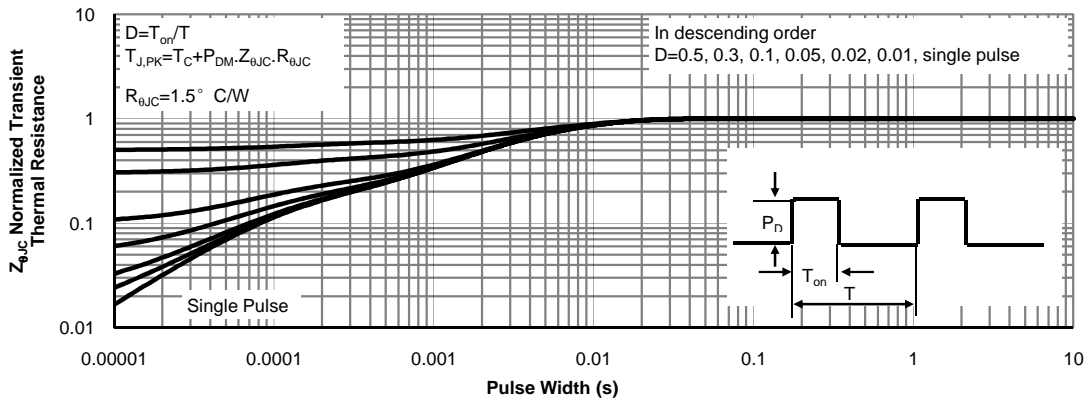


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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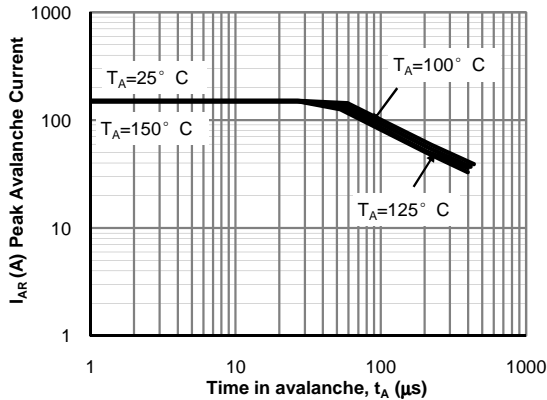


Figure 12: Single Pulse Avalanche capability (Note C)

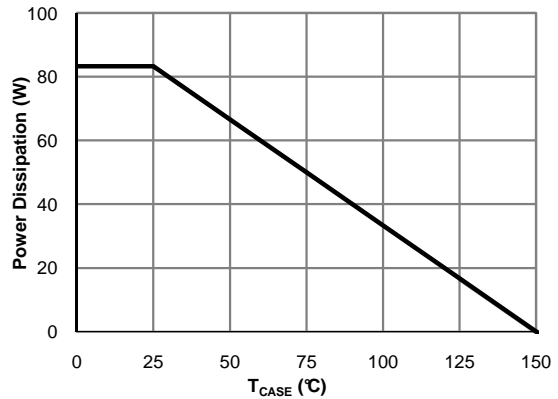


Figure 13: Power De-rating (Note F)

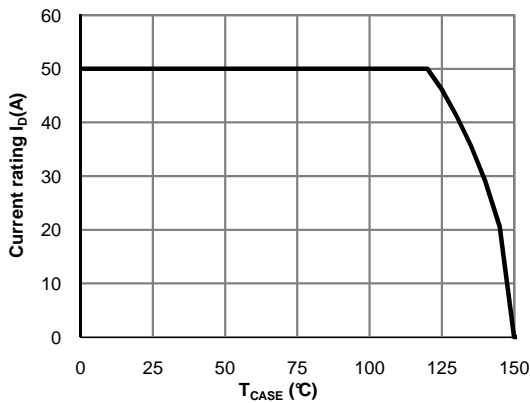


Figure 14: Current De-rating (Note F)

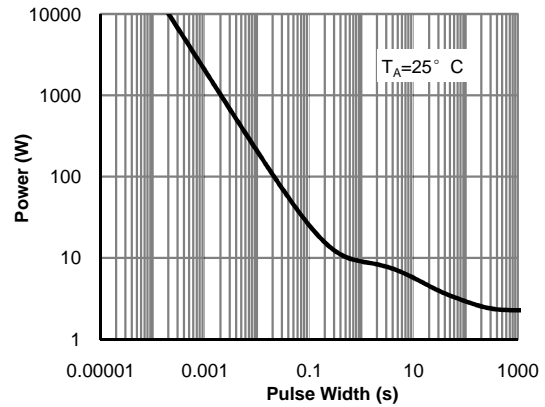


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

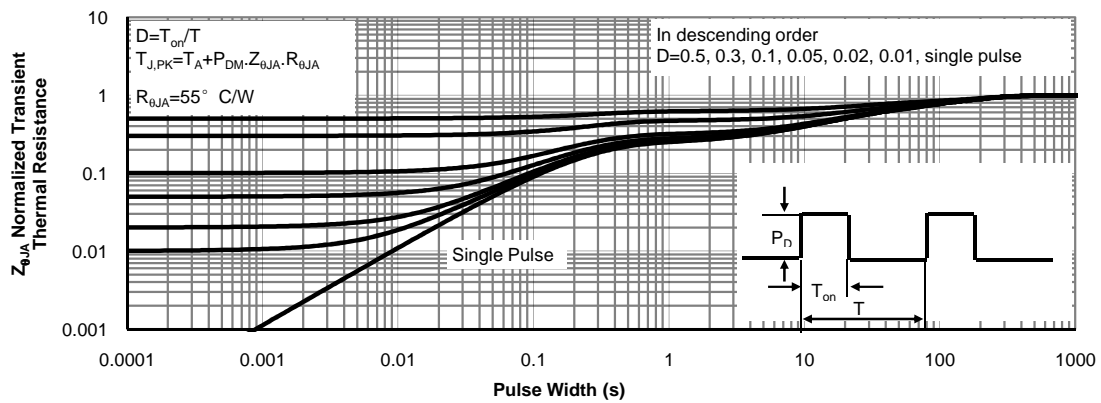
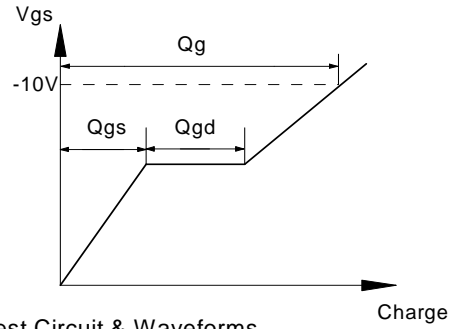
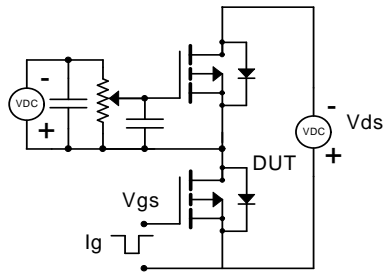
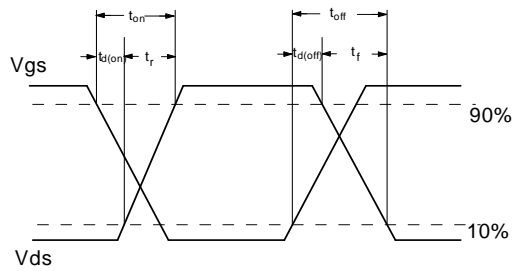
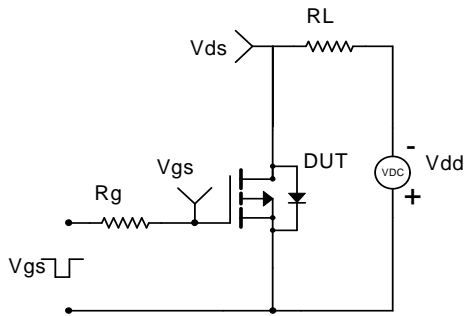


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

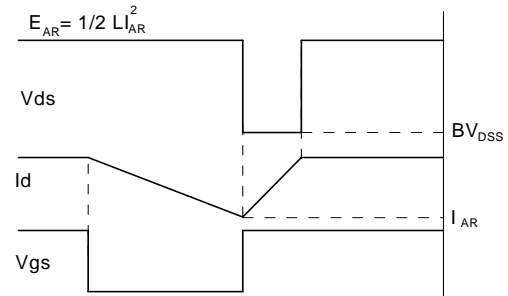
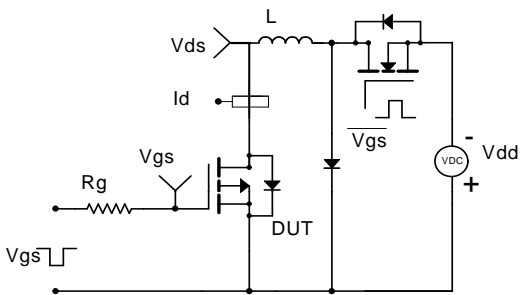
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



### Diode Recovery Test Circuit & Waveforms

