

MC100E310

5V ECL Low Voltage 2:8 Differential Fanout Buffer

The MC100E310 is a low voltage, low skew 2:8 differential ECL fanout buffer designed with clock distribution in mind. The device features fully differential clock paths to minimize both device and system skew. The E310 offers two selectable clock inputs to allow for redundant or test clocks to be incorporated into the system clock trees.

The lowest tpd delay time results from terminating only one output pair, and the greatest tpd delay time results from terminating all the output pairs. This shift is about 10–20 pS in tpd. The skew between any two output pairs within a device is typically about 25 nS. If other output pairs are not terminated, the lowest tpd delay time results from both output pairs and the skew is typically 25 nS. When all outputs are terminated, the greatest tpd (delay time) occurs and all outputs display about the same 10–20 pS increase in tpd, so the relative skew between any two output pairs remains about 25 nS.

For more information on using PECL, designers should refer to ON Semiconductor Application Note AN1406/D.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

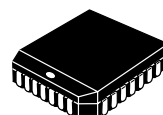
- Dual Differential Fanout Buffers
- 200 ps Part-to-Part Skew
- 50 ps Output-to-Output Skew
- 28-lead PLCC Packaging
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: V_{CC} = 4.2 V to 5.7 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -4.2 V to -5.7 V
- Internal Input Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- ESD Protection: >2KV HBM, >200V MM
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
- For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 212 devices



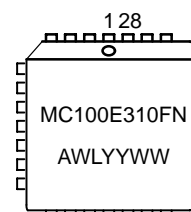
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MARKING DIAGRAMS



PLCC-28
FN SUFFIX
CASE 776



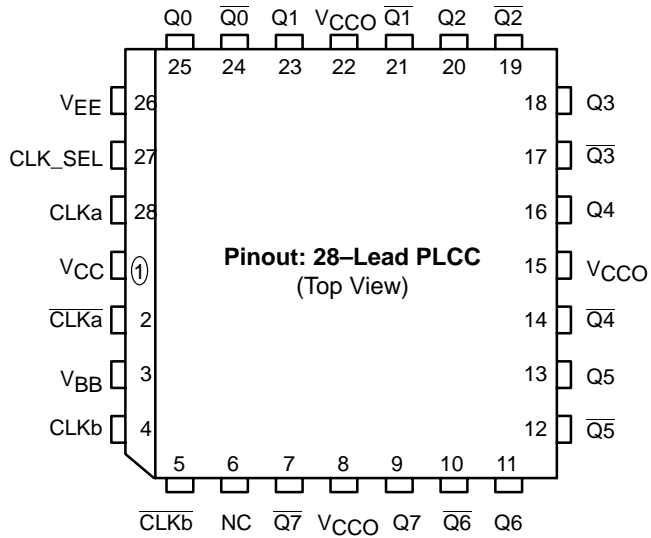
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC100E310FN	PLCC-28	37 Units/Rail
MC100E310FNR2	PLCC-28	500 Units/Reel

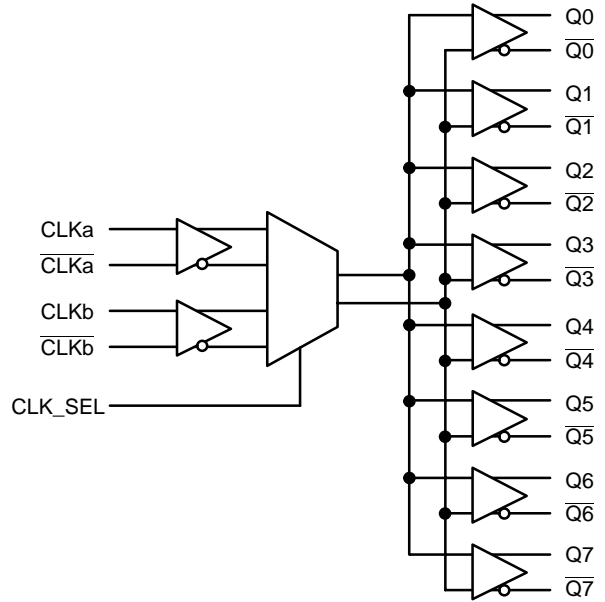
MC100E310

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



* All VCC and VCCO pins are tied together on the die.
 Warning: All VCC, VCCO, and VEE pins must be externally connected to Power Supply to guarantee proper operation.

LOGIC SYMBOL



PIN DESCRIPTION

PIN	FUNCTION
CLKa, CLKb; $\overline{\text{CLKa}}, \overline{\text{CLKb}}$	ECL Differential Input Pairs
Q0:7; $\overline{\text{Q0}}:\overline{7}$	ECL Differential Outputs
CLK_SEL	ECL Input Clock Select
VBB	Reference Voltage Output
VCC, VCCO	Positive Supply
VEE	Negative Supply
NC	No Connect

FUNCTION TABLE

CLK_SEL	Input Clock
0	CLKa Selected
1	CLKb Selected

MC100E310

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		8	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-8	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	6 -6	V V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			0 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	28 PLCC 28 PLCC	63.5 43.5	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction to Case)	std bd	28 PLCC	22 to 26	°C/W
V _{EE}	PECL Operating Range NECL Operating Range			4.2 to 5.7 -5.7 to -4.2	V V
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

100E SERIES PECL DC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V (Note 1)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		55	60		55	60		65	70	mA
V _{OH}	Output HIGH Voltage (Note 2)	3915	3995	4120	3975	4050	4120	3975	4050	4120	mV
V _{OL}	Output LOW Voltage (Note 2)	3170	3305	3445	3190	3255	3380	3190	3260	3380	mV
V _{IH}	Input HIGH Voltage (Single Ended)	3835	4050	4120	3835	4120	4120	3835	4120	4120	mV
V _{IL}	Input LOW Voltage (Single Ended)	3190	3300	3525	3190	3525	3525	3190	3525	3525	mV
V _{BB}	Output Voltage Reference	3.62		3.74	3.62		3.74	3.62		3.74	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	2.7		4.6	2.7		4.6	2.7		4.6	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / -0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}-2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

100E SERIES NECL DC CHARACTERISTICS V_{CCx} = 0.0 V; V_{EE} = -5.0 V (Note 1)

Symbol	Characteristic	0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		55	60		55	60		65	70	mA
V _{OH}	Output HIGH Voltage (Note 2)	-1085	-1005	-880	-1025	-950	-880	-1025	-950	-880	mV
V _{OL}	Output LOW Voltage (Note 2)	-1830	-1695	-1555	-1810	-1745	-1620	-1810	-1740	-1620	mV
V _{IH}	Input HIGH Voltage (Single Ended)	-1165	-950	-880	-1165	-880	-880	-1165	-880	-880	mV
V _{IL}	Input LOW Voltage (Single Ended)	-1810	-1700	-1475	-1810	-1475	-1475	-1810	-1475	-1475	mV
V _{BB}	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 3)	-2.3		-0.4	-2.3		-0.4	-2.3		-0.4	V
I _{IH}	Input HIGH Current			150			150			150	μA
I _{IL}	Input LOW Current	0.5	0.3		0.5	0.25		0.5	0.2		μA

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.46 V / -0.8 V.
2. Outputs are terminated through a 50 ohm resistor to V_{CC}-2 volts.
3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

MC100E310

MC100E310 ECL DC CHARACTERISTICS

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage	-1.085	-1.005	-0.880	-1.025	-0.955	-0.880	-1.025	-0.955	-0.880	-1.025	-0.955	-0.880	V
V _{OL}	Output LOW Voltage	-1.830	-1.695	-1.555	-1.810	-1.705	-1.620	-1.810	-1.705	-1.620	-1.810	-1.705	-1.620	V
V _{IH}	Input HIGH Voltage	-1.165		-0.880	-1.165		-0.880	-1.165		-0.880	-1.165		-0.880	V
V _{IL}	Input LOW Voltage	-1.810		-1.475	-1.810		-1.475	-1.810		-1.475	-1.810		-1.475	V
V _{BB}	Output Reference Voltage	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
V _{EE}	Power Supply Voltage	-5.25		-4.2	-5.25		-4.2	-5.25		-4.2	-5.25		-4.2	V
I _{IH}	Input HIGH Current			150			150			150			150	μA
I _{EE}	Power Supply Current		55	60		55	60		55	60		65	70	mA

MC100E310 PECL DC CHARACTERISTICS

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage (Note 1.)	3.915	3.995	4.12	3.975	4.045	4.12	3.975	4.045	4.12	3.975	4.045	4.12	V
V _{OL}	Output LOW Voltage (Note 1.)	3.170	3.305	3.445	3.19	3.295	3.38	3.19	3.295	3.38	3.19	3.295	3.38	V
V _{IH}	Input HIGH Voltage (Note 1.)	3.835		4.12	3.835		4.12	3.835		4.12	3.835		4.12	V
V _{IL}	Input LOW Voltage (Note 1.)	3.190		3.525	3.190		3.525	3.190		3.525	3.190		3.525	V
V _{BB}	Output Reference Voltage (Note 1.)	3.62		3.74	3.62		3.74	3.62		3.74	3.62		3.74	V
V _{CC}	Power Supply Voltage	4.75		5.25	4.75		5.25	4.75		5.25	4.75		5.25	V
I _{IH}	Input HIGH Current			150			150			150			150	μA
I _{EE}	Power Supply Current		55	60		55	60		55	60		65	70	mA

1. These values are for V_{CC} = 5.0 V. Level Specifications will vary 1:1 with V_{CC}.

AC CHARACTERISTICS V_{CCx} = 5.0 V; V_{EE} = 0.0 V or V_{CCx} = 0.0 V; V_{EE} = -5.0 V (Note 1)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{MAX}	Maximum Toggle Frequency		TBD			TBD			TBD		GHz
t _{PLH} t _{PHL}	Propagation Delay to Output IN (differential) (Note 2.) IN (single-ended) (Note 3.)	525 500		725 750	550 550		750 800	575 600		775 850	ps
t _{skew}	Within-Device Skew (Note 4.) Part-to-Part Skew (Diff)			75 250			50 200			50 200	ps
t _{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
V _{PP}	Minimum Input Swing (Note 5.)	500			500			500			mV
t _r /t _f	Output Rise/Fall Time (20%–80%)	200		600	200		600	200		600	ps

- V_{EE} can vary +0.46 V / -0.8 V.
- The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the ON Semiconductor High Performance ECL Data Book (DL140/D).
- The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the ON Semiconductor High Performance ECL Data Book (DL140/D).
- The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
- V_{PP(min)} is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP(min)} is AC limited for the E310 as a differential input as low as 50 mV will still produce full ECL levels at the output.

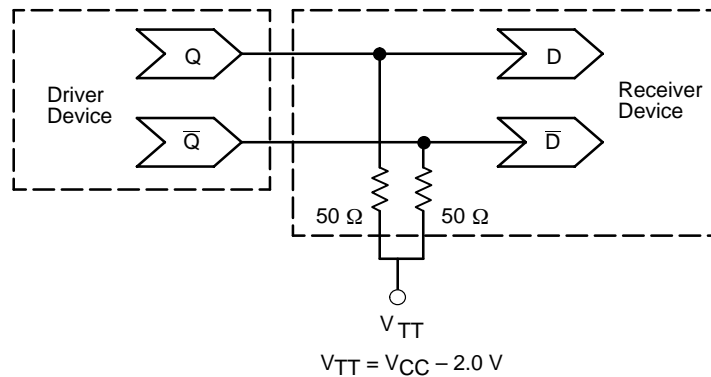


Figure 1. Typical Termination for Output Driver and Device Evaluation
 (See Application Note AND8020 – Termination of ECL Logic Devices.)

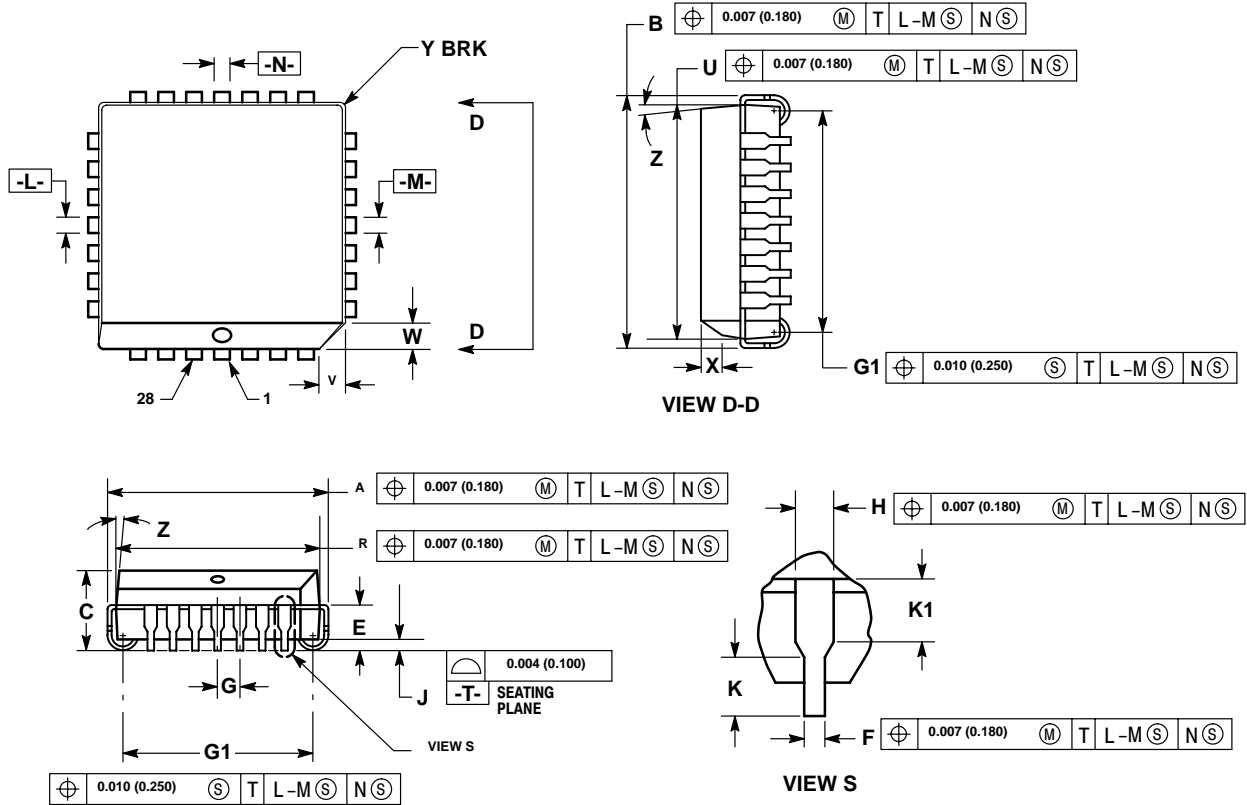
Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

MC100E310

PACKAGE DIMENSIONS

PLCC-28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE E



NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

Notes

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