Ordering number : E*NA0633

Preliminary

SANYO Semiconductors

DATA SHEET

Bi-CMOS LSI

LV25400W — DSP Tuner Front End for Automotive Applications

Overview

The LV25400W is a tuner front end IC that supports the Sanyo SDRS400 car radio DSP.
The LV25400W supports worldwide radio standards including the FM bands used in US, Europe, and Japan as well as the LW, MW, SW, and FM weather bands. It adopts an image canceling mixer for the FM mixer and incorporates a fast PLL locking function to support RDS. The LV25400W also supports automatic alignment using CCB bus control. It requires external EEPROM.
The LV25400W can implement a DSP tuner at low cost with a minimal number of external components.

Functions

- AM, FM, FE, IF, and PLL circuits

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} 8V	OSC_V_{CC} (2), FE_V_{CC} (58)	9.0	V
	V_{CC} 5V	XTAL_V_{CC} (13), V_{CC}D (22), V_{CC}A (40)	6.0	V
CCB bus maximum input voltage	V_{IN} max	Pin 18, 19, 20	-0.3 to +5.0	V
CCB bus maximum output voltage	V_O	Pin 21	-0.3 to +6.5	V
Allowable power dissipation	Pd max	Ta ≤ 85°C *1	840	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-50 to +125	°C

*1 : Ratings vary with characteristics of the circuit board (materials, size, etc.) on which the device is to be mounted.

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Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC} 8V	OSC_V_{CC} (2), FE_V_{CC} (58)	8.0	V
	V_{CC} 5V	XTAL_V_{CC} (13), V_{CC}D (22), V_{CC}A (40)	5	V
Operating supply voltage range	V_{CC} 8Vop		7.5 to 8.5	V
	V_{CC} 5Vop		4.5 to 5.5	V
CCB bus high-level input voltage	V_{IH}	CE, DI, CL	2.5 to 5.0	V
CCB bus low-level input voltage	V_{IL}	CE, DI, CL	0 to 0.8	V
CCB bus high-level input current	I_{IH}	CE, DI, CL ; VI5.5V	10 or less	μA
CCB bus low-level input current	I_{IL}	CE, DI, CL ; VI0V	10 or less	μA
DO low-level output voltage	V_{OL}		0.38 or less	V
DO high-level output voltage	V_{OH}	Connected to an LC75040.	2.1 or more	V

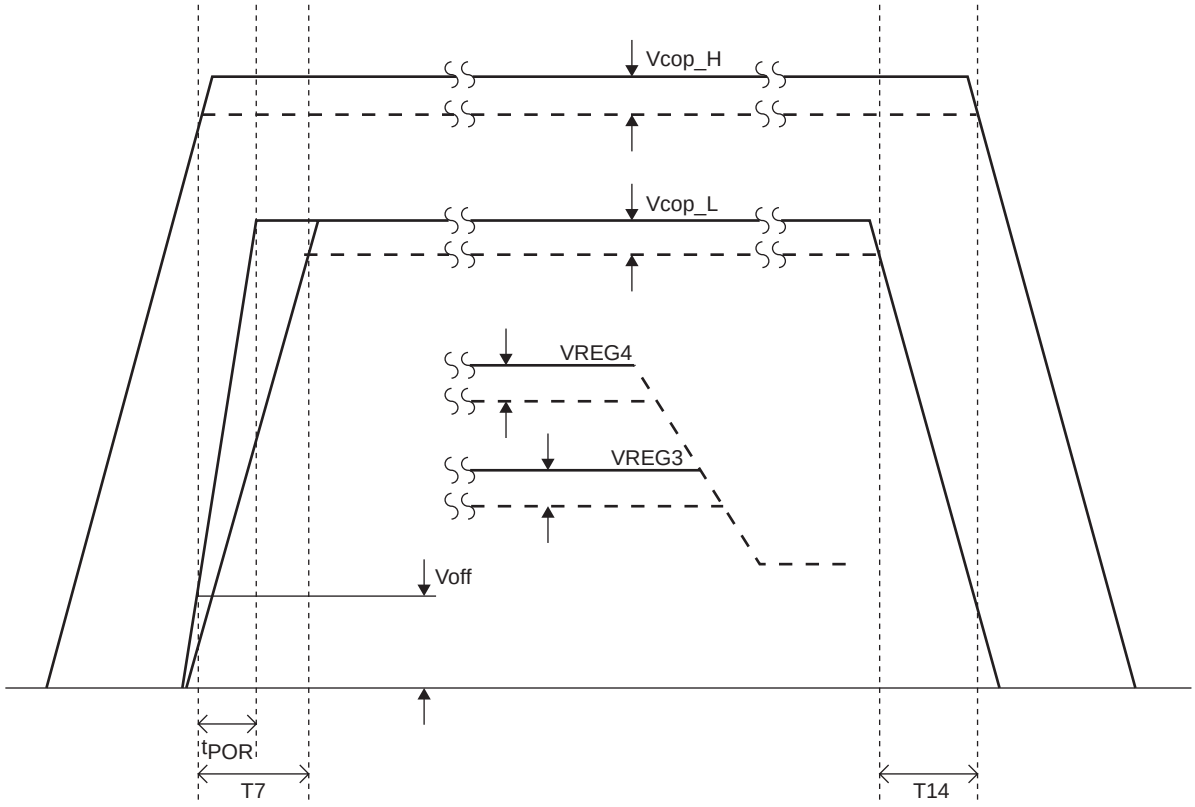
Reception Frequencies

Parameter	Symbol	Conditions	Frequency ratings	Unit
FM reception frequencies	f_{FM}	JPN, US, EUR	76 to 108.1	MHz
FM weather band reception frequencies	f_{FM-WB}		162.4 to 162.55	MHz
AM reception frequencies	f_{AMLW}	LW	144 to 288	kHz
	fAMMW	MW	520 to 1710	kHz
	fAMSW	SW	2.94 to 22.0	MHz

Power on/Power off Timing and the Power on Reset

Recommended Operating Ratings at Ta = 25°C, GND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage	Vcop H	Pin 2, 54, 55, 58	7.5		8.5	V
	Vcop L	Pin 13, 22, 40	4.5		5.5	V
Internal logic voltage	VREG3	Pin 23	2.7		3.3	V
	VREG4	Pin 24	3.7		4.3	V
Power application time (8.0 V → 5.0 V)	T7		10		100	msec
Internal register retention voltage	Vhmin3	Pin 23 : Design reference value	2.2			V
	Vhmin4	Pin 24 : Design reference value	2.2			V
Internal register reset voltage	Voff	Pin 13, 22, 40 : Design reference value	0		0.2	V
Internal register reset power supply rise time	tPOR	Pin 13, 22, 40 : Design reference value	0.05		3	msec
Power application time (5.0 V → 8.0 V)	T14		10		100	msec



AC Characteristics

Operating Characteristics at Ta = 25°C, V_{CC} = 8.0V, V_{DD} = 5.0V, unless otherwise specified. Ratings for publications

* : These measurements are made using the Yamaichi Electronics IC51-0644-807 IC socket. An IHF bandpass filter is used as the audio filter.

FM Characteristics - FM Front End Mixer Input (No dummy)

Parameter	Symbol	Conditions	Applied voltage				CCB Command				min	typ	max	unit
			Pin 25/26	Pin 32	Pin 50	Pin 64	IN1	IN2	IN3-1	IN3-2				
DC Characteristics														
Current drain-8V FM	I_{CCO}-8V FM	No input, FM mode I2+I54+I55+I58	3				15	13	25	25	38	48	56	mA
Current drain-5V FM	I_{CCO}-5V FM	No input, FM mode I13+I22+I40	3				15	13	25	25	31	40	46	mA
Current drain-8V FM	I_{CCO}-8V FM2	No input, FM mode, IFAGC-Wide = OFF I2+I54+I55+I58	3				15	13	27	25	36	46	51	mA
Current drain-5V FM	I_{CCO}-5V FM2	No input, FM mode I13+I22+I40	3				15	13	27	25	23	32	37	mA
Regulator bias 3V	VREG3V	The pin 23 voltage	3				15	13	25	25	2.7	3	3.3	V
Regulator bias 4V	VREG4V	The pin 24 voltage	3				15	13	25	25	3.6	4	4.4	V
FM antenna dump output current	IANTD-F	With 6.0V applied to pin 64 The pin 63 output current	0	0		6	15	13	25	25	5	8	12	mA
Crystal oscillator frequency	FXTAL	D2-5, 6, 7 = [110]	3				62	48	25	25		4.5		MHz
Crystal oscillator level	VXTAL	D2-5, 6, 7 = [110] (reference value)	3				62	48	25	25	15		30	mVrms
Crystal oscillator buffer level	VXTAL OSC OUT2	D2-5, 6, 7 = [110]	3				62	48	25	25	115	165		mVrms
S-meter DC output * : Adjust the shifter bits with a 50dBμV input.	VSMFM-1	10dBμV, the pin 38 DC output, no modulation	3				62	50	38	25B	0.65	0.95	1.25	V
	VSMFM-2	30dBμV, the pin 38 DC output, no modulation	3				62	50	38	25B	0.95	1.25	1.55	V
	VSMFM-3	50dBμV, the pin 38 DC output, no modulation	3				62	50	38	25B	2.10	2.15	2.20	V
	VSMFM-4	70dBμV, the pin 38 DC output, no modulation	3				62	50	38	25B	3.1	3.4	3.7	V
	VSMFM-5	90dBμV, the pin 38 DC output, no modulation	3				62	50	38	25B	3.7	4	4.3	V
Total gain from mixer to DIV IF amplifier	GMXDIV	FM_MIX_IN,DIV_OUT_IF (pin 31) Ratio of the input to output signal levels 98.1MHz mod = off, 70dBμV-Input	1.5				62	50	38	25	18.5	21.5	24.5	dB
DIV IF amplifier gain	GDIVIF	IF_N_IN1 (pin 45), DIV_OUT_IF (pin 31) Ratio of the input to output signal levels 10.7MHz mod = off, 88dBμV-Input	3				62	50	38	25	4.5	7.5	10.5	dB
1dB compression point driver IF	1DB POINT DIF	IF_N_IN1 (pin 45), DIV_OUT_IF (pin 31) Ratio of the input to output signal levels 10.7MHz mod = off	3				62	50	38	25		111		dB
Narrow IF AGC grain (FM)	GIFAGCNF1	FM_ANALOG_IN (pin 45), 10.7OUTN (pin 29) Ratio of the input to output signal levels 10.7MHz mod = off 100dBμV-Input [D32-28 to 25] = 1011, With 0V applied to pin 26	0				62	50	38	25	-3.1	-0.6	1.9	dB
Narrow IF AGC grain (FM)	GIFAGCNF2	FM_ANALOG_IN (pin 45), 10.7OUTN (pin 29) Ratio of the input to output signal levels 10.7MHz mod = off 80dBμV-Input [D32-28 to 25] = 1011, With 3V applied to pin 26	3				62	50	38	25	16.9	21.4	25.9	dB

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Parameter	Symbol	Conditions	Applied voltage				CCB Command				min	typ	max	unit
			25/26 pin	32 pin	50 pin	64 pin	IN1	IN2	IN3-1	IN3-2				
1dB complession point FM-Narrow	1DB POINT NF	FM_ANALOG_IN (pin 45), 10.7OUTN (pin 29) 10.7MHz mod = off [D32-28 to 25] = 1011, With 0V applied to pin 26	0				62	50	38	25	105			dBμV
Wide IF AGC grain (FM)	GIFAGCWF1	FM_HD_IN (pin 48), HD_OUTN (pin 27) Ratio of the input to output signal levels 10.7MHz mod = off 100dBμV-Input [D2-15 to 12] = 1011, With 0V applied to pin 25	0				62	50	38	25	-3.5	-1	1.5	dB
Wide IF AGC grain (FM)	GIFAGCWF2	FM_HD_IN (pin 48), HD_OUTN (pin 27) Ratio of the input to output signal levels 10.7MHz mod = off 80dBμV-Input [D2-15 to 12] = 1011, With 3V applied to pin 25	3				62	50	38	25	16.5	21	25.5	dB
1dB compression point FM - wide	1DB POINT WF	FM_HD_IN (pin 48), HD_OUTP (pin 27) 10.7MHz mod = off [D2-15 to 12] = 1011	0				62	50	38	25	104			dBμV
Image cancellation ratio (US)	IR US	98.1MHz reference, the amount rejected at +21.4MHz	1.5				62	50	38	25	17			dB
Image cancellation ratio (JPN)	IR JPN	83MHz reference, the amount rejected at -21.4MHz [D1-26, 27] = 01	1.5				69	50	38	25	15			dB
FM wide AGC on sensitivity F1	WAGC ON-F1	fr = 102.1MHz FM-Wide AGC-Bit [D32-3 to 0] = 0000 : minimum keyed-AGC-Bit [D32-11 to 8] = 0000 : minimum	0	0			62	50	38	13	78	85	92	dBμV
FM wide AGC on sensitivity F2	WAGC ON-F2	fr = 102.1MHz FM-Wide AGC-Bit [D32-3 to 0] = 1111 : maximum keyed-AGC-Bit [D32-11 to 8] = 0000 : minimum	0	0			62	50	38	15	92	99	106	dBμV
FM narrow AGC on sensitivity F1	NAGC ON-F1	fr = 98.1MHz FM-Narrow AGC-Bit [D32-7 to 4] = 0000 : minimum	0	3			62	50	38	16	66.5	73.5	80.5	dBμV
FM narrow AGC on sensitivity F2	NAGC ON-F2	fr = 98.1MHz FM-Narrow AGC-Bit [D32-7 to 4] = 1111 : maximum	0	3			62	50	38	18	82.5	89.5	96.5	dBμV
Practical sensitivity	S/N-31	Connected to an LA1787 (MPX, left channel output) *HCC OFF 98.1MHz, 31dBμV, fm = 1kHz, 22.5kHz-mod 61/62pin input	3				62	50	38	25	30			dB
Signal-to-noise ratio	S/N-90	Connected to an LA1787 (MPX, left channel output) 98.1MHz, 90dBμV, fm = 1kHz, 22.5kHz-mod 61/62pin input	0				62	50	38	25	54	57		dB

AM Characteristics : AM, AMANT inputs

Parameter	Symbol	Conditions	Applied voltage				CCB Command				min	typ	max	unit
			Pin 25/26	Pin 32	Pin 50	Pin 64	IN1	IN2	IN3-1	IN3-2				
DC Characteristics														
Current drain-8V AM	I_{CCO}-8V AM	No input, AM mode I2+I54+I55+I58	3				33	15	26	26	32	44	54	mA
Current drain-5V AM	I_{CCO}-5V AM	No input, AM mode I13+I22+I40	3				33	15	26	26	21	28	34	mA
AM antenna dump output current	IANTD-A	When pin 50 is connected to ground The ANT-D (pin 52) output current	3				33	15	26	26	3.5	6	9	mA
AC Characteristics														
First AM amplifier gain	GAMP1	FM_N_IN1 (pin 45) IF_OUT (pin 43), after CF matching, 10.7MHz mod = off 74dBμV = Input	0				33	44	26	26	5.2	6.2	7.2	dB
Narrow IF AGC grain (AM)	GIFAGCNA1	AM_ANALOG_IN (pin 37), 10.7OUTN (pin 29) Ratio of the input to output signal levels 10.7MHz mod = off 100dBμV-Input [D32-28 to 25] = 1011, With 0V applied to pin 26	0				33	44	26	26	-1.6	0.9	3.4	dB
Narrow IF AGC grain (AM)	GIFAGCNA2	AM_ANALOG_IN (pin 37), 10.7OUTN (pin 29) Ratio of the input to output signal levels 10.7MHz mod = off 80dBμV-Input [D32-28 to 25] = 1011, With 3V applied to pin 26	3				33	44	26	26	18	22.9	27	dB
1dB compression point AM - narrow	1DB POINT NA	AM_ANALOG_IN (pin 37), 10.7OUTN (pin29) 10.7MHz mod = off [D32-28 to 25] = 1011, With 0V applied to pin 26	0				33	44	26	26	105			dBμV
Wide IF AGC grain (AM)	GIFAGCWA1	AM_HD_IN (pin 39), HD_OUTN (pin 27) Ratio of the input to output signal levels 10.7MHz mod = off 100dBμV-Input [D2-15 to 12] = 1011, With 0V applied to pin 25	0				33	44	26	26	-2.5	0	2.5	dB
Wide IF AGC grain (AM)	GIFAGCWA2	AM_HD_IN (pin 39), HD_OUTN (pin 27) Ratio of the input to output signal levels 10.7MHz mod = off 80dBμV-Input [D2-15 to 12] = 1011, With 3V applied to pin 25	3				33	44	26	26	17.5	22	26.5	dB
1dB compression point AM - wide	1DB POINT WA	AM_HD_IN (pin 39), HD_OUTP (pin 27) 10.7MHz mod = off [D2-15 to 12] = 1011, With 0V applied to pin 25	0				33	44	26	26	104			dBμV
AM wide AGC on sensitivity A1	WAGC ON-A1	AM-ANT-IN = 1.4MHz, mod = off The input level such that the ANT_D (pin 52) level becomes 0.5V. AM wide AGC sensitivity control setting (D32-3 to D32-0) : 0000 (the minimum value)	3				33	44	26	27	78.5	83.5	88.5	dBμV
AM wide AGC on sensitivity A2	WAGC ON-A2	AM-ANT-IN = 1.4MHz, mod = off The input level such that the ANT_D (pin 52) level becomes 0.5V. AM wide AGC sensitivity control setting (D32-3 to D32-0) : 1101	3				33	44	26	29	92	97	102	dBμV

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Parameter	Symbol	Conditions	Applied voltage				CCB Command				min	typ	max	unit
			Pin 25/26	Pin 32	Pin 50	Pin 64	IN1	IN2	IN3-1	IN3-2				
AM narrow AGC on sensitivity A1	NAGC ON-A1	AM-ANT-IN = 1MHz, mod = off The input level such that the ANT_D (pin 52) level becomes 0.5V. AM narrow AGC sensitivity control setting (D32-7 to D32-4) : 0000 (the minimum value)	3				33	44	26	30	60	65	70	dBμV
AM narrow AGC on sensitivity A2	NAGC ON-A2	AM-ANT-IN = 1MHz, mod = off The input level such that the ANT_D (pin 52) level becomes 0.5V. AM narrow AGC sensitivity control setting (D32-7 to D32-4) : 1111 (the maxim value)	3				33	44	26	32	75	80	85	dBμV
Total AM gain	AMGAIN	1MHz, 60dBμV, mod = off, the ration of the AM_ANT input and the 10.7OUTN (pin 29) output levels	3				33	44	26	32	33.5	39	44.5	dB
Practical sensitivity	S/N-33	With an LA1787 connected With a 1MHz, 33dBμV, fm = 1kHz, 30% modulation ANT input and the IF AGC voltage = 3V add.	3				33	44	26	32	20			dB
THD_1	THD-74	With an LA1787 connected With a 1MHz, 74dBμV, fm = 1kHz, 80% modulation ANT input and the IF AGC voltage adjusted so that the IFAGCOUT level is 100dBμV.	Adjusted				33	44	26	32		0.7	1.2	%
THD_2	THD-77	With an LA1787 connected With a 1MHz, 77dBμV, fm = 1kHz, 80% modulation ANT input and the IF AGC voltage adjusted so that the IFAGCOUT level is 100dBμV.	Adjusted				33	44	26	32		0.7	1.2	%
Signal-to-noise ratio	S/N-74	With an LA1787 connected With a 1MHz, 74dBμV, fm = 1kHz, 80% modulation ANT input and the IF AGC voltage adjusted so that the IFAGCOUT level is 100dBμV.	Adjusted				33	44	26	32	52.5	56		dB

DC Characteristics

Operating Characteristics at Ta = 25°C, V_{CC} = 8.0V, V_{DD} = 5.0, GND = 0, V_{SS} = 0, unless otherwise specified.
Ratings for publications

* : These measurements are made using the Yamaichi Electronics IC51-0644-807 IC socket. *: Undefined

FM: No input

Pin No.	Parameter	Symbol	Conditions	CCB Command				min	typ	max	unit
				IN1	IN2	IN3-1	IN3-2				
1	FE_GND	V1FM		15	13	25	25	0			V
2	OSC_V_{CC}	V2FM		15	13	25	25			8	V
3	OSC_B	V3FM		15	13	25	25		2.65		V
4	OSC_C	V4FM		15	13	25	25		7.45		V
5	VT	V5FM		15	13	25	25	0		8	V
6	FET_GND	V6FM		15	13	25	25	0			V
7	PLL-LPF	V7FM		15	13	25	25		*		V
8	FM FET	V8FM		15	13	25	25		*		V
9	AM FET	V9FM		15	13	25	25		*		V
10	CPAM	V10FM		15	13	25	25		*		V
11	CPFM	V11FM		15	13	25	25		*		V
12	GND (Digital)	V12FM		15	13	25	25	0			V
13	V_{CC} (X'TAL)	V13FM		15	13	25	25			5	V
14	X'tal IN	V14FM		15	13	25	25		2.7		V
15	X'tal OUT	V15FM		15	13	25	25		4.1		V
16	GND (X'TAL)	V16FM		15	13	25	25	0			V
17	X'tal-Buffer-OUT	V17FM		15	13	25	25		3.45		V
18	CE	V18FM		15	13	25	25		BUS		V
19	DI	V19FM		15	13	25	25		BUS		V
20	CL	V20FM		15	13	25	25		BUS		V
21	DO	V21FM		15	13	25	25	0		Note 1	V
22	V_{CC} 5V (Digital)	V22FM		15	13	25	25			5	V
23	PLL V_{DD} (3V REG)	V23FM		15	13	25	25		3.1		V
24	PLL V_{DD} (4V REG)	V24FM		15	13	25	25		4.15		V
25	AGC-Control-IN (HD)	V25FM		15	13	25	25		Input		V
26	AGC-Control-IN (Analog)	V26FM		15	13	25	25		Input		V
27	IFAGC-OUTN (HD)	V27FM		15	13	25	25		2.75		V
28	IFAGC-OUTP (HD)	V28FM		15	13	25	25		2.75		V
29	IFAGC-OUTN (Analog)	V29FM		15	13	25	25		2.75		V
30	IFAGC-OUTP (Analog)	V30FM		15	13	25	25		2.75		V
31	DIV-IF-OUT	V31FM		15	13	25	25		1.95		V
32	VSM-DC	V32FM		15	13	25	25	0		5	V
33	2.7V REG	V33FM		15	13	25	25		2.7		V
34	IFAGC-IN (Analog-Bypass)	V34FM		15	13	25	25		2.45		V
35	IFAGC-IN (HD-Bypass)	V35FM		15	13	25	25		2.45		V
36	GND (Analog)	V36FM		15	13	25	25		0		V
37	IFAGC-IN (Analog)	V37FM		15	13	25	25		2.45		V
38	VSM-AC	V38FM		15	13	25	25	0		5	V
39	IFAGC-IN (HD)	V39FM		15	13	25	25		2.45		V
40	V_{CC} 5V (Analog)	V40FM		15	13	25	25		5		V
41	AM-Narrow-AGC-IN	V41FM		15	13	25	25		*		V
42	Address SW/DAC-Monitor	V42FM		15	13	25	25		3.1		V
43	AM-1st-IF-OUT	V43FM		15	13	25	25		7.5		V
44	4.9V REG	V44FM		15	13	25	25		4.7		V
45	IF-Narrow-IN	V45FM		15	13	25	25		2.6		V
46	IF-Narrow-IN(Bypass)	V46FM		15	13	25	25		2.6		V
47	AM-Wide-AGC (Bypass)	V47FM		15	13	25	25			1.5	V

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Pin No.	Parameter	Symbol	Conditions	CCB Command				min	typ	max	unit
				IN1	IN2	IN3-1	IN3-2				
48	IF-Wide-IN	V48FM		15	13	25	25		2.05		V
49	IF-Wide-IN (Bypass)	V49FM		15	13	25	25		2.05		V
50	AM-RF-AGC	V50FM		15	13	25	25			1	V
51	AM-RF-AGC (Bypass)	V51FM		15	13	25	25			1	V
52	AM-ANT-D	V52FM		15	13	25	25	0		0.3	V
53	FM-Narrow-AGC-IN	V53FM		15	13	25	25			0.3	V
54	FM/AM-MIX-OUT	V54FM		15	13	25	25			8	V
55	FM/AM-MIX-OUT	V55FM		15	13	25	25			8	V
56	ANT-DAC	V56FM		15	13	25	25	0		8	V
57	RF-DAC	V57FM		15	13	25	25	0		8	V
58	V_{CC} (8V)	V58FM		15	13	25	25			8	V
59	AM-MIX-IN	V59FM		15	13	25	25			0.2	V
60	AM-MIX-IN	V60FM		15	13	25	25			0.2	V
61	FM-MIX-IN	V61FM		15	13	25	25		3		V
62	FM-MIX-IN	V62FM		15	13	25	25		3		V
63	FM-RF-AGC	V63FM		15	13	25	25		0.2		V
64	FM-ANT-D	V64FM		15	13	25	25		8		V

Note 1 : Pull-up voltage

AM: No input

Pin No.	Parameter	Symbol	Conditions	CCB Command				min	typ	max	unit
				IN1	IN2	IN3-1	IN3-2				
1	FE_GND	V1AM		33	15	26	26	0			V
2	OSC_V_{CC}	V2AM		33	15	26	26			8	V
3	OSC_B	V3AM		33	15	26	26		2.65		V
4	OSC_C	V4AM		33	15	26	26		7.45		V
5	VT	V5AM		33	15	26	26	0		8	V
6	FET_GND	V6AM		33	15	26	26	0			V
7	PLL-LPF	V7AM		33	15	26	26		*		V
8	FM FET	V8AM		33	15	26	26		*		V
9	AM FET	V9AM		33	15	26	26		*		V
10	CPAM	V10AM		33	15	26	26		*		V
11	CPFM	V11AM		33	15	26	26		*		V
12	GND (Digital)	V12AM		33	15	26	26	0			V
13	V_{CC} (X'TAL)	V13AM		33	15	26	26			5	V
14	X'tal IN	V14AM		33	15	26	26		2.7		V
15	X'tal OUT	V15AM		33	15	26	26		4.1		V
16	GND (X'TAL)	V16AM		33	15	26	26	0			V
17	X'tal-Buffer-OUT	V17AM		33	15	26	26		3.45		V
18	CE	V18AM		33	15	26	26		BUS		V
19	DI	V19AM		33	15	26	26		BUS		V
20	CL	V20AM		33	15	26	26		BUS		V
21	DO	V21AM		33	15	26	26	0		Note 1	V
22	V_{CC} 5V (Digital)	V22AM		33	15	26	26			5	V
23	PLL V_{DD} (3V REG)	V23AM		33	15	26	26		3.1		V
24	PLL V_{DD} (4V REG)	V24AM		33	15	26	26		4.15		V
25	AGC-Control-IN (HD)	V25AM		33	15	26	26		Input		V
26	AGC-Control-IN (Analog)	V26AM		33	15	26	26		Input		V
27	IFAGC-OUTN (HD)	V27AM		33	15	26	26		2.75		V

Continued on next page.

Continued from preceding page.

Pin No.	Parameter	Symbol	Conditions	CCB Command				min	typ	max	unit
				IN1	IN2	IN3-1	IN3-2				
28	IFAGC-OUTP (HD)	V28AM		33	15	26	26		2.75		V
29	IFAGC-OUTN (Analog)	V29AM		33	15	26	26		2.75		V
30	IFAGC-OUTP (Analog)	V30AM		33	15	26	26		2.75		V
31	DIV-IF-OUT	V31AM		33	15	26	26		1.95		V
32	VSM-DC	V32AM		33	15	26	26	0		5	V
33	2.7V REG	V33AM		33	15	26	26		2.7		V
34	IFAGC-IN (Analog-Bypass)	V34AM		33	15	26	26		2.2		V
35	IFAGC-IN (HD-Bypass)	V35AM		33	15	26	26		2.1		V
36	GND (Analog)	V36AM		33	15	26	26		0		V
37	IFAGC-IN (Analog)	V37AM		33	15	26	26		2.2		V
38	VSM-AC	V38AM		33	15	26	26	0		5	V
39	IFAGC-IN (HD)	V39AM		33	15	26	26		2.1		V
40	V_{CC} 5V (Analog)	V40AM		33	15	26	26		5		V
41	AM-Narrow-AGC-IN	V41AM		33	15	26	26		*		V
42	Address SW/DAC-Monitor	V42AM		33	15	26	26		3.1		V
43	AM-1st-IF-OUT	V43AM		33	15	26	26		4.8		V
44	4.9V REG	V44AM		33	15	26	26		4.7		V
45	IF-Narrow-IN	V45AM		33	15	26	26		2.65		V
46	IF-Narrow-IN (Bypass)	V46AM		33	15	26	26		2.65		V
47	AM-Wide-AGC (Bypass)	V47AM		33	15	26	26		2.25		V
48	IF-Wide-IN	V48AM		33	15	26	26		2.4		V
49	IF-Wide-IN (Bypass)	V49AM		33	15	26	26		2.4		V
50	AM-RF-AGC	V50AM		33	15	26	26		6.45		V
51	AM-RF-AGC (Bypass)	V51AM		33	15	26	26		0.8		V
52	AM-ANT-D	V52AM		33	15	26	26	0			V
53	FM-Narrow-AGC-IN	V53AM		33	15	26	26		0.4		V
54	FM/AM-MIX-OUT	V54AM		33	15	26	26			8	V
55	FM/AM-MIX-OUT	V55AM		33	15	26	26			8	V
56	ANT-DAC	V56AM		33	15	26	26	0		8	V
57	RF-DAC	V57AM		33	15	26	26	0		8	V
58	V_{CC} (8V)	V58AM		33	15	26	26			8	V
59	AM-MIX-IN	V59AM		33	15	26	26		2.65		V
60	AM-MIX-IN	V60AM		33	15	26	26		2.65		V
61	FM-MIX-IN	V61AM		33	15	26	26			1.5	V
62	FM-MIX-IN	V62AM		33	15	26	26			1.5	V
63	FM-RF-AGC	V63AM		33	15	26	26		7		V
64	FM-ANT-D	V64AM		33	15	26	26	0			V

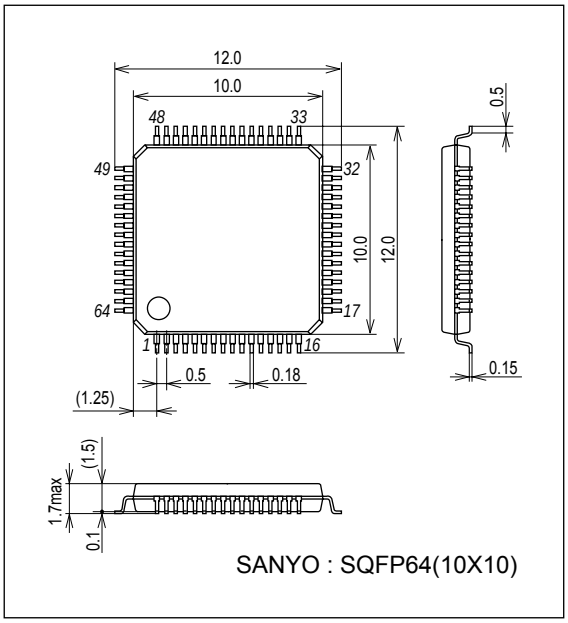
Parameter	Symbol	Conditions	CCB Command				min	typ	max	unit
			IN1	IN2	IN3-1	IN3-2				
TUNER OFF	V33		19	37	25	25		0.03		V

Parameter	Symbol	Conditions	CCB Command				min	typ	max	unit
			IN1	IN2	IN3-1	IN3-2				
ANT-DAC										
ALL_OFF (000000000)	DAC560		15	13	1	25	105		285	mV
D10_SETP (100000000)	DAC561	(DAC56_1)-(DAC56_0)	15	13	2	25	3		20	mV
D11_SETP (010000000)	DAC562	(DAC56_2)-(DAC56_0)	15	13	3	25	5		35	mV
D12_SETP (001000000)	DAC563	(DAC56_3)-(DAC56_0)	15	13	5	25	15		65	mV
D13_SETP (000100000)	DAC564	(DAC56_4)-(DAC56_0)	15	13	7	25	35		125	mV
D14_SETP (000010000)	DAC565	(DAC56_5)-(DAC56_0)	15	13	9	25	120		250	mV
D15_SETP (000001000)	DAC566	(DAC56_6)-(DAC56_0)	15	13	11	25	310		490	mV
D16_SETP (000000100)	DAC567	(DAC56_7)-(DAC56_0)	15	13	13	25	730		960	mV
D17_SETP (000000010)	DAC568	(DAC56_8)-(DAC56_0)	15	13	15	25	1.5		1.9	V
D18_SETP (000000001)	DAC569	(DAC56_9)-(DAC56_0)	15	13	17	25	3.05		3.75	V
ALL_ON (111111111)	DAC56A		15	13	18	25	6.25		7.55	V
RF-DAC										
ALL_OFF (111111111)	DAC570		15	13	1	25	105		285	mV
D0_SETP (100000000)	DAC571	(DAC57_1)-(DAC57_0)	15	13	2	25	3		20	mV
D1_SETP (010000000)	DAC572	(DAC57_2)-(DAC57_0)	15	13	3	25	5		35	mV
D2_SETP (001000000)	DAC573	(DAC57_3)-(DAC57_0)	15	13	5	25	15		65	mV
D3_SETP (000100000)	DAC574	(DAC57_4)-(DAC57_0)	15	13	7	25	35		125	mV
D4_SETP (000010000)	DAC575	(DAC57_5)-(DAC57_0)	15	13	9	25	120		250	mV
D5_SETP (000001000)	DAC576	(DAC57_6)-(DAC57_0)	15	13	11	25	310		490	mV
D6_SETP (000000100)	DAC577	(DAC57_7)-(DAC57_0)	15	13	13	25	730		960	mV
D7_SETP (000000010)	DAC578	(DAC57_8)-(DAC57_0)	15	13	15	25	1.5		1.9	V
D8_SETP (000000001)	DAC579	(DAC57_9)-(DAC57_0)	15	13	17	25	3.05		3.75	V
ALL_ON (111111111)	DAC57A		15	13	18	25	6.25		7.55	V

Package Dimensions

unit : mm (typ)

3190A



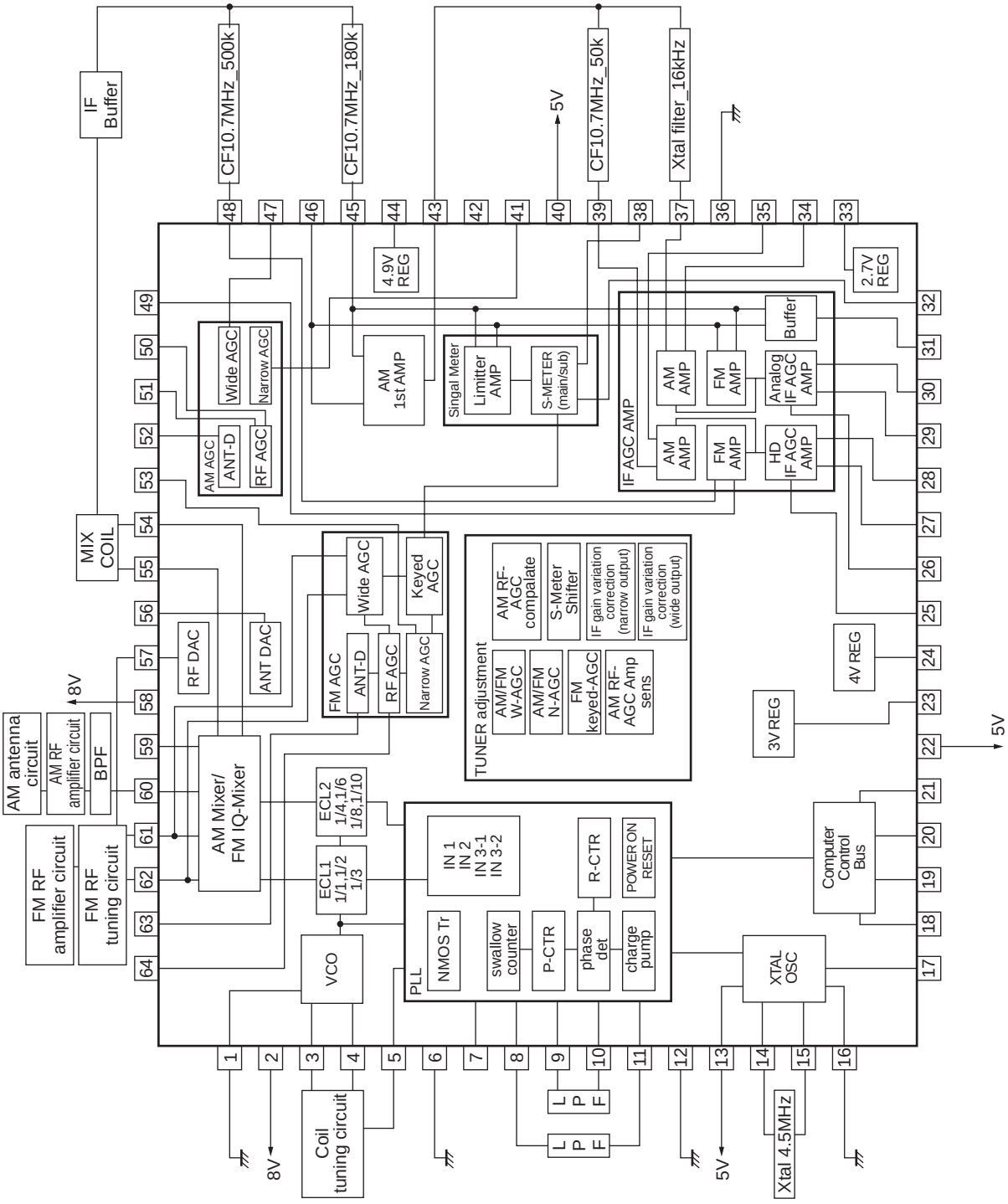
Pin Functions

Pin No.	Pin	Pin No.	Pin
1	FE_GND	33	VREG2.7V
2	OSC_V_{CC}	34	AM_ANALOG_IN Bypass
3	OSC_B	35	AM_HD_IN Bypass
4	OSC_C	36	AGND
5	PLL-VT	37	AM ANALOG IN
6	FET_GND	38	VSM_AC
7	PLL-LPF_AM	39	AM HD IN (35k CF)
8	FM_FET_OUT	40	V_{CC}A5V
9	AM_FET_OUT	41	AM_N-AGC pick-up
10	AM_CP	42	Address-SW
11	FM_CP	43	IF_OUT
12	DGND	44	VREG4.9V
13	XTAL_V_{CC}	45	IF-N_IN1 (CF = 180k)
14	XTAL-IN	46	IF-N_IN2 (180k_Bypass)
15	XTAL-OUT	47	AM-W-AGC
16	XTAL_GND	48	IF-W_IN1 (CF = 500k)
17	XTAL_OSC_OUT2	49	IF-W_IN2 (500k_Bypass)
18	CE	50	AM-RF-AGC
19	DI	51	AM RF-AGC (Bypass)
20	CL	52	AM-ANT-D
21	DO	53	FM N-AGC-IN
22	V_{CC}D5V	54	MIX-OUT
23	VREG 3V	55	MIX-OUT
24	VREG 4V	56	ANT-DAC
25	AGC_DAC_I	57	RF-DAC
26	AGC_DAC_S	58	FE_V_{CC}8V
27	HD-Radio out N	59	AM-MIX-IN2 (Bypass)
28	HD-Radio out P	60	AM-MIX-IN1
29	10.7M OUT N	61	FM-MIX-IN1
30	10.7M OUT P	62	FM-MIX-IN2
31	DIV_OUT_IF	63	FM-ANT D
32	VSM_DC	64	FM-RF-AGC

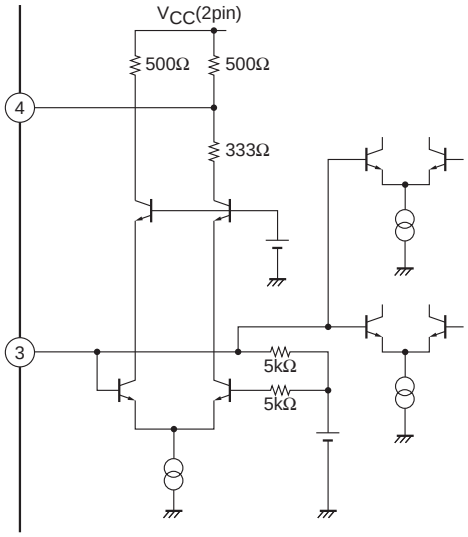
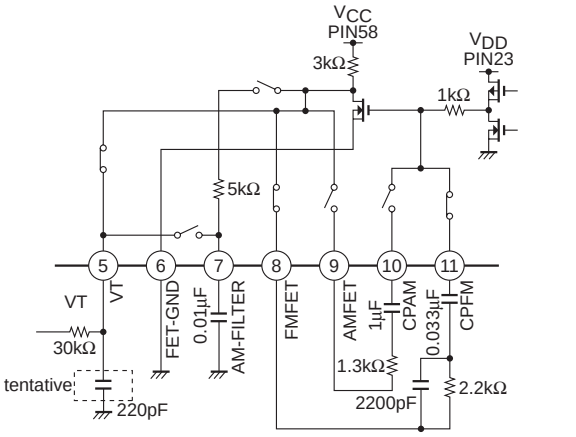
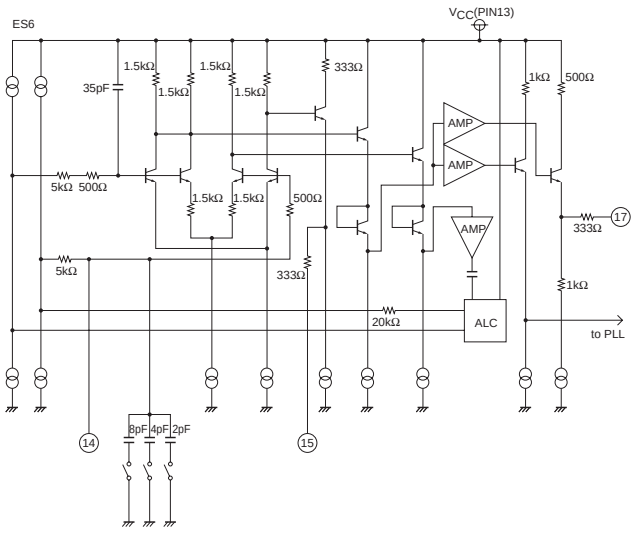
Functions

AM/FM front-end AGC block	
FM Image rejection Mixer (IQ-MIX)	Gain switching : 1 bit
FM IQ-MIX phase adjust (For the Japanese FM band)	2 bit DAC
AM Double balance Mixer	
Pin diode drive AGC output (AM/FM)	
Wide AGC sensitivity setting (AM/FM)	4 bit DAC
Narrow AGC sensitivity setting (AM/FM)	4 bit DAC
Keyed AGC adjust (FM)	4 bit DAC
AM RF AGC	4 bit DAC
Local oscillator	155MHz to 262MHz
Local osc divider (FM/AM)	Division by 1, 2, or 3
Local osc divider (AM)	Division by 10, 8, 6, or 4
ANT/RF DAC (FM)	9 bit DAC
AM 1st IF AMP block	
1st-IF amplifier 10.7M (Narrow)	
FM IF block	
S-meter shifter	5 bit DAC
IF Limiter Amplifier 6 stage	
S-meter (DC for keyed AGC) (FM)	
IF output Driver for DSP/iBoc (10.7MHz output)	
IF-AGC block	
IF AGC Amplifier (control Voltage from DSP)	
IF output Driver for DSP/iBoc	10.7MHz IF
IF Buffer Output for Diversity	10.7MHz IF
IF Gain Adjust	4 bit DAC
IF AGC Amp-OFF-Sw	For the analog system and the iBoc system ; 1 bit each
PLL	
Fast lock PLL	
Filter SW	1 bit SW
other	
Tuner off	1 bit SW
2.7V Regurator adjust	2 bit DAC

Block Diagram



Equivalent Circuits

Pin No.	Pin	Description	Equivalent Circuit
1	FE.GND		8V GND (F.E.)
2	OSC V_{CC}	Dedicated oscillator system power supply	8V V_{CC} (VCO.)
3 4	FM/AM OSC_B FM/AM OSC_C	Oscillator connections	
5 6 7 8 9 10 11	Tuning voltage output Low-pass filter output FET ground AM filter FM mode FET AM mode FET AM charge pump FM charge pump	FM mode : A PLL filter is formed on pins 8 through 11. (Pins 9 and 10 are left open.) AM mode : A PLL filter is formed on pins 7, 9, and 10. In this mode, a low-pass filter is formed by the internal impedance (10kΩ) and an external capacitor.	
12	DIGITAL GND		
13	XTAL V_{CC}	Dedicated crystal oscillator system power supply	5V V_{CC} (XTAL)
14 15	X'tal-OSC-IN X'tal-OSC-OUT	Connect a 4,5MHz crystal element between pins 14 and 15. Connect a 10pF capacitor between pin 14 and ground, and connect a 150pF capacitor between pin 15 and ground.	

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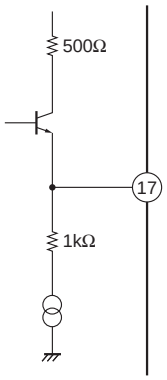
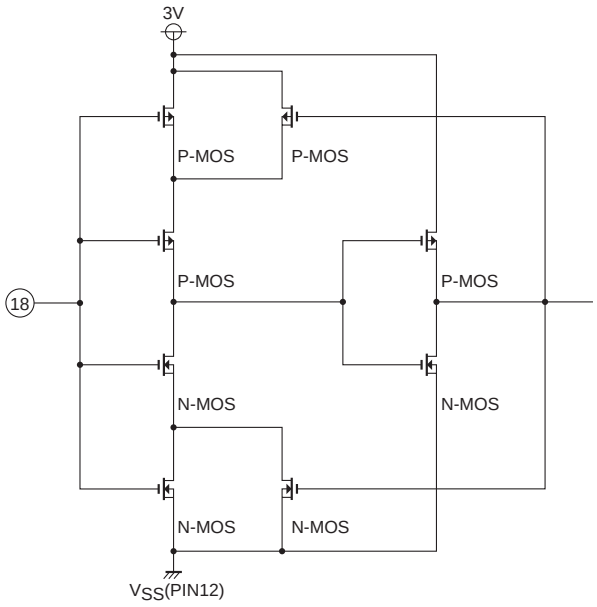
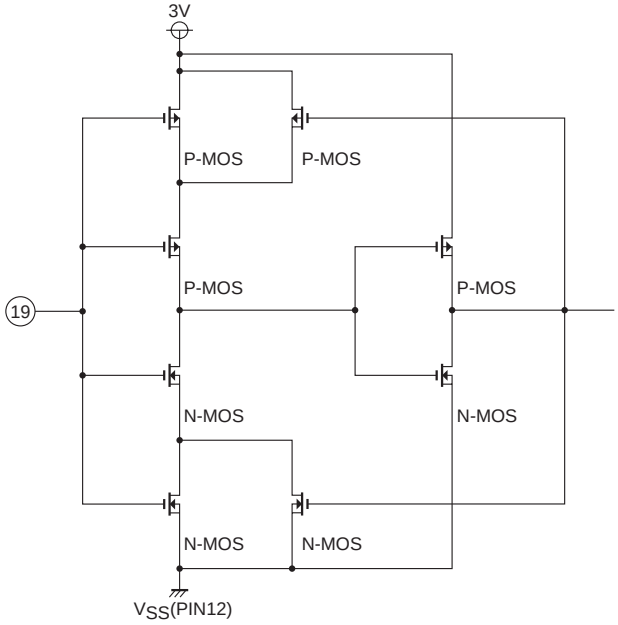
Pin No.	Pin	Description	Equivalent Circuit
16	XTAL GND	Dedicated crystal oscillator system ground	
17	XTAL OSC2	Crystal oscillator output 2 for use by a 2-tuner clock	
18	CE	Used to enable serial data input (DI) to the LV25400W or force the output to the high level during serial data output.	
19	DI	Input for the serial data transferred to the LV25400W from the controller.	

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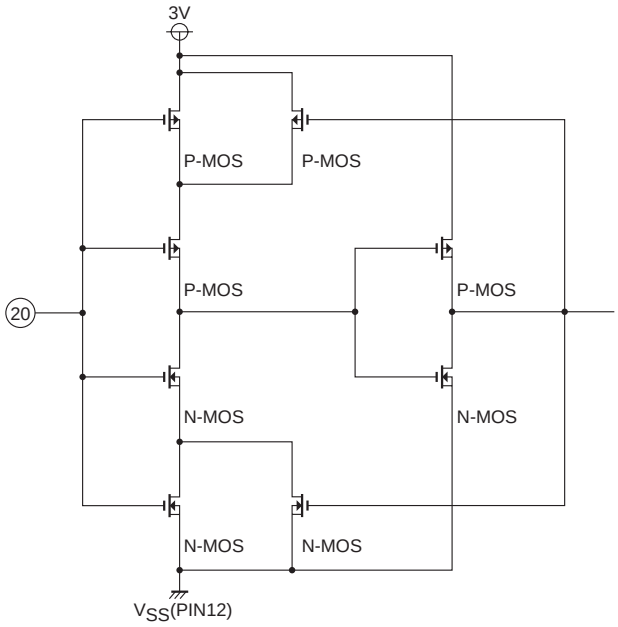
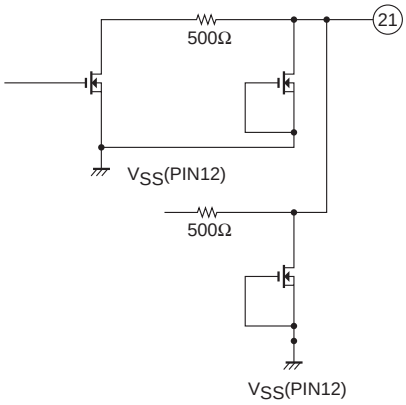
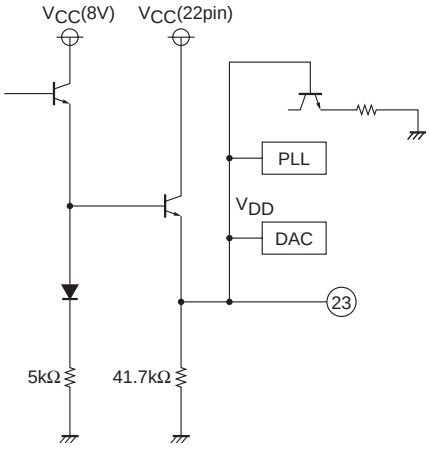
Pin No.	Pin	Description	Equivalent Circuit
20	CL	Clock used for synchronization when serial data is input to the LV25400W (DI) or when serial data is output (DO).	
21	DO	Output for serial data output to the controller by the LV25400W. Note : The pull-up resistor must be in the range 10kΩ to 50kΩ.	
22	$V_{CC}D$	Digital system power supply	5V V_{CC} (Digital)
23	PLL VREG (V_{DD}) - 3V	Regulator output for the PLL circuit - 3V	

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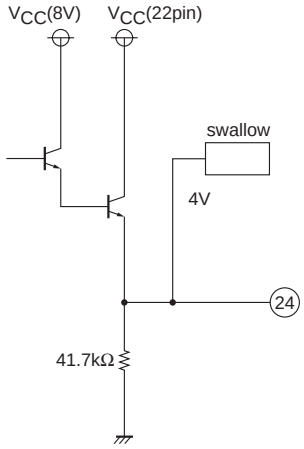
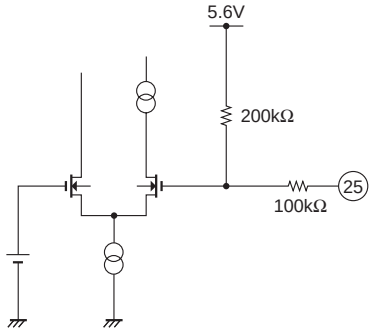
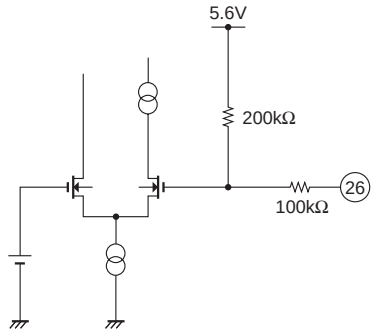
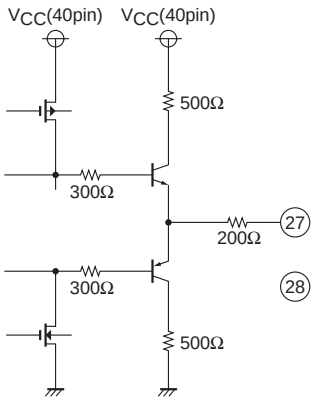
Pin No.	Pin	Description	Equivalent Circuit
24	Swallow counter VREG - 4V	Regulator output for the PLL swallow counter - 4V	
25	AGC_DAC_I	IF AGC control bias is supplied from the LC75040 (for iBoc).	
26	AGC_DAC_S	IF AGC control bias is supplied from the LC75040 (for the analog system).	
27 28	HD_OUTN HD_OUTP	Wideband IF (10.7MHz) signal differential output to the LC75040 for iBoc use.	

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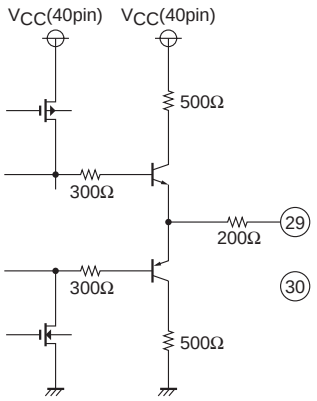
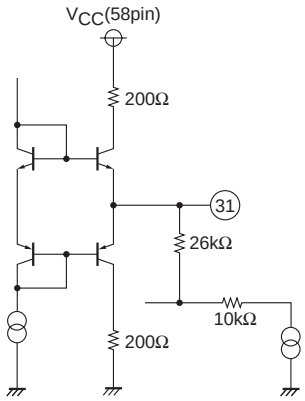
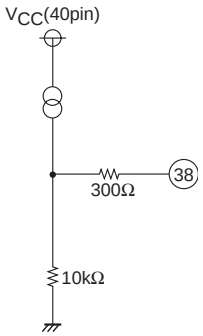
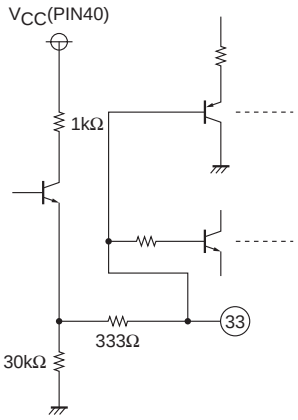
Pin No.	Pin	Description	Equivalent Circuit
29 30	10.7OUTN 10.7OUTP	Narrowband IF (10.7MHz) signal differential output to the LC75040 for analog use.	
31	DIV_OUT_IF	Driver 10.7MHz signal buffer output	
32	S-meter (DC)	Current driver S-meter output AC components are removed with an external capacitor.	
33	Vref 2.7V	2.7V regulator	

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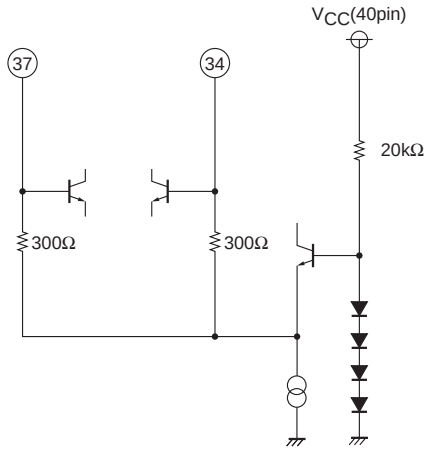
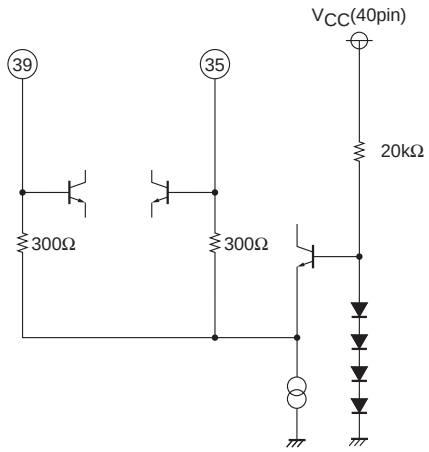
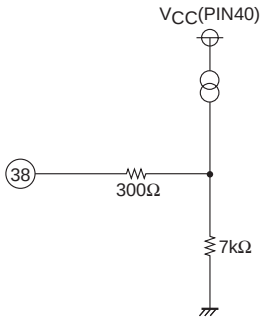
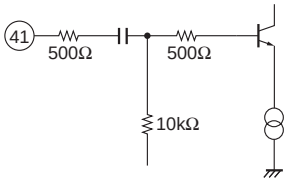
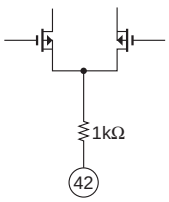
Pin No.	Pin	Description	Equivalent Circuit
34 37	AM ANALOG_IN Bypass AM ANALOG_IN	AM analog signal system related input (AM narrowband 10.7MHz IF signal)	
35 39	AM HD_IN Bypass AM HD_IN	iBoc and AM analog signal system related input (AM narrowband 10.7MHz IF signal)	
36	ANALOG GND		
38	S-meter AC output pin	FM mode: S-meter AC signal output	
40	V_{CC}A	Analog system power supply	5V V_{CC} (Analog)
41	AM Narrow-AGC Pick-Up	AM narrow AGC detection	
42	Address_SW	When two tuners are used, one of the two ICs' pin 42 is connected to ground, need changes the address.	

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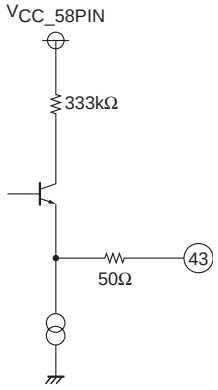
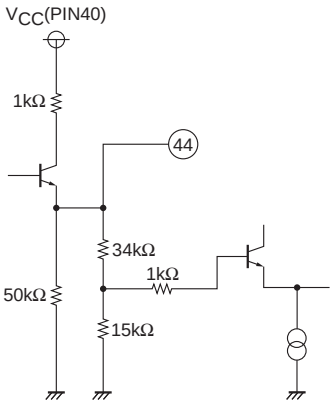
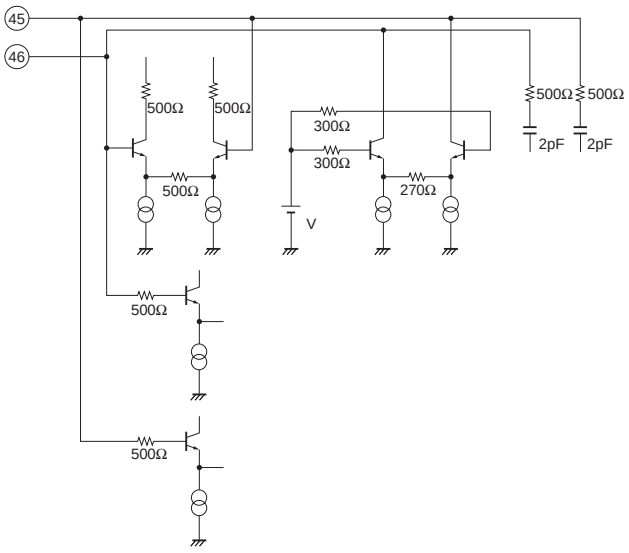
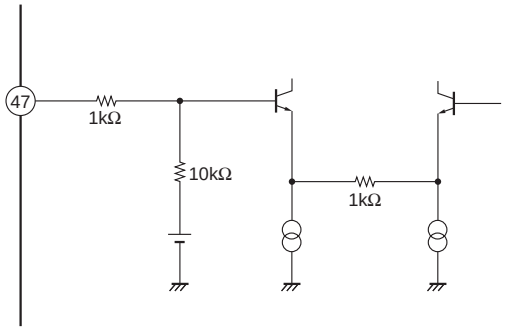
Pin No.	Pin	Description	Equivalent Circuit
43	AM 1stIF_AMP_OUT	First AM IF amplifier output	
44	VREG4.9V	4.9V regulator	
45 46	IF-N_IN1 IF-N_IN2	First AM IF amplifier input Driver 10.7MHz signal buffer input FM limiter amplifier input	
47	AM W-AGC	Used for wide AGC pickup. There is a built-in amplifier.	

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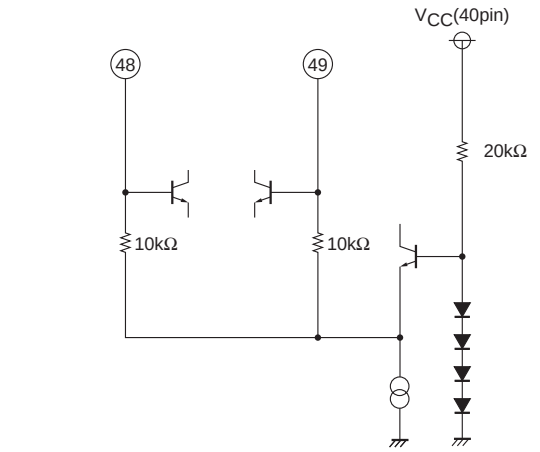
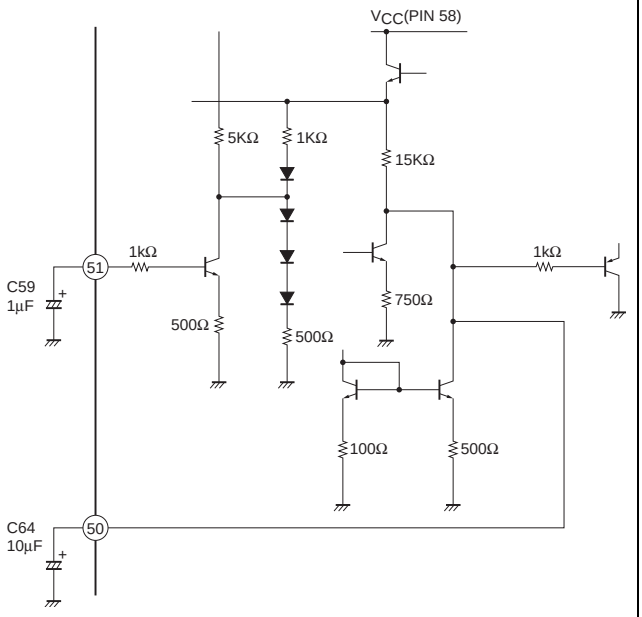
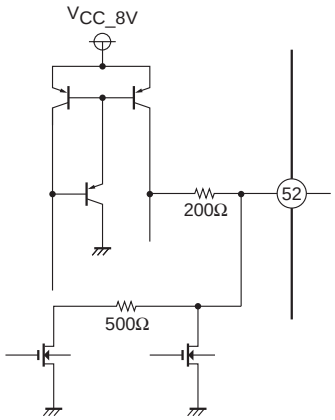
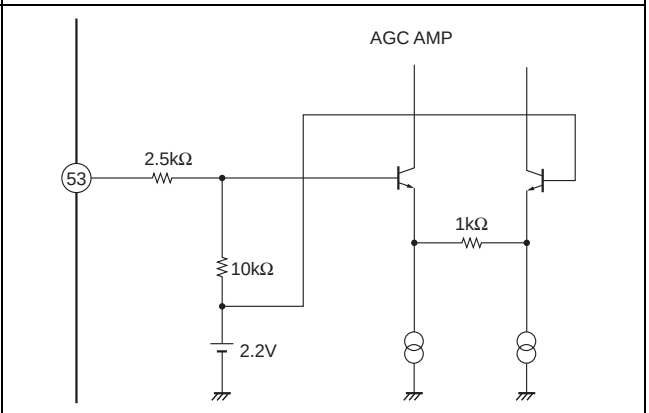
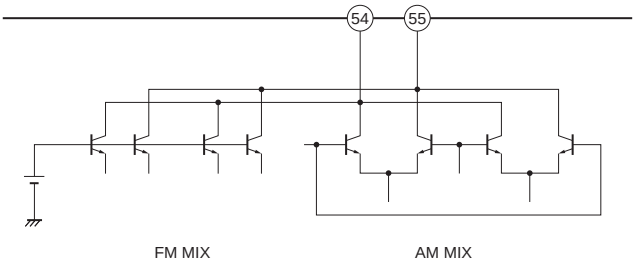
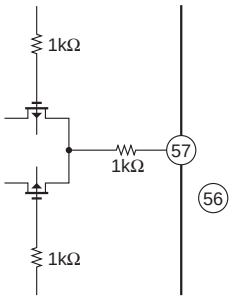
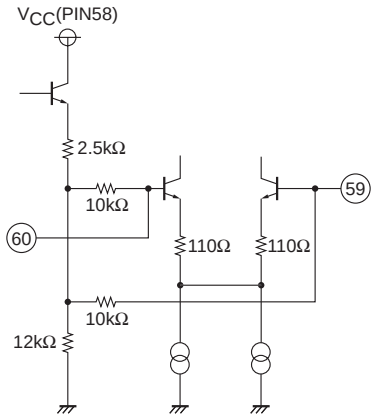
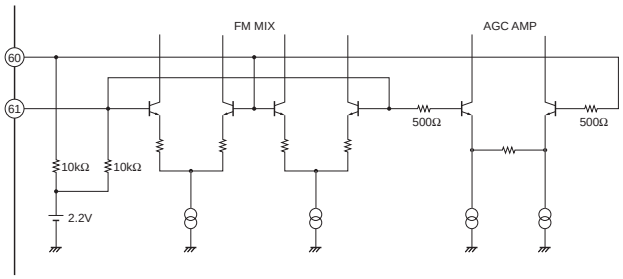
Pin No.	Pin	Description	Equivalent Circuit
48 49	FM IF-W_IN1 FM IF-W_IN2	Wideband FM IF AGC clamp input	
50 51	AM RF-AGC AM RF-AGC-Bypass	RF AGC rectifying capacitor Determines the distortion for low-frequency modulation. Increasing the size of C50 and C 51 : Distortion → Improves Response → Becomes slower Reducing the size of C50 and C 51 : Distortion → Degrades Response → Becomes faster	
52	AM ANT-D	Provides the PIN diode drive current. I52 = 6mA This is the antenna dumping current.	

Continued on next page.

Continued from preceding page.

Pin No.	Pin	Description	Equivalent Circuit
53	FM Narrow AGC	Used for narrow AGC pickup. There is a built-in amplifier.	
54 55	AM/FM 1st-MIX OUT	FM/AM mixer output (common)	
56 57	ANT DAC RF DAC	9-bit D/A converter	
58	V_{CC}A		V_{CC}8V FM FE/AM
59 60	AM MIX-IN2 (Bypass) AM MIX-IN1	AM mixer input Input impedance : 10kΩ	
61 62	FM MIX-IN1 FM MIX-IN2	FM mixer input FM wide AGC pickup Input impedance : 10kΩ	

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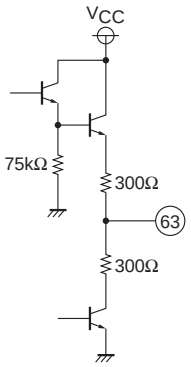
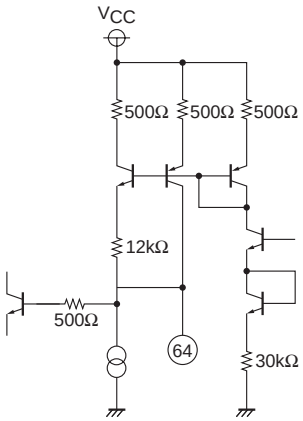
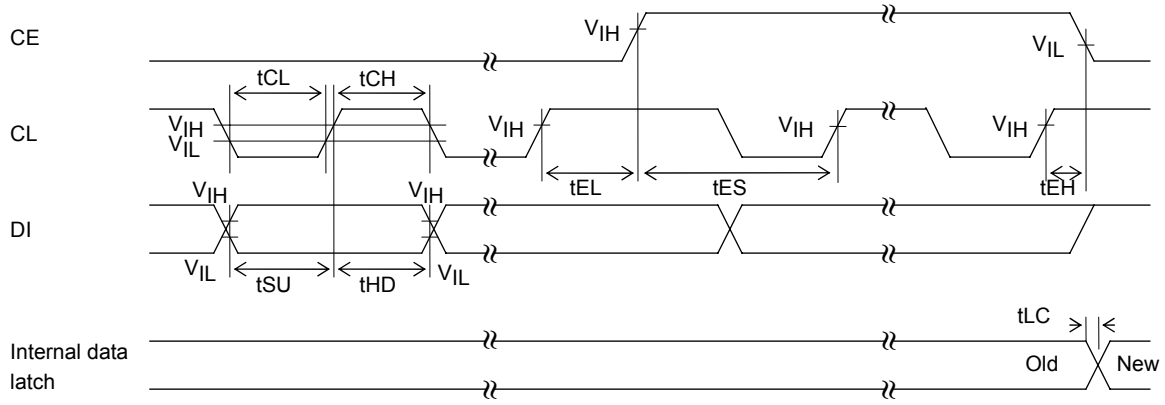
Continued from preceding page.

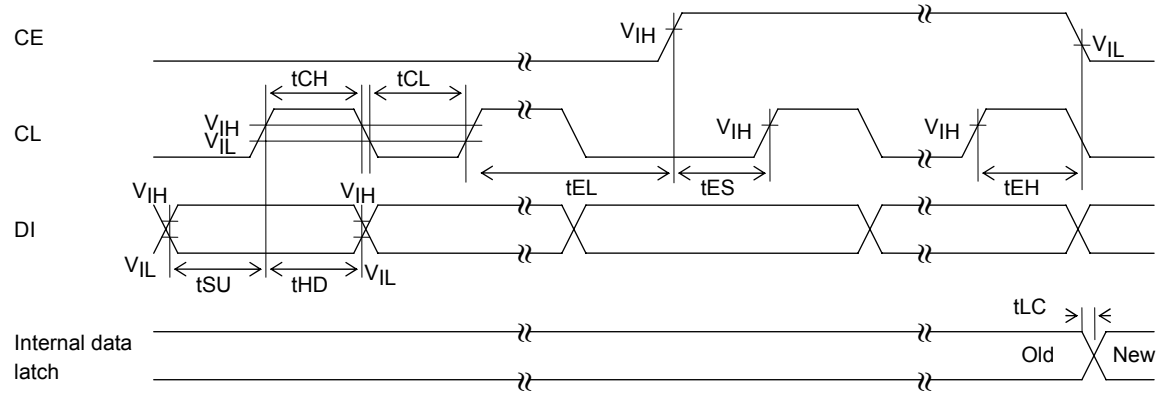
Pin No.	Pin	Description	Equivalent Circuit
63	FM ANT D	Pin 63 : The antenna driving current flows when the RF AGC voltage reaches (V_{CC} - Vbe).	
64	FM RF AGC	RF AGC voltage	

SANYO Serial Bus Data Timing

CE : Chip enable
CL : Clock
DI : Data input
DO : Data output (pin information only)



〈〈 When CL is stopped at the L level 〉〉



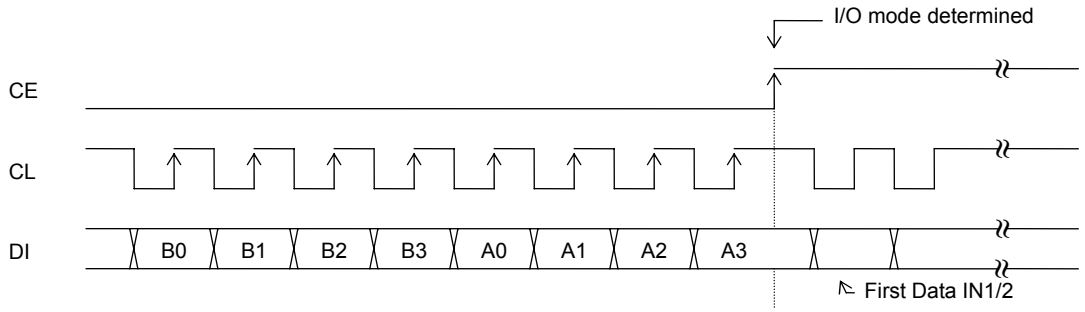
〈〈 When CL is stopped at the H level 〉〉

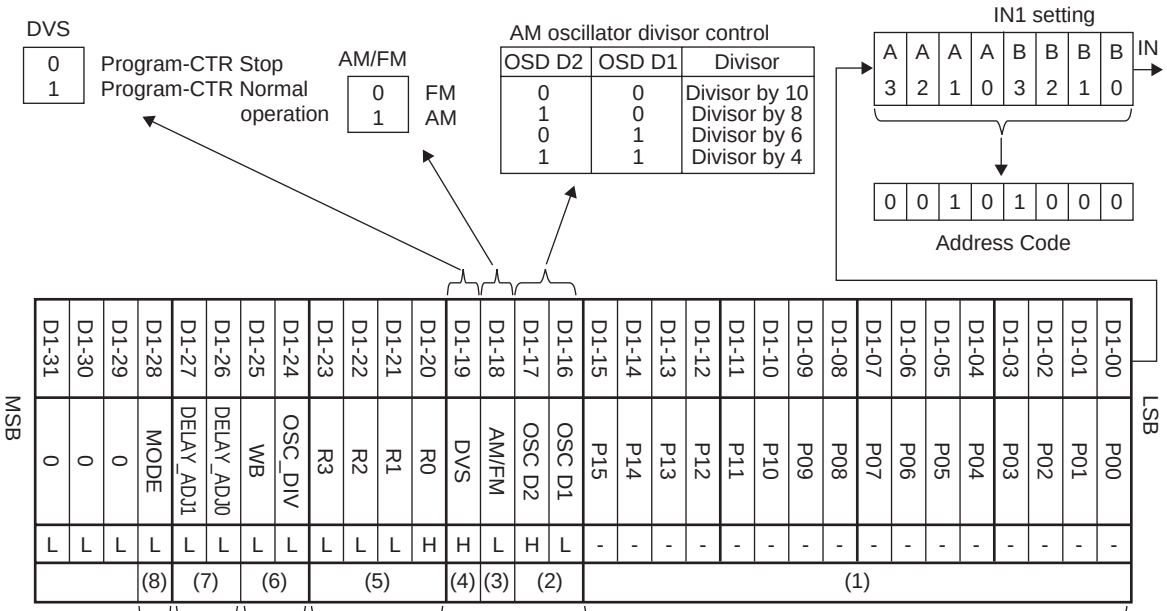
Parameter	Symbol	Pin	Conditions	min	typ	max	unit
Data setup time	tSU	DI, CL		0.45			μs
Data hold time	tHD	DI, CL		0.45			μs
Clock L-level time	tCL	CL		0.45			μs
Clock H-level time	tCH	CL		0.45			μs
CE wait time	tEL	CE, CL		0.45			μs
CE setup time	tES	CE, CL		0.45			μs
CE hold time	tEH	CE, CL		0.45			μs
Data latch change time	tLC					0.45	μs
Data input high-level voltage	V_{IH}	CL, DI, CE		2.5		5.0	V
Data input low-level voltage	V_{IL}	CL, DI, CE		-0.3		0.8	V

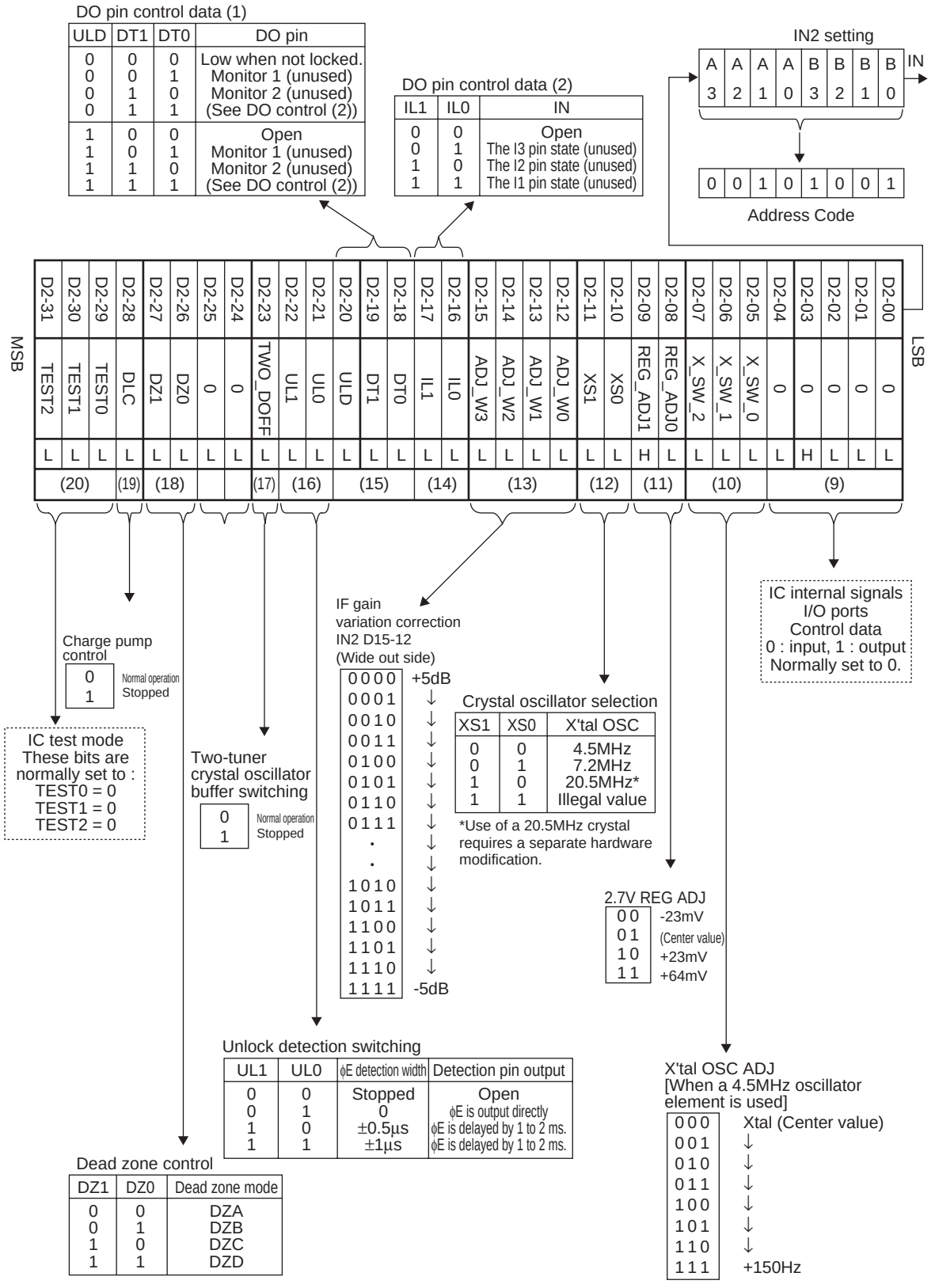
Serial Data I/O Procedures

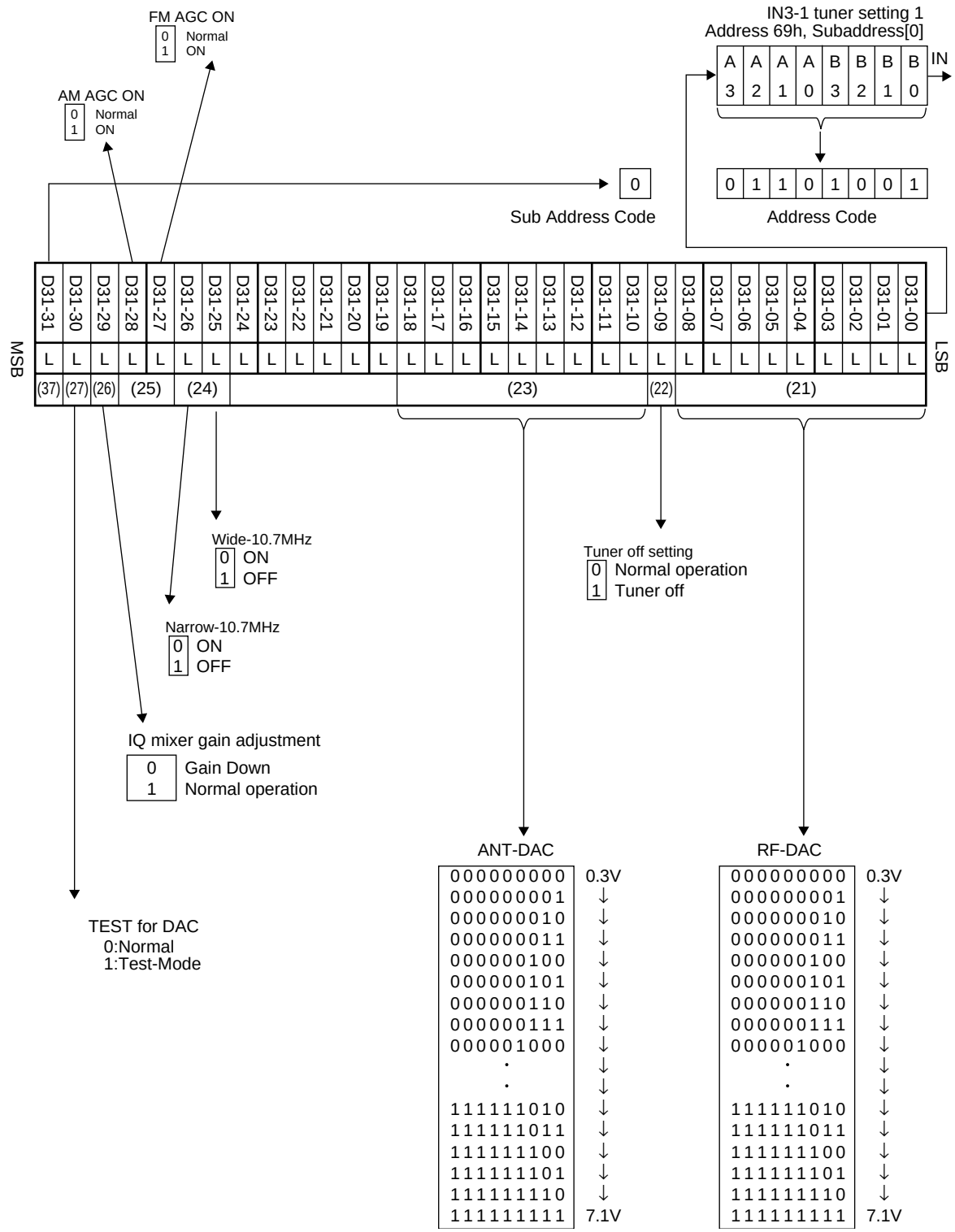
The LV25400W uses the SANYO audio IC serial bus format. Data is input and output using a CCB (Computer Control Bus). The LV25400W adopts an 8-bit address version of the CCB format.

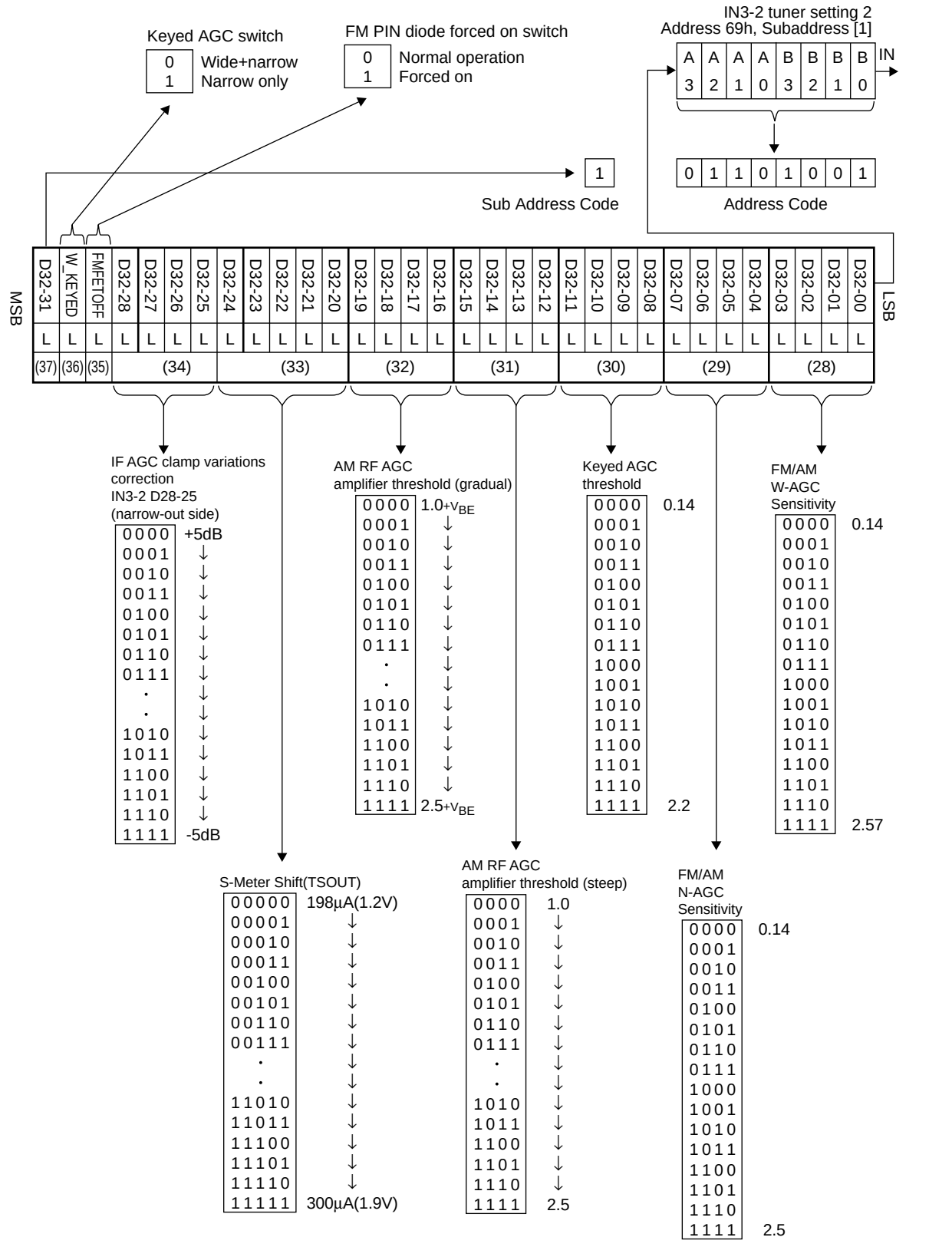
	I/O mode	Address								Contents
		B0	B1	B2	B3	A0	A1	A2	A3	
[1]	IN1	0	0	0	1	0	1	0	0	• Control data input mode. PLL setup • 32 bits of data are input • IN1B is the 2-tuner mode address (when pin 42 is tied to ground)
	IN1B	0	1	0	1	0	1	0	0	
[2]	IN2	1	0	0	1	0	1	0	0	• Control data input mode. PLL setup • 32 bits of data are input • IN2B is the 2-tuner mode address (when pin 42 is tied to ground)
	IN2B	1	1	0	1	0	1	0	0	
[3]	IN3	1	0	0	1	0	1	1	0	• The tuner block is set up in control data input (serial data input) mode. • 32 bits of data are input - There is a sub-address • IN3B is the 2-tuner mode address (when pin 42 is tied to ground)
	IN3B	0	0	0	1	0	1	1	0	




DVS
0
1
Program-CTR Stop
Program-CTR Normal operation
AM/FM
0
1
FM
AM
AM oscillator divisor control
OSD D2 | OSD D1 | Divisor
0 | 0 | Divisor by 10
1 | 0 | Divisor by 8
0 | 1 | Divisor by 6
1 | 1 | Divisor by 4
IN1 setting
A3 A2 A1 A0 B3 B2 B1 B0 IN
0 0 1 0 1 0 0 0
Address Code
D1-31 D1-30 D1-29 D1-28 D1-27 D1-26 D1-25 D1-24 D1-23 D1-22 D1-21 D1-20 D1-19 D1-18 D1-17 D1-16 D1-15 D1-14 D1-13 D1-12 D1-11 D1-10 D1-09 D1-08 D1-07 D1-06 D1-05 D1-04 D1-03 D1-02 D1-01 D1-00
MSB
0 0 0 MODE DELAY_ADJ1 DELAY_ADJ0 WB OSC_DIV R3 R2 R1 R0 DVS AM/FM OSC D2 OSC D1 P15 P14 P13 P12 P11 P10 P09 P08 P07 P06 P05 P04 P03 P02 P01 P00
LSB
L L L L L L L L L L L H H L H L - - - - - - - - - - - - - - - -
(8) (7) (6) (5) (4) (3) (2) (1)
AM/FM/WB oscillator divisor control
WB | OSD DIV | Divisor
0 | 0 | Divisor by 2
0 | 1 | Divisor by 3
1 | 0 | Divisor by 1
1 | 1 | Divisor by 1
*WB : Select 1 for weather band reception
Reference frequency setting
0 0 0 0 100kHz
0 0 0 1 50kHz
0 0 1 0 25kHz
0 0 1 1 25kHz
0 1 0 0 12.5kHz
0 1 0 1 6.25kHz
0 1 1 0 3.125kHz
0 1 1 1 3.125kHz
1 0 0 0 10kHz
1 0 0 1 9kHz
1 0 1 0 5kHz
1 0 1 1 1kHz
1 1 0 0 3kHz
1 1 0 1 30kHz
1 1 1 0 Illegal value
1 1 1 1 Illegal value
4.5, 7.2MHz
PLL filter switching
Filter state | MODE | AM/FM | AM filter | FM filter
Normal | 0 | 0 | OFF | ON
Normal | 0 | 1 | ON | OFF
W-FILTER | 1 | 0 | ON | ON
W-FILTER | 1 | 1 | ON | ON
FM-IQMIX phase_Adjust
DEIAY_ADJ0 | DEIAY_ADJ1 | Adjustment amount
0 | 0 | Small
1 | 0 | ↓
0 | 1 | ↓
1 | 1 | Large
Programmable counter divisor setting (from 272 to 65535)
0 0 0 0 0 0 0 1 0 0 0 1 0 0 0 0 Divide by 272
0 0 0 0 0 0 0 1 1 1 1 1 0 1 0 0 Divide by 500
0 0 0 0 0 0 1 1 1 1 1 0 1 0 0 0 Divide by 1000
0 0 0 0 0 1 1 1 1 1 0 1 0 0 0 0 Divide by 2000
0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 Divide by 21845
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 Divide by 43690
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 Divide by 65535


DO pin control data (1)
ULD DT1 DT0 DO pin
0 0 0 Low when not locked.
0 0 1 Monitor 1 (unused)
0 1 0 Monitor 2 (unused)
0 1 1 (See DO control (2))
1 0 0 Open
1 0 1 Monitor 1 (unused)
1 1 0 Monitor 2 (unused)
1 1 1 (See DO control (2))
DO pin control data (2)
IL1 IL0 IN
0 0 Open
0 1 The I3 pin state (unused)
1 0 The I2 pin state (unused)
1 1 The I1 pin state (unused)
IN2 setting
A3 A2 A1 A0 B3 B2 B1 B0 IN
0 0 1 0 1 0 0 1
Address Code
MSB
LSB
D2-31 D2-30 D2-29 D2-28 D2-27 D2-26 D2-25 D2-24 D2-23 D2-22 D2-21 D2-20 D2-19 D2-18 D2-17 D2-16 D2-15 D2-14 D2-13 D2-12 D2-11 D2-10 D2-09 D2-08 D2-07 D2-06 D2-05 D2-04 D2-03 D2-02 D2-01 D2-00
TEST2 TEST1 TEST0 DLC DZ1 DZ0 0 0 TWO_DOFF UL1 UL0 ULD DT1 DT0 IL1 IL0 ADJ_W3 ADJ_W2 ADJ_W1 ADJ_W0 XS1 XS0 REG_ADJ1 REG_ADJ0 X_SW_2 X_SW_1 X_SW_0 0 0 0 0 0
L L L L L L L L L L L L L L L L L L L L L L H L L L L H L L L
(20) (19) (18) (17) (16) (15) (14) (13) (12) (11) (10) (9)
Charge pump control
0 Normal operation
1 Stopped
IC test mode
These bits are normally set to :
TEST0 = 0
TEST1 = 0
TEST2 = 0
Two-tuner crystal oscillator buffer switching
0 Normal operation
1 Stopped
IF gain variation correction IN2 D15-12 (Wide out side)
0000 +5dB
0001 ↓
0010 ↓
0011 ↓
0100 ↓
0101 ↓
0110 ↓
0111 ↓
· ↓
· ↓
1010 ↓
1011 ↓
1100 ↓
1101 ↓
1110 ↓
1111 -5dB
Crystal oscillator selection
XS1 XS0 X'tal OSC
0 0 4.5MHz
0 1 7.2MHz
1 0 20.5MHz*
1 1 Illegal value
*Use of a 20.5MHz crystal requires a separate hardware modification.
2.7V REG ADJ
00 -23mV
01 (Center value)
10 +23mV
11 +64mV
IC internal signals
I/O ports
Control data
0 : input, 1 : output
Normally set to 0.
Unlock detection switching
UL1 UL0 φE detection width Detection pin output
0 0 Stopped Open
0 1 0 φE is output directly
1 0 ±0.5µs φE is delayed by 1 to 2 ms.
1 1 ±1µs φE is delayed by 1 to 2 ms.
Dead zone control
DZ1 DZ0 Dead zone mode
0 0 DZA
0 1 DZB
1 0 DZC
1 1 DZD
X'tal OSC ADJ
[When a 4.5MHz oscillator element is used]
000 Xtal (Center value)
001 ↓
010 ↓
011 ↓
100 ↓
101 ↓
110 ↓
111 +150Hz


FM AGC ON
0 Normal
1 ON
AM AGC ON
0 Normal
1 ON
IN3-1 tuner setting 1
Address 69h, Subaddress[0]
A3 A2 A1 A0 B3 B2 B1 B0 IN
0 1 1 0 1 0 0 1
Address Code
0
Sub Address Code
MSB
LSB
D31-31 D31-30 D31-29 D31-28 D31-27 D31-26 D31-25 D31-24 D31-23 D31-22 D31-21 D31-20 D31-19 D31-18 D31-17 D31-16 D31-15 D31-14 D31-13 D31-12 D31-11 D31-10 D31-09 D31-08 D31-07 D31-06 D31-05 D31-04 D31-03 D31-02 D31-01 D31-00
(37) (27) (26) (25) (24) (23) (22) (21)
Wide-10.7MHz
0 ON
1 OFF
Narrow-10.7MHz
0 ON
1 OFF
Tuner off setting
0 Normal operation
1 Tuner off
IQ mixer gain adjustment
0 Gain Down
1 Normal operation
TEST for DAC
0:Normal
1:Test-Mode
ANT-DAC
000000000 0.3V
000000001 ↓
000000010 ↓
000000011 ↓
000000100 ↓
000000101 ↓
000000110 ↓
000000111 ↓
000001000 ↓
· ↓
· ↓
111111010 ↓
111111011 ↓
111111100 ↓
111111101 ↓
111111110 ↓
111111111 7.1V
RF-DAC
000000000 0.3V
000000001 ↓
000000010 ↓
000000011 ↓
000000100 ↓
000000101 ↓
000000110 ↓
000000111 ↓
000001000 ↓
· ↓
· ↓
111111010 ↓
111111011 ↓
111111100 ↓
111111101 ↓
111111110 ↓
111111111 7.1V


Keyed AGC switch
0 Wide+narrow
1 Narrow only
FM PIN diode forced on switch
0 Normal operation
1 Forced on
IN3-2 tuner setting 2
Address 69h, Subaddress [1]
A3 A2 A1 A0 B3 B2 B1 B0 IN
0 1 1 0 1 0 0 1
Address Code
1
Sub Address Code
MSB
D32-31 W_KEYED FMFETOFF D32-28 D32-27 D32-26 D32-25 D32-24 D32-23 D32-22 D32-21 D32-20 D32-19 D32-18 D32-17 D32-16 D32-15 D32-14 D32-13 D32-12 D32-11 D32-10 D32-09 D32-08 D32-07 D32-06 D32-05 D32-04 D32-03 D32-02 D32-01 D32-00
LSB
(37) (36) (35) (34) (33) (32) (31) (30) (29) (28)
IF AGC clamp variations correction
IN3-2 D28-25
(narrow-out side)
0000 +5dB
0001
0010
0011
0100
0101
0110
0111
1010
1011
1100
1101
1110
1111 -5dB
AM RF AGC amplifier threshold (gradual)
0000 1.0+VBE
1111 2.5+VBE
Keyed AGC threshold
0000 0.14
1111 2.2
FM/AM W-AGC Sensitivity
0000 0.14
1111 2.57
S-Meter Shift(TSOUT)
00000 198μA(1.2V)
11010
11011
11100
11101
11110
11111 300μA(1.9V)
AM RF AGC amplifier threshold (steep)
0000 1.0
1111 2.5
FM/AM N-AGC Sensitivity
0000 0.14
1111 2.5

Control Data Documentation

<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data
P0 to P15

DVS</td><td>• Sets the programmable divider's divisor.
This is a binary value in which P0 is the LSB, P15 the MSB.
DVS = 0 : The IC internal FMIN pin is stopped (pulled down)
DVS = 1 : The IC internal FMIN pin is selected
Set divisor (N) : 272 to 65536
Input frequency range : 120 to 270 MHz
* : See the "Programmable Divider Structure" section for more information.</td><td>AM/FM
OSC D1, D2
WB, OSC DIV</td></tr>
<tr><td>(2)</td><td>AM oscillator divisor control

OSC D1, OSC D2</td><td>• OSC D1, OSC D2–AM oscillator divisor control
<table>
<tr><th>OSC D1</th><th>OSC D2</th><th>Divisor</th></tr>
<tr><td>0</td><td>0</td><td>Divide by 10</td></tr>
<tr><td>0</td><td>1</td><td>Divide by 8</td></tr>
<tr><td>1</td><td>0</td><td>Divide by 6</td></tr>
<tr><td>1</td><td>1</td><td>Divide by 4</td></tr>
</table></td><td>AM/FM
P0 to P15</td></tr>
<tr><td>(3)</td><td>Tuner mode switching

AM/FM</td><td>• Tuner mode switching between AM and FM
1 = AM 0 = FM</td><td>P0 to P15
OSC D1, D2</td></tr>
<tr><td>(4)</td><td>Programmable divider stop

DVS</td><td>• DVS = 0 : The IC internal PLL-IN pin is stopped (pulled down)
DVS = 1 : The IC internal PLL-IN pin is selected
Set divisor (N) : 272 to 65536
Input frequency range : 120 to 270 MHz
* : See the "Programmable Divider Structure" section for more information.</td><td>CTS
GT0, GT1
CTP
CTC</td></tr>
<tr><td>(5)</td><td>Reference divider data

R0 to R3</td><td>• Selects the reference frequency.
<table>
<tr><th colspan="4"></th><th colspan="2">Reference frequency setting (kHz)</th></tr>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Crystal : 20.5MHz</th><th>Crystal : 4.5/7.2MHz</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Illegal value</td><td>100</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>100</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>50</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Illegal value</td><td>9</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Illegal value</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Illegal value</td><td>30</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Illegal value</td><td>Illegal value</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Illegal value</td><td>Illegal value</td></tr>
</table></td><td></td></tr>
</table>

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<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(6)</td><td>Tuner mode switching

AM/FM oscillator divisor

OSC_DIV
WB</td><td>(1) AM/FM/WB oscillator divisor control
<table>
<tr><th>WB</th><th>OSC DIV</th><th>Divisor</th></tr>
<tr><td>0</td><td>0</td><td>Divide by 2</td></tr>
<tr><td>0</td><td>1</td><td>Divide by 3</td></tr>
<tr><td>1</td><td>0</td><td>Divide by 1</td></tr>
<tr><td>1</td><td>1</td><td>Divide by 1</td></tr>
</table>
* : WB: Select 1 for weather band reception

(2) AM oscillator divisor control
<table>
<tr><th>OSD D2</th><th>OSC D1</th><th>Divisor</th></tr>
<tr><td>0</td><td>0</td><td>Divide by 10</td></tr>
<tr><td>1</td><td>0</td><td>Divide by 8</td></tr>
<tr><td>0</td><td>1</td><td>Divide by 6</td></tr>
<tr><td>1</td><td>1</td><td>Divide by 4</td></tr>
</table>
In FM mode, only the WB and OSC DIV bits are valid.
In AM mode, this function is set up by combination of the OSC D2, OSC (however, this is fixed at the divide-by-2 setting) D1, WB, and the OSC DIV bits.
FM (Japan) : Fixed at the divide-by-3 setting
FM (other regions) : Fixed at the divide-by-2 setting
WB : Fixed at the divide-by-1 setting (OK if WB = 1)

In AM mode, set WB = 0, OSC DIV = 0 for the divide-by-2 setting.
The OSC D2 and OSC D1 bits can be set according to end product needs.

Example : USA : (1) <divide by 2> × (2) <divide by 10> = divide by 20
SW2 : (1) <divide by 2> × (2) <divide by 4> = divide by 8</td><td>P0 to P15
DVS</td></tr>
<tr><td>(7)</td><td>FM IQ mixer phase adjustment

DELAY_ADJ0
DELAY_ADJ1</td><td>• FM IQ mixer phase adjustment
FM-IQMIX phase_Adjust
<table>
<tr><th>DELAY_ADJ0</th><th>DELAY_ADJ1</th><th>Adjustment amount</th></tr>
<tr><td>0</td><td>0</td><td>Small</td></tr>
<tr><td>0</td><td>1</td><td>↓</td></tr>
<tr><td>1</td><td>0</td><td>↓</td></tr>
<tr><td>1</td><td>1</td><td>Large</td></tr>
</table></td><td>OSC_DIV</td></tr>
</table>

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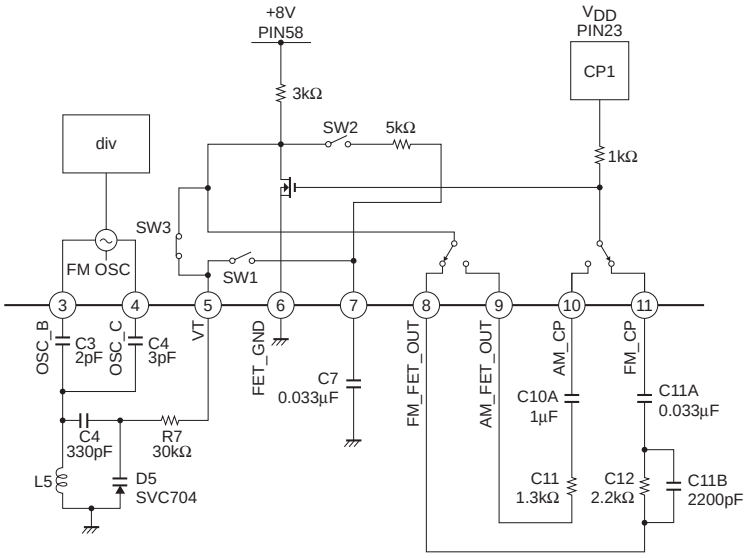
<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(8)</td><td>PLL filter switching mode

MODE</td><td>• Switches the PLL filter
PLL filter switching
<table>
<tr><th>Filter state</th><th>MODE</th><th>AM/FM</th><th>AM filter</th><th>FM filter</th></tr>
<tr><td rowspan="2">Normal</td><td rowspan="2">0</td><td>0</td><td>OFF</td><td>ON</td></tr>
<tr><td>1</td><td>ON</td><td>OFF</td></tr>
<tr><td rowspan="2">W-FILTER</td><td rowspan="2">1</td><td>0</td><td rowspan="2">ON</td><td rowspan="2">ON</td></tr>
<tr><td>1</td></tr>
</table>
Normal mode (MODE = 0)
The filter state is switched in conjunction with the AM/FM bit.

FM mode (AM/FM = 0)
A filter is formed on pins 8 and 11.
Since this filter can be independent of the filter used in AM mode, PLL locking can be fast.

AM mode (AM/FM = 1)
A filter is formed on pins 9 and 10 and with the two internal switches SW1 and SW2.
An additional filter is added using an internal resistor and an external capacitor.

W-filter mode (MODE = 1)
Both filters are enabled, regardless of the AM/FM bit.
(All of pins 8, 9, 10, and 11, and switches SW1 and SW2 are used.)

This is used when sidebands occur in AM mode, and in other cases.
However, there are case where, depending on the particular filter component values, this mode cannot be used.
 
</td><td>AM/FM</td></tr>
<tr><td>(9)</td><td>IC internal signals
I/O ports
Control data</td><td>• Specifies the I/O direction for the I/O ports
Data = 0 : Input port. The value 0 should be specified in normal operation.
= 1 : Output port. A value of 1 is used for IC testing.
* : This data must be set to 0 at all times other than IC evaluation.
Normally set to 0.</td><td></td></tr>
<tr><td>(10)</td><td>Crystal oscillator fine adjustment

X_SW_0
X_SW_1
X_SW_2</td><td>• Adjusts the crystal 4.5 MHz reference frequency if beating occurs

X'tal OSC ADJ [When a 4.5MHz oscillator element is used]
<table>
<tr><td>0 0 0</td><td>Xtal (Center value)</td></tr>
<tr><td>0 0 1</td><td>↓</td></tr>
<tr><td>0 1 0</td><td>↓</td></tr>
<tr><td>0 1 1</td><td>↓</td></tr>
<tr><td>1 0 0</td><td>↓</td></tr>
<tr><td>1 0 1</td><td>↓</td></tr>
<tr><td>1 1 0</td><td>↓</td></tr>
<tr><td>1 1 1</td><td>+150Hz</td></tr>
</table></td><td>XS0, XS1
R0 to R3</td></tr>
</table>

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<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(11)</td><td>2.7V REG ADJ

REG_ADJ0
REG_ADJ1</td><td>• Adjusts the 2.7 V regulator

2.7V REG ADJ
<table><tr><td>0 0</td><td>-23mV</td></tr><tr><td>0 1</td><td>(Center value)</td></tr><tr><td>1 0</td><td>+23mV</td></tr><tr><td>1 1</td><td>+64mV</td></tr></table></td><td></td></tr>
<tr><td>(12)</td><td>Crystal oscillator selection

XS0, XS1</td><td>• Selects the crystal element.
<table><tr><th>XS1</th><th>XS0</th><th>X’tal OSC</th></tr><tr><td>0</td><td>0</td><td>4.5MHz</td></tr><tr><td>0</td><td>1</td><td>Illegal value</td></tr><tr><td>1</td><td>0</td><td>Illegal value</td></tr><tr><td>1</td><td>1</td><td>Illegal value</td></tr></table></td><td></td></tr>
<tr><td>(13)</td><td>HD (wide) IF AGC amplifier variation correction bits

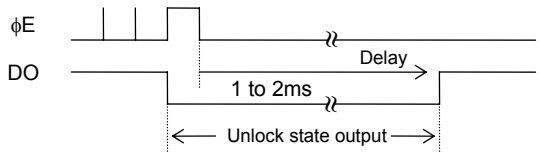
ADJ_W0
ADJ_W1
ADJ_W2
ADJ_W3</td><td>• Corrects for sample-to-sample variations in the IF AGC amplifier gain

Amount of correction : ±5 dB

4 bit</td><td></td></tr>
<tr><td>(14)</td><td>DO pin control data (2)

IL0, IL1</td><td>• Controls the DO pin output
DO pin control data (2)
<table><tr><th>IL1</th><th>IL0</th><th>IN</th></tr><tr><td>0</td><td>0</td><td>Open</td></tr><tr><td>0</td><td>1</td><td>The I3 pin state (unused)</td></tr><tr><td>1</td><td>0</td><td>The I2 pin state (unused)</td></tr><tr><td>1</td><td>1</td><td>The I1 pin state (unused)</td></tr></table>Since there are no connected pins in the current product, the open setting must be used.</td><td></td></tr>
<tr><td>(15)</td><td>DO pin control data (1)

ULD
DT0, DT1</td><td>• Determines the DO pin output.
DO pin control data (1)
<table><tr><th>ULD</th><th>IL0</th><th>DT0</th><th>DO pin</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Low when not locked.</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Monitor 1 (unused)</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Monitor 2 (unused)</td></tr><tr><td>1</td><td>1</td><td>1</td><td>(See DO control (2))</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Monitor 1 (unused)</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Monitor 2 (unused)</td></tr><tr><td>1</td><td>1</td><td>1</td><td>(See DO control (2))</td></tr></table>The following item (5) must also be set when monitoring the unlock detection signal.</td><td>UL0, UL1</td></tr>
<tr><td>(16)</td><td>Unlock state detection data

UL0, UL1</td><td>• Selects the phase error (øE) detection width used to judge the PLL locked state.
If a phase error in excess of the øE detection width from the table below occurs, the PLL is seen as being in the unlocked state.
When the PLL is seen as being unlocked, the detection pin (DO) is set low.
<table><tr><th>UL1</th><th>UL0</th><th>ϕE detection width</th><th>Detection pin output</th></tr><tr><td>0</td><td>0</td><td>Stopped</td><td>Open</td></tr><tr><td>0</td><td>1</td><td>0</td><td>ϕE is output directly</td></tr><tr><td>1</td><td>0</td><td>±0.5μs</td><td>ϕE is delayed by 1 to 2 ms.</td></tr><tr><td>1</td><td>1</td><td>±1μs</td><td>ϕE is delayed by 1 to 2 ms.</td></tr></table> 
</td><td>ULD
DT0, DT1</td></tr>
</table>

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<table>
<tr><th>No.</th><th>Control block/data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(17)</td><td>Crystal oscillator buffer output stop switching

TWO_DOFF</td><td>• Stops the crystal oscillator buffer output.
1 bit Two-tuner crystal oscillator buffer switching
0 Normal operation
1 Stopped</td><td></td></tr>
<tr><td>(18)</td><td>Phase comparator control data

DZ0, DZ1</td><td>• Controls the phase comparator's dead zone.
<table><tr><th>DZ1</th><th>DZ0</th><th>Dead zone mode</th></tr><tr><td>0</td><td>0</td><td>DZA</td></tr><tr><td>0</td><td>1</td><td>DZB</td></tr><tr><td>1</td><td>0</td><td>DZC</td></tr><tr><td>1</td><td>1</td><td>DZD</td></tr></table>The DZA setting is selected after the power-on reset.</td><td></td></tr>
<tr><td>(19)</td><td>Charge pump control data

DLC</td><td>• Forcibly sets the charge pump output to the low level (V_{SS} level).
DLC = 1 : Low level
DLC = 0 : Normal operation
* : If the IC deadlocks with VCO oscillator stopped with the VCO control voltage (Vtune) at 0 V, the deadlock can be resolved by setting the charge pump output to the low level and setting Vtune to V_{CC}.
This item is set to the normal operation state after the power-on reset.</td><td></td></tr>
<tr><td>(20)</td><td>IC internal signal I/O port control data</td><td>• Specifies the I/O direction for the I/O ports

Data = 0 : Input port. The value 0 should be specified in normal operation.
= 1 : Output port. A value of 1 is used for IC testing.
* : This data must be set to 0 at all times other than IC evaluation.</td><td></td></tr>
<tr><td>(21)</td><td>RF tuning D/A converter output
D31-00 to D31-08</td><td>• Applies a control voltage to the RF tuning circuit (varactor).

9 bit</td><td></td></tr>
<tr><td>(22)</td><td>Tuner off setting

D31-09</td><td>• Set the IC to tuner off mode.

1 bit Tuner OFF mord
0 Normal operation
1 Tuner-OFF</td><td></td></tr>
<tr><td>(23)</td><td>Antenna tuning D/A converter output

D31-10 to D31-18</td><td>• Applies a control voltage to the antenna tuning circuit (varactor).

9 bit</td><td></td></tr>
<tr><td>(24)</td><td>IF AGC amplifier (narrow/wide) on/off switching

D31-25
D31-26</td><td>• Operates the IF AGC amplifier circuit (narrow/wide).

D31-25 : wide-10.7MHz「0」= ON ,「1」= OFF
D31-26 : narrow-10.7MHz「0」= ON ,「1」= OFF

Each 1 bit</td><td></td></tr>
<tr><td>(25)</td><td>Forced AGC (AM/FM) switching

D31-27
D31-28</td><td>• Operates the forced AGC circuit (narrow/wide).

D31-27:FM AGC「0」= NORMAL,「1」= ON
D31-28:AM AGC「0」= NORMAL,「1」= ON

Each 1 bit</td><td></td></tr>
<tr><td>(26)</td><td>IQ mixer gain adjustment

D31-29</td><td>• Switches the FM IQ mixer gain.

1 bit IQ mixer gain adjustment
0 Gain Down
1 Normal operation</td><td></td></tr>
<tr><td>(27)</td><td></td><td></td><td></td></tr>
<tr><td>(28)</td><td>AM/FM wide AGC setting

D32-0 to D32-3</td><td>• Sets the AM/FM wide AGC sensitivity.

4 bit</td><td></td></tr>
</table>

Continued on next page.

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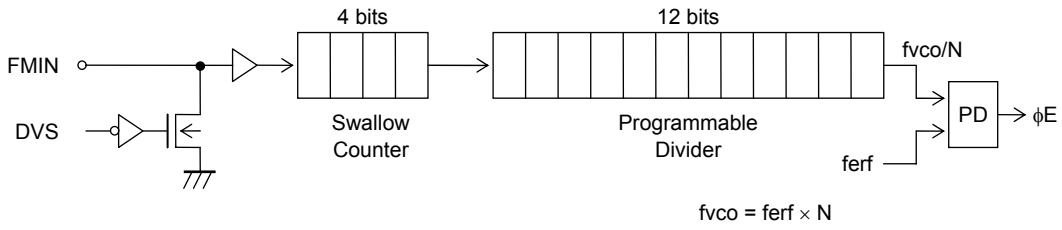
No.	Control block/data	Description	Related data
(29)	AM/FM narrow AGC setting D33-4 to D33-7	• Sets the AM/FM narrow AGC sensitivity. 4 bit	
(30)	Keyed AGC setting D32-8 to D32-11	• Controls the FM keyed AGC sensitivity. 4 bit	
(31)	AM RF AGC amplifier threshold (steep) setting D32-12 to D32-15	• Sets the AM RF AGC amplifier circuit threshold (steep). 4 bit	
(32)	AM RF AGC amplifier threshold (gradual) setting D32-16 to D32-19	• Sets the AM RF AGC amplifier circuit threshold (gradual). 4 bit	
(33)	S-meter shifter control D32-20 to D32-24	• Controls the FM S-meter shifter circuit output value. 5 bit	
(34)	Analog (narrow) IF AGC clamp variations correction D32-25 to D32-28	• Corrects the sample-to-sample variations in the IF AGC clamp circuit. Amount of correction : ±5 dB 4 bit	
(35)	FM PIN diode forced on state bit FMFETOFF	• Forcibly sets the FM PIN diode to the on state. 1 bit	
(36)	Keyed AGC connection circuit selection W_KEYED	• Modifies the keyed AGC connection circuit. 1 bit Keyed AGC switch 0 Wide + narroww 1 Narrow only	
(37)	D31-31 D32-31	• Sub-code address Each 1 bit	

Programmable Divider Structure



DVS	Set divisor (N)	Input frequency range (f (MHz))	IC internal FMIN pin
1	272 to 65535	120 ≤ f ≤ 270	Selected
0	-	-	Stopped

* : Since the IC is closed internally, the input sensitivity is not specified.

Phase Comparator and Charge Pump Circuits

(1) Phase comparator and charge pump operation

In the PLL circuit block shown in figure 1, the phase comparator compares the phases of the reference frequency (fr) and the comparison frequency (fp), and outputs the amount of the phase difference from the charge pump.

Figure 1 PLL Circuit Block

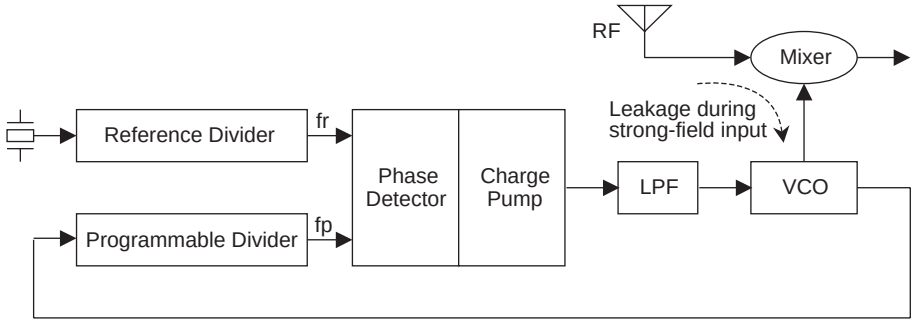
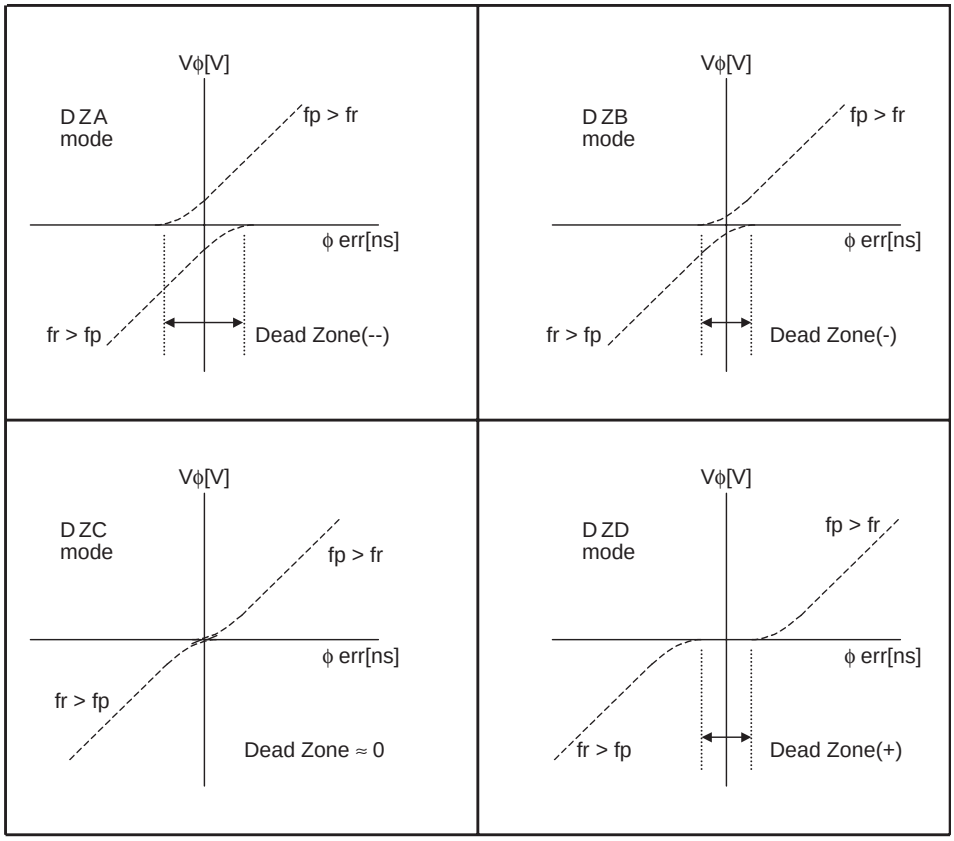


Figure 2 shows the phase comparator/charge pump output characteristics. The phase comparator outputs a voltage Vϕ that is proportional to the phase difference ϕ between fr and fp. The phase comparator's characteristics can be switched by changing the phase comparator dead zone mode setting. The phase comparator can be set to modes (DZA, DZB) in which both the charge pump p-channel and n-channel sides are turned on when the phase difference is small, or can be set to a mode (DZD) that does not output the phase difference when the phase difference is small.

Figure 2 Phase Comparator/Charge Pump Characteristics



(2) Dead zone mode characteristics

The table below presents an overview of the characteristics in each of the dead zone modes.

Setting		Dead zone mode	Charge pump (p/n-channel) state at 0 phase difference	Dead zone width (for reference purposes)	Notes
DZ1	DZ0				
0	0	DZA	On/on	- -(-15[ns])	
0	1	DZB	On/on	- (-8[ns])	
1	0	DZC	On or off	Close to 0 (0[ns])	Illegal setting
1	1	DZD	Off/off	+ (+8[ns])	

(3) Dead zone mode characteristics and selection criteria

This section describes the characteristics of each dead zone mode and the criteria for selecting that mode.

(1) DZA mode

In DZA mode, the correction signal is output from the charge pump even if the reference frequency (fr) and comparison frequency (fp) match. This results in excellent signal-to-noise ratio characteristics. However, due to the generation of reference frequency component sidebands, beating may occur in the presence of a strong input signal. This is because the PLL loop responds sensitively to leakage components from the RF stage through the mixer and this modulates the VCO.

(2) DZB mode

Like DZA mode, in DZB mode the correction signal is output from the charge pump even if the reference frequency (fr) and comparison frequency (fp) match. However, the correction signal voltage is lower in DZB mode than in DZA mode. The feature of this mode is that it provides a better signal-to-noise ratio than DZC or DZD mode yet is less susceptible to beating than DZA mode.

(3) DZC mode

In DZC mode, a correction signal proportional to the phase difference between the reference frequency (fr) and comparison frequency (fp) is output from the charge pump. A small amount of noise may occur when the phase difference is close to 0 ns. Since the signal-to-noise ratio may degrade significantly at low temperatures (under -30°C), this mode should not be used.

(4) DZD mode

In DZD mode, a correction signal proportional to the phase difference between the reference frequency (fr) and comparison frequency (fp) is output from the charge pump. The correction signal is not output when the phase difference is in the vicinity of ± <a few ns>. As a result the signal-to-noise ratio is worse than the other modes, but the occurrence of beating is suppressed.

LV25400W bit control specification: reference values

1. FM S-Meter shifter

LSB				MSB	Functions
D32-20	D32-21	D32-22	D32-23	D32-24	
0	0	0	0	0	Vsm (DC) =1.87V : +5.6dB
					↑
0	0	0	0	1	Vsm (DC) = 2.15V : 0dB
					↓
1	1	1	1	1	Vsm (DC) = 2.45V : -6.0dB

2-1. FM IFAGC (HD)

LSB			MSB	Functions
D2-12	D2-13	D2-14	D2-15	
0	0	0	0	IFAGC (HD) -Amp-Gain : +4dB
				↑
1	1	0	1	IFAGC (HD) -Amp-Gain : 0dB
				↓
1	1	1	1	IFAGC (HD) -Amp-Gain : -4dB

2-2. AM IFAGC (HD)

LSB			MSB	Functions
D2-12	D2-13	D2-14	D2-15	
0	0	0	0	IFAGC (HD) -Amp-Gain : +4dB
				↑
1	1	0	1	IFAGC (HD) -Amp-Gain : 0dB
				↓
1	1	1	1	IFAGC (HD) -Amp-Gain : -4dB

3-1. FM IFAGC (Analog)

LSB			MSB	Functions
D32-25	D32-26	D32-27	D32-28	
0	0	0	0	IFAGC (Analog) -Amp-Gain : +4dB
				↑
1	1	0	1	IFAGC (Analog) -Amp-Gain : 0dB
				↓
1	1	1	1	IFAGC (Analog) -Amp-Gain : -4dB

3-2. AM IFAGC (Analog)

LSB			MSB	Functions
D32-25	D32-26	D32-27	D32-28	
0	0	0	0	IFAGC (Analog) -Amp-Gain : +4dB
				↑
1	1	0	1	IFAGC (Analog) -Amp-Gain : 0dB
				↓
1	1	1	1	IFAGC (Analog) -Amp-Gain : -4dB

4-1. FM Wide-AGC-ON-Level

LSB			MSB	Functions
D32-00	D32-01	D32-02	D32-03	
0	0	0	0	Wide-AGC-ON-Level : -8.5dB
				↑
1	1	1	0	Wide-AGC-ON-Level : 0dB
				↓
1	1	1	1	Wide-AGC-ON-Level : +5.5dB

4-2. AM Wide-AGC-ON-Level

LSB			MSB	Functions
D32-00	D32-01	D32-02	D32-03	
0	0	0	0	Wide-AGC-ON-Level : -8.5dB
				↑
1	1	1	0	Wide-AGC-ON-Level : 0dB
				↓
1	1	1	1	Wide-AGC-ON-Level : +7.0dB

5-1. FM Narrow-AGC-ON-Level

LSB			MSB	Functions
D32-04	D32-05	D32-06	D32-07	
0	0	0	0	Narrow-AGC-ON-Level : -9.5dB
				↑
1	1	1	0	Narrow-AGC-ON-Level : 0dB
				↓
1	1	1	1	Narrow-AGC-ON-Level : +6.5dB

5-2. AM Narrow-AGC-ON-Level

LSB			MSB	Functions
D32-04	D32-05	D32-06	D32-07	
0	0	0	0	Narrow-AGC-ON-Level : -9.0dB
				↑
1	1	1	0	Narrow-AGC-ON-Level : 0dB
				↓
1	1	1	1	Narrow-AGC-ON-Level : +5.0dB

6-1. Keyed-AGC-ON-Level

LSB			MSB	Functions
D32-08	D32-09	D32-10	D32-11	
0	0	0	0	Keyed-AGC-ON V32 : 0.27V
				↑
1	1	1	0	Keyed-AGC-ON V32 : 1.20V
				↓
1	1	1	1	Keyed-AGC-ON V32 : 2.25V

Data content

LV25400W (AC/DC) Serial data

	PLL IN1 data	CCB address								Control data 1								Control data 2								Control data 3								Control data 4								PLL Counter value	Delay-Adj
IN1	Data contents	A0	A1	A2	A3	A4	A5	A6	A7	P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	OSC_D1	OSC_D2	AM/FM	DVS	R0	R1	R2	R3	OSC_DIV	WB	DELAY_ADJ0	DELAY_ADJ1	MODE	- - - -	- - - -	- - - -		
15	FM_US98.1M fref = 100k	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	2176	0
33	MW1000k fref = 10k (USA)	0	0	0	1	0	1	0	0	0	0	0	1	0	1	1	0	1	1	0	1	1	0	1	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	23400	0
62	X45FM_US98.1M fref = 100k	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	2176	0
69	X45FM_JP83M fref = 100k Delay = 1	0	0	0	1	0	1	0	0	1	0	0	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	0	2169	1

	PLL IN2 data	CCB address								Control data 1								Control data 2								Control data 3								Control data 4								X'tal-Adj	IFAGC-Amp Gain (HD)
IN2	Data contents	A0	A1	A2	A3	A4	A5	A6	A7	I/O-1	I/O-2	I/O-3	I/O-4	I/O-5	X_SW_0	X_SW_1	X_SW_2	REG_ADJ0	REG_ADJ1	XS0	XS1	ADJ_W0	ADJ_W1	ADJ_W2	ADJ_W3	IL0	IL1	DT0	DT1	ULD	UL0	UL1	TWO_DOFF	- - - -	- - - -	DZ0	DZ1	DLC	TEST0	TEST1	TEST2		
13	FM reception mode settings	1	0	0	1	0	1	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	11
15	MW reception mode settings	1	0	0	1	0	1	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1	1	0	1	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	6	11
44	X45 MW reception mode settings	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0	11
48	X45X'tal_ADJ = 0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	11
50	X45Xtal_ADJ = 7 (IF_Dain_W = 11)	1	0	0	1	0	1	0	0	0	0	0	0	0	1	1	1	0	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	7	11

	PLL IN3-1 data	CCB address								Control data 1								Control data 2								Control data 3								Control data 4								RF-DAC	ANT-DAC
IN3-1	Data contents	A0	A1	A2	A3	A4	A5	A6	A7	RFDAC0	RFDAC1	RFDAC2	RFDAC3	RFDAC4	RFDAC5	RFDAC6	RFDAC7	RFDAC8	TUNEROFF	ANTDAC0	ANTDAC1	ANTDAC2	ANTDAC3	ANTDAC4	ANTDAC5	ANTDAC6	ANTDAC7	ANTDAC8	ANC_OFF	NC_AGC_SW	NOISE_AGC	AGC_LIMIT	NC_SENS0	NC_SENS1	WIDE_OFF	NARROW_OFF	FMAGC_ON	AMAGC_ON	IQMIX-Gain	DTESTSW	Sub-Address		
1	Bit-Check-0	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	Bit-Check-1	1	0	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
3	Bit-Check-2	1	0	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	2
5	Bit-Check-4	1	0	0	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4	4
7	Bit-Check-8	1	0	0	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8	8
9	Bit-Check-16	1	0	0	1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16	16
11	Bit-Check-32	1	0	0	1	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	32	32
13	Bit-Check-64	1	0	0	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	64	64
15	Bit-Check-128	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	128	128
17	Bit-Check-256	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	256	256
18	Bit-Check-511	1	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	511	511
25	Standard FM	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	256	256
26	Standard AM	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
27	FM-Wide-OFF	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	256	256
38	FM-IQMIX-GAIN-UP	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	256	256

	PLL IN3-2 data	CCB address								Control data 1								Control data 2								Control data 3								Control data 4								Wide-AGC	Narrow-AGC	Keyed-AGC	AM-RFAGC Hard	AM-RFAGC Soft	FM-S-meter Shifter	IFAGC-Amp Gain (Analog)
IN3-2	Data contents	A0	A1	A2	A3	A4	A5	A6	A7	W_AGC0	W_AGC1	W_AGC2	W_AGC3	N_AGC0	N_AGC1	N_AGC2	N_AGC3	KEY_AGC0	KEY_AGC1	KEY_AGC2	KEY_AGC3	RFAGC_H0	RFAGC_H1	RFAGC_H2	RFAGC_H3	RFAGC_S0	RFAGC_S1	RFAGC_S2	RFAGC_S3	S_METER0	S_METER1	S_METER2	S_METER3	S_METER4	ADJ_N0	ADJ_N1	ADJ_N2	ADJ_N3	FMFETOFF	W_KEYED	Sub-Address						
13	FM (W-AGC-Bit = 0)	1	0	0	1	0	1	1	0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	0	7	7	0	0	15	0
15	FM (W-AGC-Bit = 15)	1	0	0	1	0	1	1	0	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	15	7	7	0	0	15	0
16	FM (N-AGC-Bit = 0)	1	0	0	1	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	7	0	7	0	0	15	0
18	FM (N-AGC-Bit = 15)	1	0	0	1	0	1	1	0	1	1	1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	7	15	7	0	0	15	0
25	Standard FM-2	1	0	0	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	*	*	*	*	*	1	1	0	1	0	1	1	7	7	7	0	0	Adjust-ment	11
26	Standard AM-2	1	0	0	1	0	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	0	1	0	0	0	1	0	1	1	1	1	1	0	1	1	0	1	0	0	1	7	7	7	2	10	15	11
27	AM (W-AGC-Bit = 0)	1	0	0	1	0	1	1	0	0	0	0	0	1	1	1	0	1	1	1	0	0	1	0	0	0	1	0	1	1	1	1	1	0	1	1	0	1	0	0	1	0	7	7	2	10	15	11
29	AM (W-AGC-Bit = 15)	1	0	0	1	0	1	1	0	1	1	1	1	1	1	1	0	1	1	1	0	0	1	0	0	0	1	0	1	1	1	1	1	0	1	1	0	1	0	0	1	15	7	7	2	10	15	11
30	AM (N-AGC-Bit = 0)	1	0	0	1	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	1	1	1	1	0	1	1	0	1	0	0	1	7	0	7	2	10	15	11
32	AM (A-AGC-Bit = 15)	1	0	0	1	0	1	1	0	1	1	1	0	1	1	1	1	1	1	1	0	0	1	0	0	0	1	0	1	1	1	1	1	0	1	1	0	1	0	0	1	7	15	7	2	10	15	11

Items marked with an asterisk are Vsm adjustment items. The bit values after adjustment must be retained.

Sample Application Circuit