Document Title

Multi-Chip Package MEMORY

64M Bit (8Mx8) Nand Flash Memory / 32M Bit (2Mx16) UtRAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial issue.	Dec. 19th 2000	Advanced Information
0.1	Changed Device name K5Q6420YCM-TO70 -> K5Q6432YCM-T010 <UtRAM> - Improve operating current from 30mA to 25mA.. - Release speed from 70ns to 100ns. - Release standby current form 170µA to 200µA. - Add Power up timing diagram. - Add AC characteristics for continuous write.	Feb. 28th 2001	Preliminary
0.2	- Expand max operating temperature from 70°C to 85°C. - Changed I_{OL} / I_{OH} from 1.0mA/-0.5mA to 0.1mA/-0.1mA. <UtRAM> - Release standby current from 200uA to 250uA - Release deep power down current from 10uA to 20uA - Release tWC for continuous write operation from 100ns to 110ns - Release tCW for continuous write operation from 90ns to 100ns - Release tAW for continuous write operation from 90ns to 100ns - Release tBW for continuous write operation from 90ns to 100ns - Release tWP for continuous write operation from 90ns to 100ns	April. 6th 2001	Preliminary
0.3	<UtRAM> - Improve standby current from 250uA to 150uA	June. 11th 2001	Final

Note : For more detailed features and specifications including FAQ, please refer to Samsung's web site.
http://samsungelectronics.com/semiconductors/products/products_index.html

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Multi-Chip Package MEMORY

64M Bit (8Mx8) Nand Flash Memory / 32M Bit (2Mx16) UtRAM

FEATURES

- Power Supply voltage : 2.7V to 3.3 V
- Organization
  - Flash : (8M + 256K)bit x 8bit
  - UtRAM : 2M x 16 bit
- Access Time
  - Flash : Random access : 10us(Max.), Serial read : 50ns(Min.)
  - UtRAM : 100 ns
- Power Consumption (typical value)
  - Flash Read Current : 10 mA(@20MHz)
    Program/Erase Current : 10 mA
    Standby Current : 10 µA
  - UtRAM Operating Current : 18 mA
    Standby Current : 120 µA
- Flash Automatic Program and Erase
  Page Program : (512 + 16)Byte
  Block Erase : (8K + 256)Byte
- Flash Fast Write Cycle Time
  Program time : 300us(Typ.)
  Block Erase Time : 2ms(Typ.)
- Flash Endurance : 100,000 Program/Erase Cycles Minimum
- Flash Data Retention : 10 years
- Operating Temperature : -25°C ~ 85°C
- Package : 69 - ball TBGA Type - 8 x 13mm, 0.8 mm pitch

GENERAL DESCRIPTION

The K5Q6432YCM featuring single 3.0V power supply is a Multi Chip Package Memory which combines 64Mbit Nand Flash and 32Mbit Unit Transistor CMOS RAM.

The 64Mbit Flash memory is organized as 8M x8 bit and the 32Mbit UtRAM is organized as 2M x16 bit. In 64Mb NAND Flash a 528-byte page program can be typically achieved within 300us and an 8K-byte block erase can be typically achieved within 2ms. In serial read operation, a byte can be read by 50ns. The DQ pins serve as the ports for address and data input/output as well as command inputs. Even the write-intensive systems can take advantage of the FLASH's extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. These algorithms have been implemented in many mass storage applications and also the spare 16 bytes of a page combined with the other 512 bytes can be utilized by system-level ECC. The K5Q6432YCM is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 69-ball TBGA Type.

BALL CONFIGURATION

	1	2	3	4	5	6	7	8	9	10
A	N.C				N.C	N.C				N.C
B	Index		A7	$\overline{LB}$	CLE	$\overline{WE}$	A8	A11		
C		A3	A6	$\overline{UB}$	$\overline{CEf}$	$\overline{ZZ}$	A19	A12	A15	
D		A2	A5	A18	ALE	A20	A9	A13	N.C	
E	N.C	A1	A4	A17			A10	A14	Vccf	N.C
F	N.C	A0	Vss	DQ1			DQ6	N.C	A16	N.C
G		$\overline{WP}$	$\overline{OE}$/$\overline{RE}$	DQ9	DQ3	DQ4	DQ13	DQ15	R/$\overline{B}$	
H		$\overline{CSu}$	DQ0	DQ10	VccQF	Vccu	DQ12	DQ7	Vss	
J			DQ8	DQ2	DQ11	N.C	DQ5	DQ14		
K	N.C				N.C	N.C				N.C

69 Ball TBGA , 0.8mm Pitch
Top View (Ball Down)

BALL DESCRIPTION

Ball Name	Description
A_0 to A_{20}	Address Input Balls (UtRAM)
DQ_0 to DQ_7	Data Input/Output Balls (Common)
DQ_8 to DQ_{15}	Data Input/Output Balls (UtRAM)
Vccu	Power Supply (UtRAM)
VccF	Power Supply (Flash Memory)
VccQF	Output Buffer Power (Flash Memory) This input may be tied directly to VCCF.
Vss	Ground (Common)
$\overline{UB}$	Upper Byte Enable (UtRAM)
$\overline{LB}$	Lower Byte Enable (UtRAM)
$\overline{WP}$	Write Protection (Flash Memory)
CLE	Command Latch Enable(Flash Memory)
ALE	Address Latch Enable(Flash Memory)
$\overline{CE_F}$	Chip Enable (Flash Memory)
$\overline{CS_U}$	Chip Enable (UtRAM Low Active)
$\overline{ZZ}$	Deep Power Down(UtRAM High Active)
$\overline{WE}$	Write Enable (Common)
$\overline{OE}$/$\overline{RE}$	Output Enable (Common)
R/$\overline{B}$	Ready/Busy (Flash memory)
N.C	No Connection

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Figure 1. FUNCTIONAL BLOCK DIAGRAM

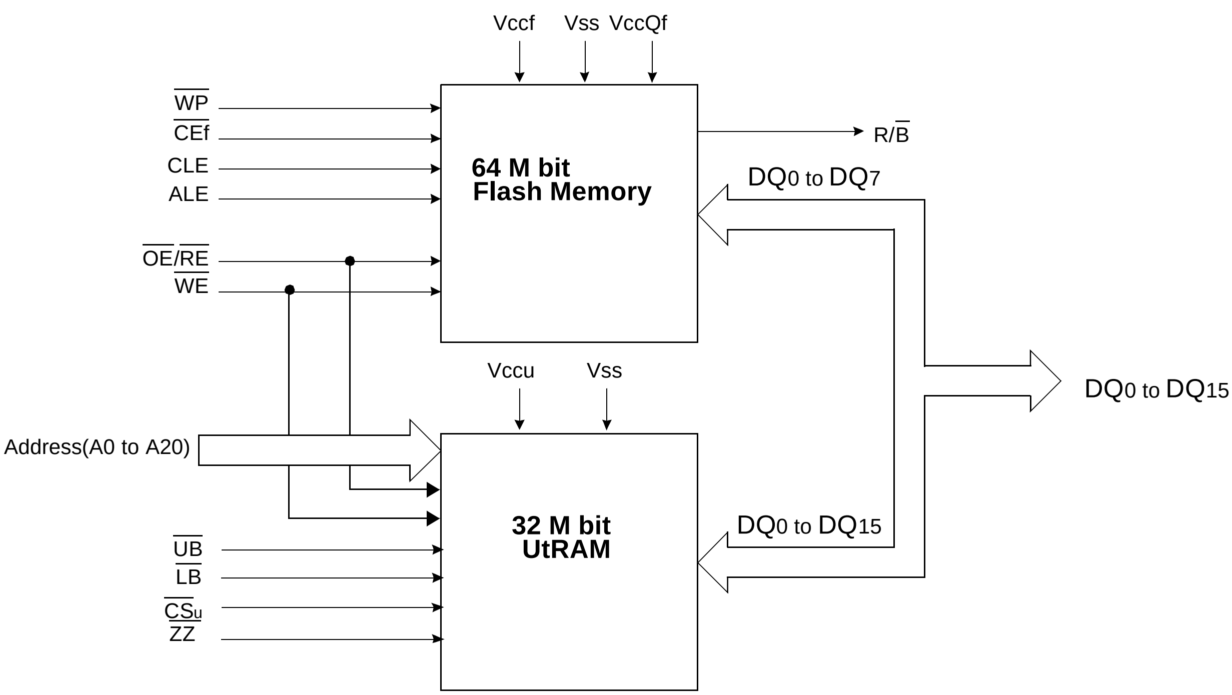
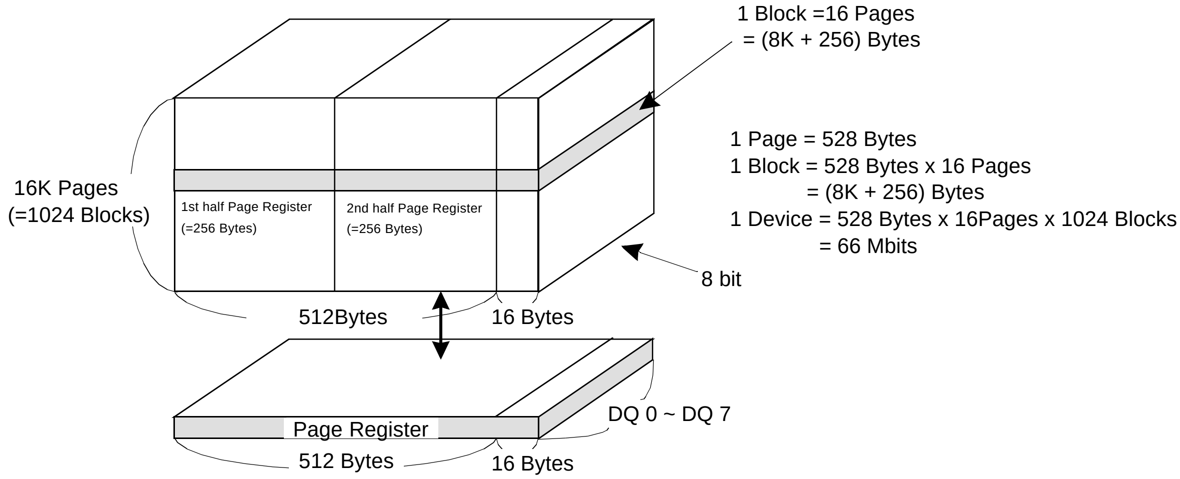


Figure 2. Flash ARRAY ORGANIZATION



	DQ 0	DQ 1	DQ 2	DQ 3	DQ 4	DQ 5	DQ 6	DQ 7	
1st Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	**Column Address**
2nd Cycle	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	**Row Address**
3rd Cycle	A_{17}	A_{18}	A_{19}	A_{20}	A_{21}	A_{22}	*L	*L	**(Page Address)**

NOTE : Column Address : Starting Address of the Register.
00h Command(Read) : Defines the starting address of the 1st half of the register.
01h Command(Read) : Defines the starting address of the 2nd half of the register.
* A_8 is set to "Low" or "High" by the 00h or 01h Command.
* L must be set to "Low"

NAND FLASH PRODUCT INTRODUCTION

The Flash Memory is a 69Mbit(69,206,016 bit) memory organized as 16,384 rows(pages) by 528 columns. Spare sixteen columns are located from column address of 512 to 527. A 528-byte data register is connected to memory cell arrays accommodating data transfer between the DQ buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells resides in a different page. A block consists of the 16 pages formed by one NAND structures, totaling 4,224 NAND structures of 16 cells. The array organization is shown in Figure 2. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 1024 separately erasable 8K-byte blocks. It indicates that the bit by bit erase operation is prohibited on the Flash Memory.

The Flash Memory has addresses multiplexed into 8 DQ′s. This scheme dramatically reduces pin counts and allows systems upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through DQ′s by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the DQ pins. All commands require one bus cycle except for Block Erase command which requires two cycles: one cycle for erase-setup and another for erase-execution after block address loading. The 8M byte physical space requires 23 addresses, thereby requiring three cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same three address cycles following the required command input. In Block Erase operation, however, only the two row address cycles are used.
Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the Flash Memory.

Table 1. COMMAND SETS

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy
Read 1	00h/01h(1)	-	
Read 2	50h	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Block Erase	60h	D0h	
Read Status	70h	-	O

NOTE : 1. The 00h command defines starting address of the 1st half of registers.
The 01h command defines starting address of the 2nd half of registers.
After data access on the 2nd half of register by the 01h command, the status pointer is automatically moved to the 1st half register(00h) on the next cycle.

Table 2. FLASH MEMORY OPERATIONS TABLE

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input(3clock)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input(3clock)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Sequential Read & Data Output	
L	L	X	H	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X[1]	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}[2]	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Table 3. UtRAM OPERATIONS TABLE

$\overline{CS}$	$\overline{ZZ}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	$DQ_{1\sim8}$	$DQ_{9\sim1}$	Mode	Power
H	H	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Deep Power Down
L	H	X[1]	X[1]	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X[1]	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X[1]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X[1]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X[1]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X[1]	L	L	L	Din	Din	Word Write	Active

1. X means don′t care.(Must be low or high state)

FLASH MEMORY OPERATION

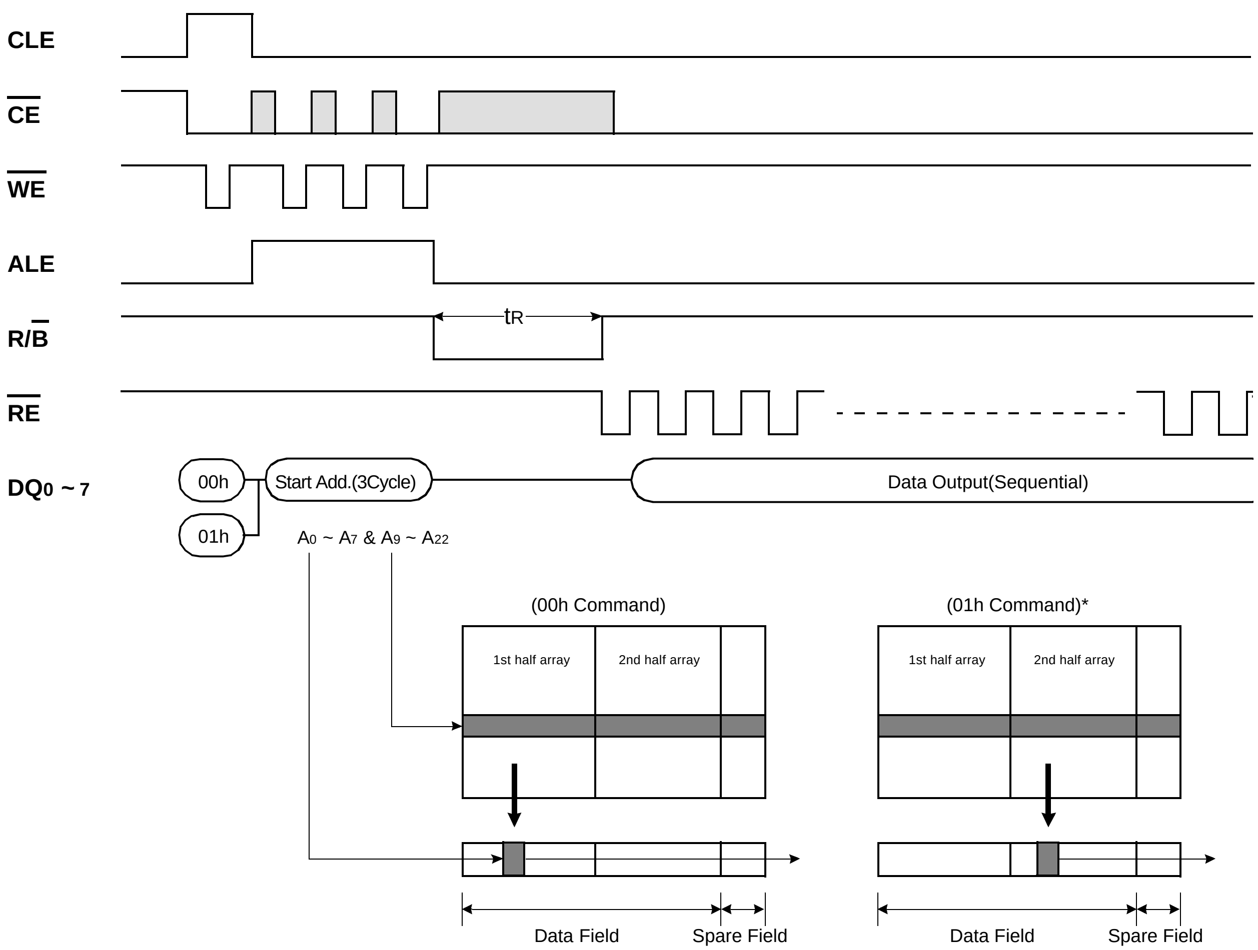
PAGE READ

Upon initial device power up, the device defaults to Read1 mode. This operation is also initiated by writing 00h to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Two types of operations are available : random read, serial page read .

The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 10µs(tR). During Read Busy, the device can go into pseudo-standy mode by taking $\overline{CE}$ to V_{IH}, which frees DQ bus and allows the CPU to access other devices. The CPU can detect the completion of this data transfer(tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing $\overline{RE}$. High to low transitions of the $\overline{RE}$ clock output the data stating from the selected column address up to the last column address.

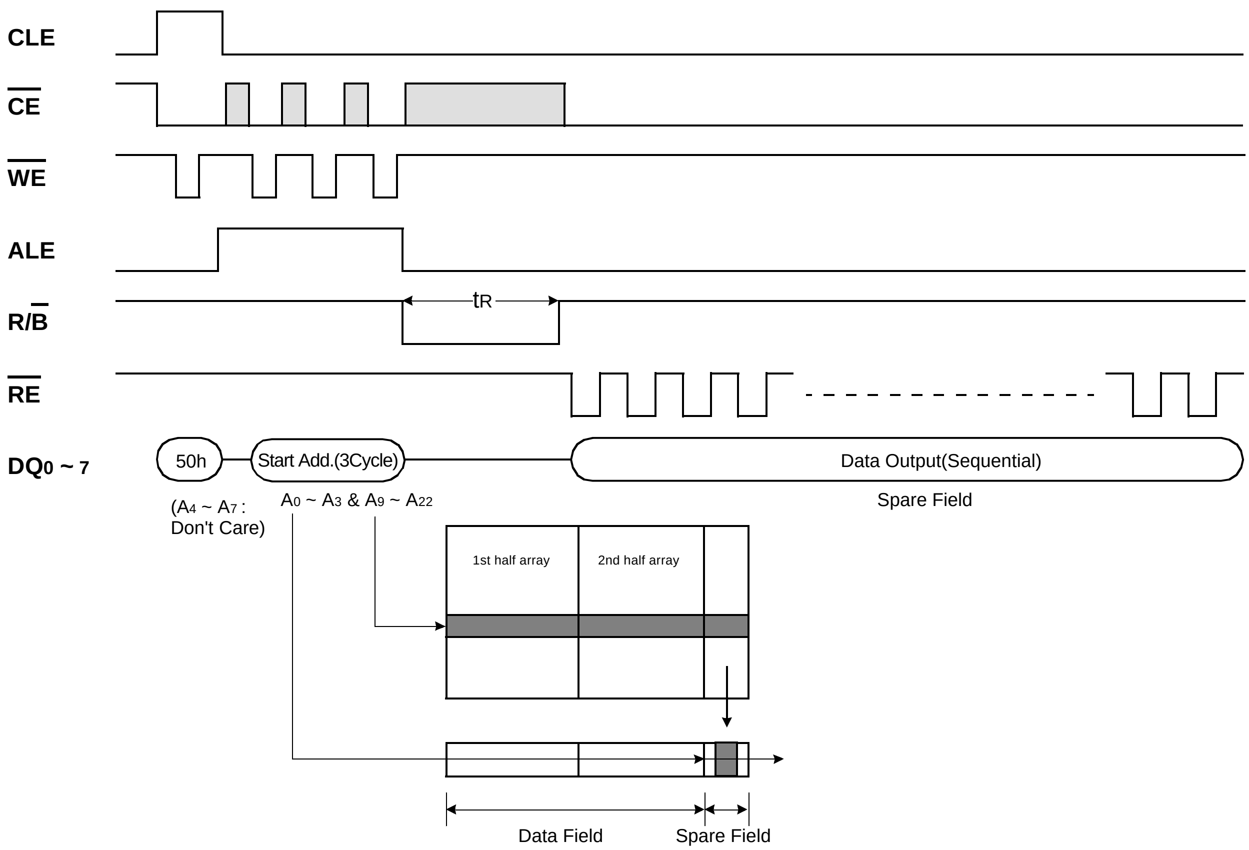
The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of bytes 512 to 527 may be selectively accessed by writing the Read2 command. Addresses A_0 to A_3 set the starting address of the spare area while addresses A_4 to A_7 are ignored. The Read1 command(00h/01h) is needed to move the pointer back to the main area. Figures 3 and 4 show typical sequence and timings for each read operation.

Figure 3. Read1 Operation



* After data access on 2nd half array by 01H command, the start pointer is automatically moved to 1st half array (00h) at next cycle.

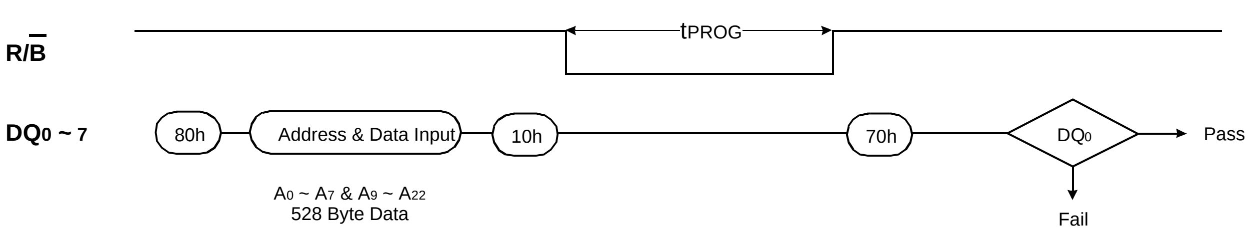
Figure 4. Read2 Operation



PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation should not exceed 2 for main array and 3 for spare array. The addressing may be done in any random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. Serial data loading can be started from 2nd half array by moving pointer. About the pointer operation, please refer to the attached technical notes.
The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the three cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded.The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state-control automatically executes the algorithms and timings necessary for program and verify, thereby freeing the CPU for other tasks. Once the program process starts, the Read Status Register command may be entered, with RE and CE low, to read the status register. The CPU can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(DQ 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(DQ 0) may be checked(Figure 5). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 5. Program & Read Status Operation



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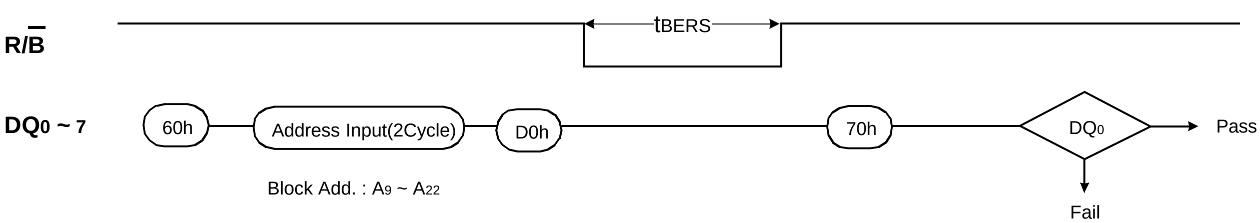
BLOCK ERASE

The Erase operation is done on a block(8K Byte) basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60h). Only address A_{13} to A_{22} is valid while A_9 to A_{12} is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write state-control handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(DQ 0) may be checked.
Figure 6 details the sequence.

Figure 6. Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the DQ pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 4 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command(00h or 50h) should be given before sequential page read cycle.

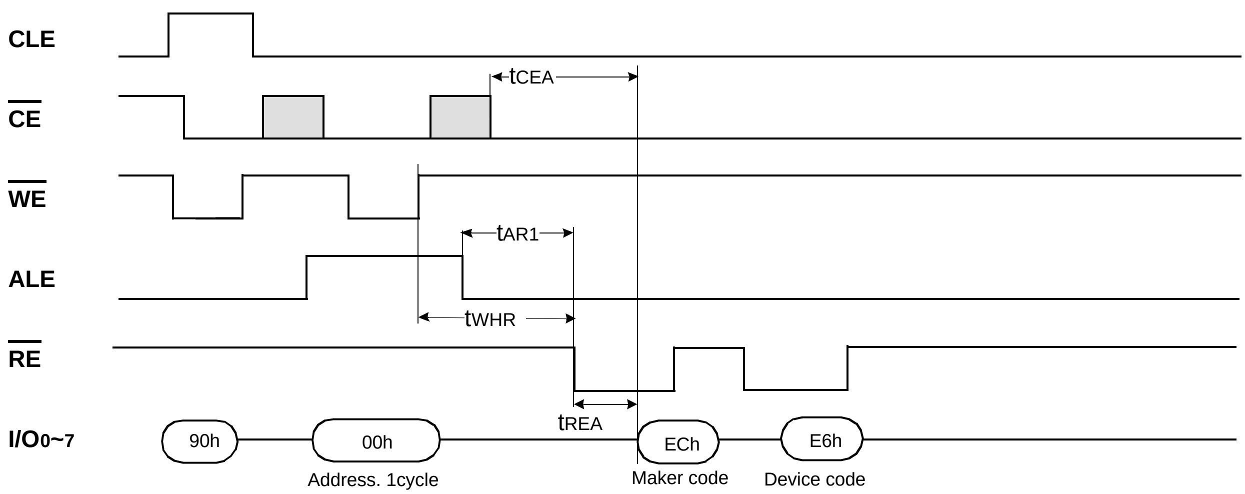
Table4. Read Status Register Definition

DQ #	Status	Definition
DQ_0	Program / Erase	"0" : Successful Program / Erase
		"1" : Error in Program / Erase
DQ_1	Reserved for Future Use	"0"
DQ_2		"0"
DQ_3		"0"
DQ_4		"0"
DQ_5		"0"
DQ_6	Device Operation	"0" : Busy "1" : Ready
DQ_7	Write Protect	"0" : Protected "1" : Not Protected

READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Two read cycles sequentially output the manufacture code(ECh), and the device code (E6h) respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 7 shows the operation sequence.

Figure 7. Read ID Operation



RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase modes, the reset operation will abort these operation. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. Internal address registers are cleared to "0"s and data registers to "1"s. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to table 5 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted to by the command register. The R/$\overline{B}$ pin transitions to low for t_{RST} after the Reset command is written. Reset command is not necessary for normal operation. Refer to Figure 8 below.

Figure 8. RESET Operation

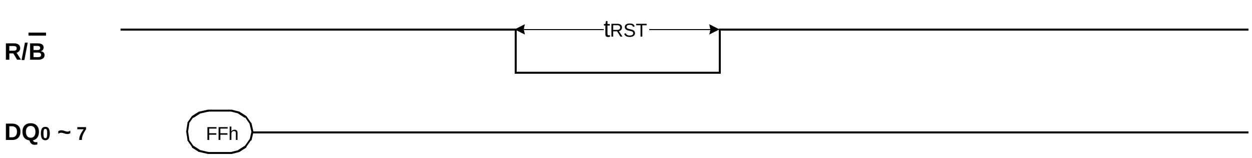
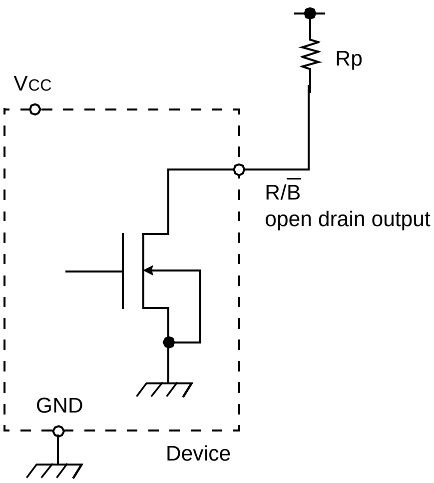


Table5. Device Status

	After Power-up	After Reset
Operation Mode	Read 1	Waiting for next command

READY/$\overline{\text{BUSY}}$

The device has a R/$\overline{\text{B}}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{\text{B}}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{\text{B}}$ outputs to be Or-tied. An appropriate pull-up resister is required for proper operation and the value may be calculated by the following equation.



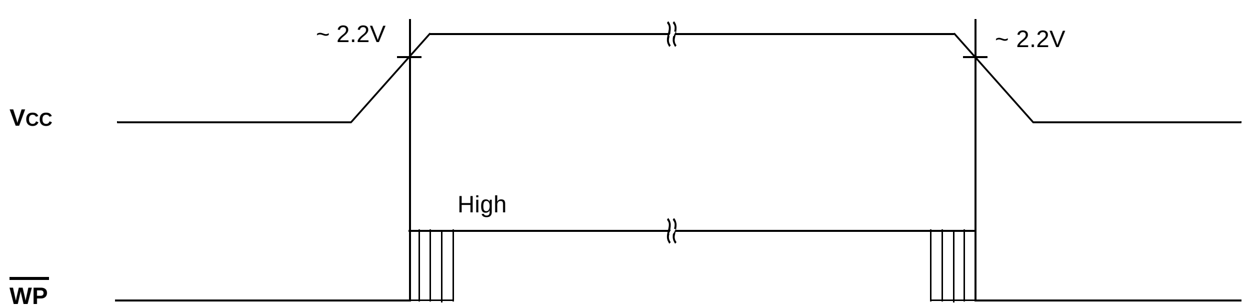
$$Rp = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \sum I_L} = \frac{2.9V}{8mA + \sum I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{\text{B}}$ pin.

DATA PROTECTION

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2.2V. $\overline{\text{WP}}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down as shown in Figure 9. The two step command sequence for program/erase provides additional software protection.

Figure 9. AC Waveforms for Power Transition



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NAND Flash Technical Notes

Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more invalid bits whose reliability is not guaranteed by Samsung. The information regarding the invalid block(s) is so called as the invalid block information. Devices with invalid block(s) have the same quality level or as devices with all valid blocks and have the same AC and DC characteristics. An invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is fully guaranteed to be a valid block, therefore you dont need to execute error correction for 1st block.

Identifying Invalid Block(s)

All device locations are erased(FFh) except locations where the invalid block(s) information is written prior to shipping. The invalid block(s) status is defined by the 6th byte in the spare area. Samsung makes sure that either the 1st or 2nd page of every invalid block has non-FFh data at the column address of 517. Since the invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the invalid block(s) based on the original invalid block information and create the invalid block table via the following suggested flow chart(Figure 10). Any intentional erasure of the original invalid block information is prohibited.

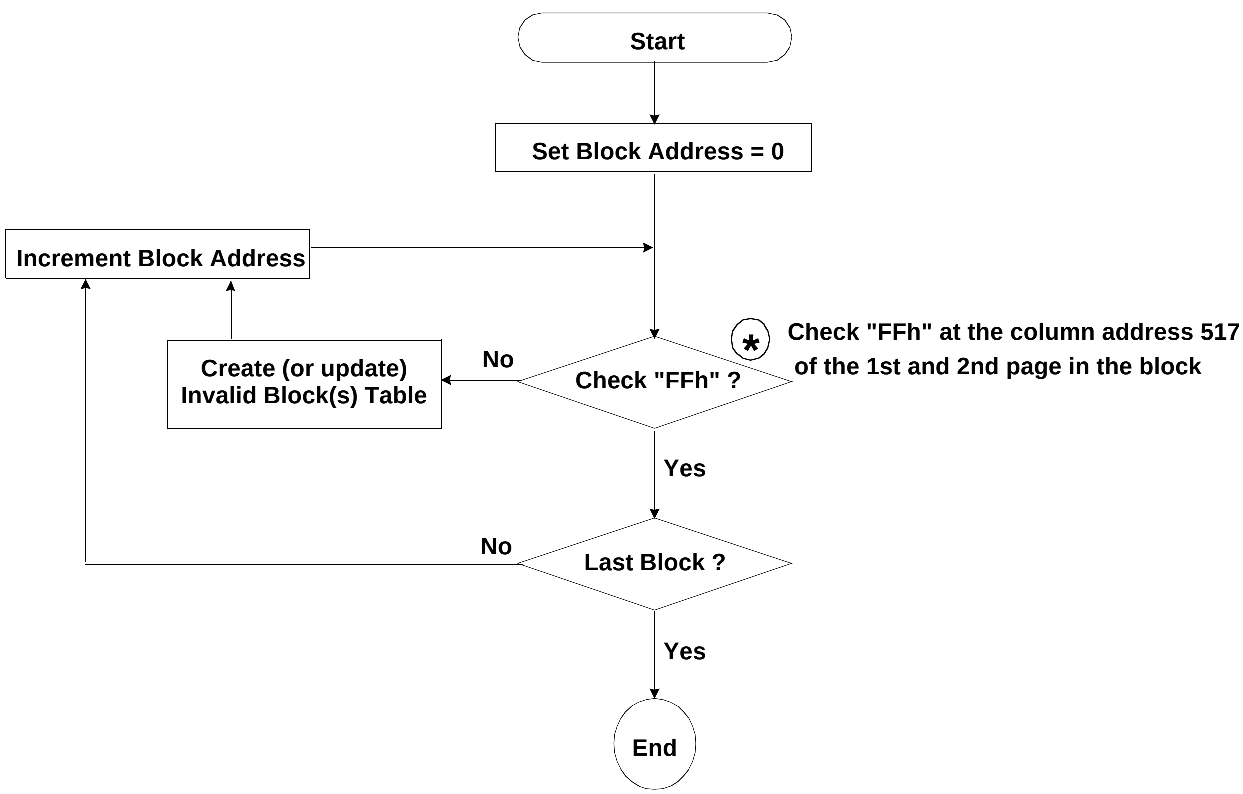


Figure 10. Flow chart to create invalid block table

NAND Flash Technical Notes

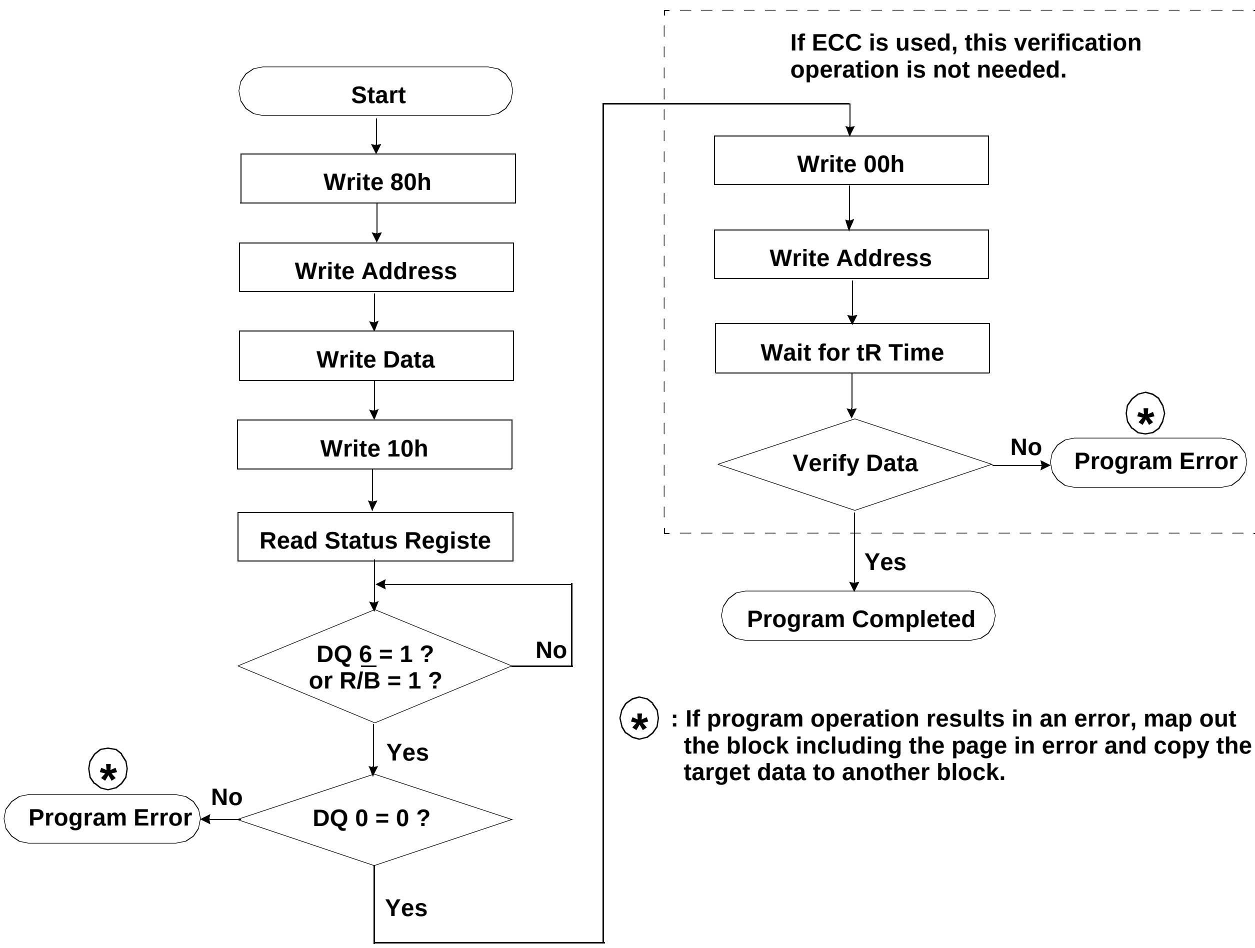
Error in write or read operation

Over its life time, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data.The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, so you can execute block replacement on a page basis with a page sized buffer. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement Read back (Verify after Program) --> Block Replacement or ECC Correction
Read	Single Bit Failure	Verify ECC -> ECC Correction

ECC : Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

Figure 11. Flash Program flow chart



NAND Flash Technical Notes

Figure 12. Flash Erase Flow Chart

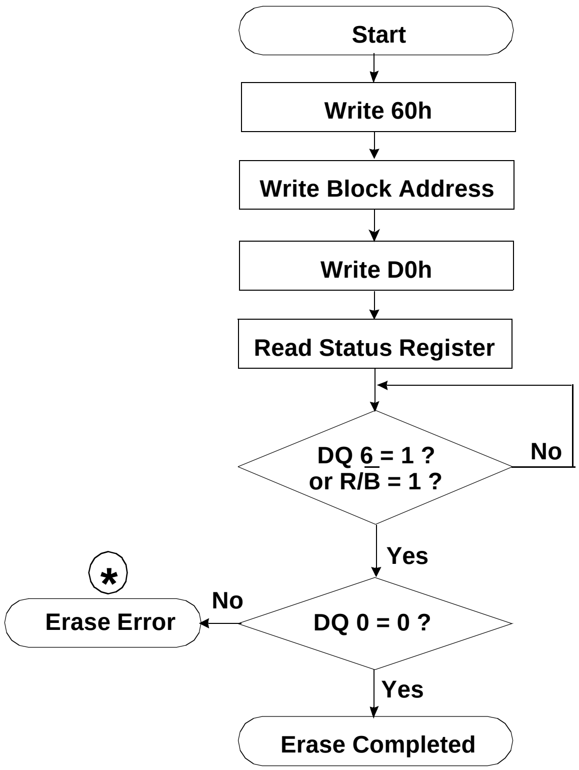
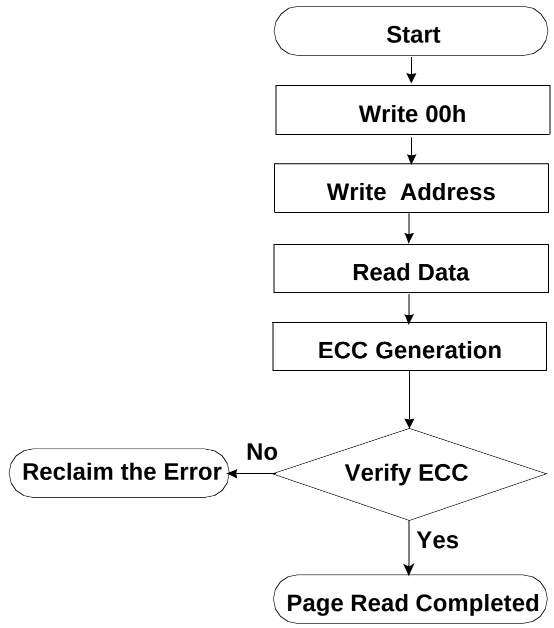
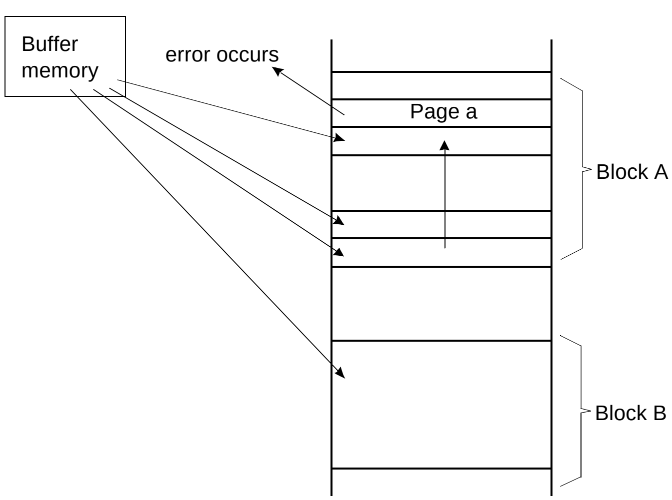


Figure 13. Flash Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

Figure 14. Flash Block Replacement



When the error happens with page "a" of Block "A", try to write the data into another Block "B" from an external buffer. Then, prevent further system access to Block "A" (by creating a "invalid block" table or other appropriate scheme.)

NAND Flash Technical Notes

Pointer Operation of NAND Flash

Samsung NAND Flash has three address pointer commands as a substitute for the two most significant column addresses. 00h' command sets the pointer to A'area(0~255byte), 01h'command sets the pointer to B'area(256~511byte), and 50h'command sets the pointer to C' area(512~527byte). With these commands, the starting column address can be set to any of a whole page(0~527byte). 00h'or 50h'is sustained until another address pointer command is inputted. 01h'command, however, is effective only for one operation. After any operation of Read, Program, Erase, Reset, Power_Up is executed once with 01h'command, the address pointer returns to A'area by itself. To program data starting from A'or C'area, 00h'or 50h'command must be inputted before 80h'command is written. A complete read operation prior to 80h'command is not necessary. To program data starting from B'area, 01h'command must be inputted right before 80h'command is written.

Table 6. Destination of the pointer

Command	Pointer position	Area
00h	0 ~ 255 byte	1st half array(A)
01h	256 ~ 511 byte	2nd half array(B)
50h	512 ~ 527 byte	spare array(C)

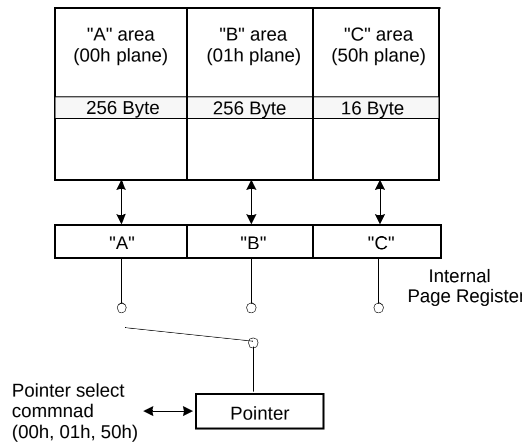
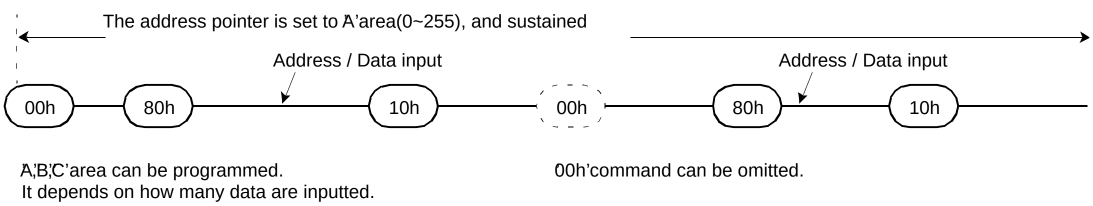
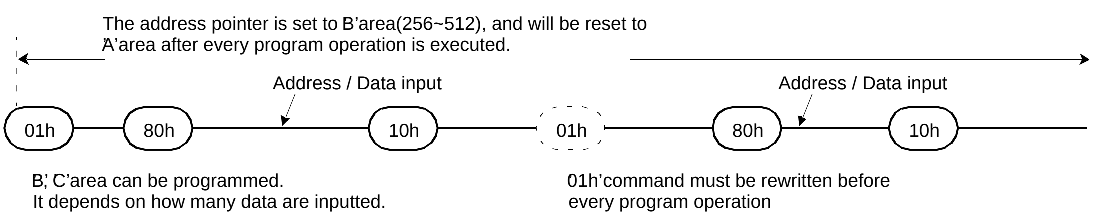


Figure 15. Block Diagram of Pointer Operation

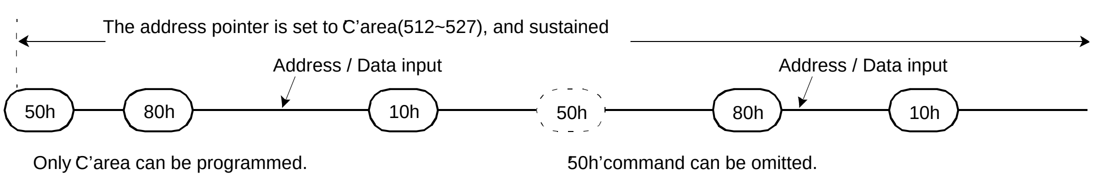
(1) Command input sequence for programming A'area



(2) Command input sequence for programming B'area



(3) Command input sequence for programming C'area



NAND Flash Technical Notes

System Interface Using $\overline{CE}$ dont-care.

For an easier system interface, $\overline{CE}$ may be inactive during data-loading or sequential data-reading as shown below. The internal 528byte page registers are utilized as seperate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of u-seconds, de-activating $\overline{CE}$ during the data-loading and reading would provide significant saving in power consumption.

Figure 16. Program Operation with $\overline{CE}$ dont-care.

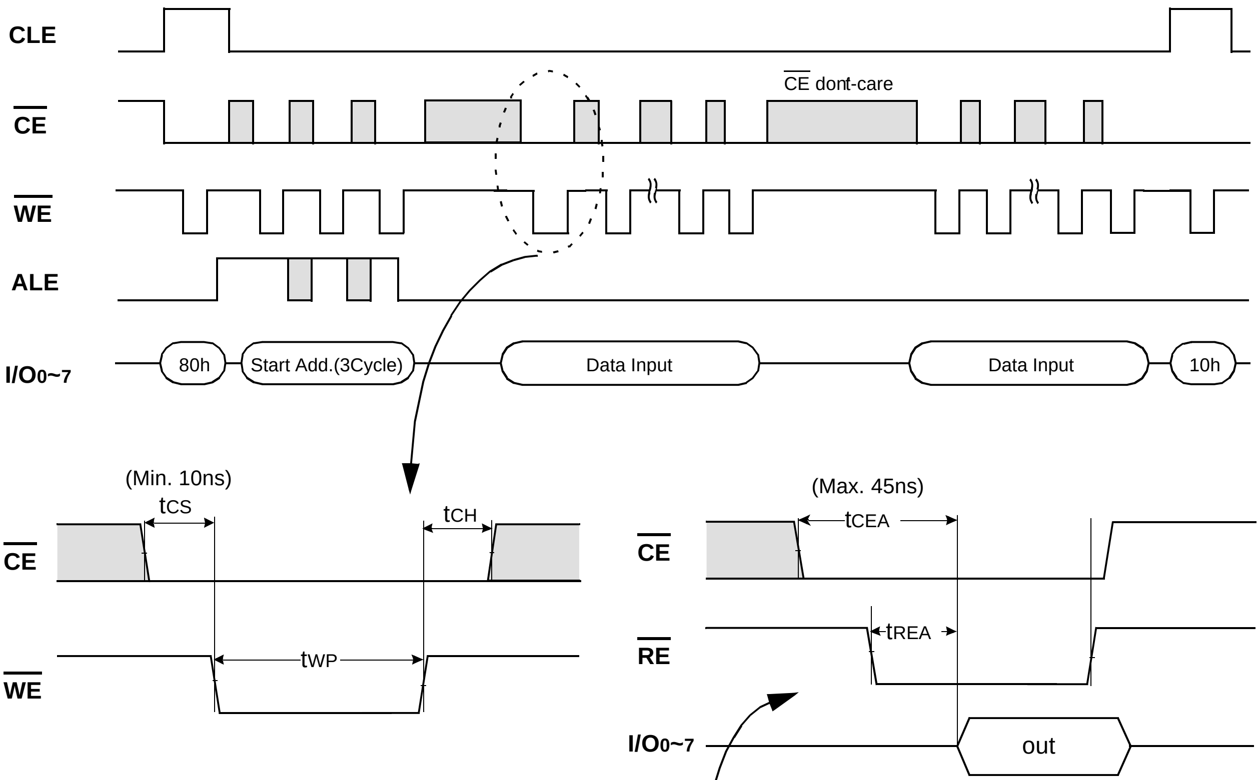
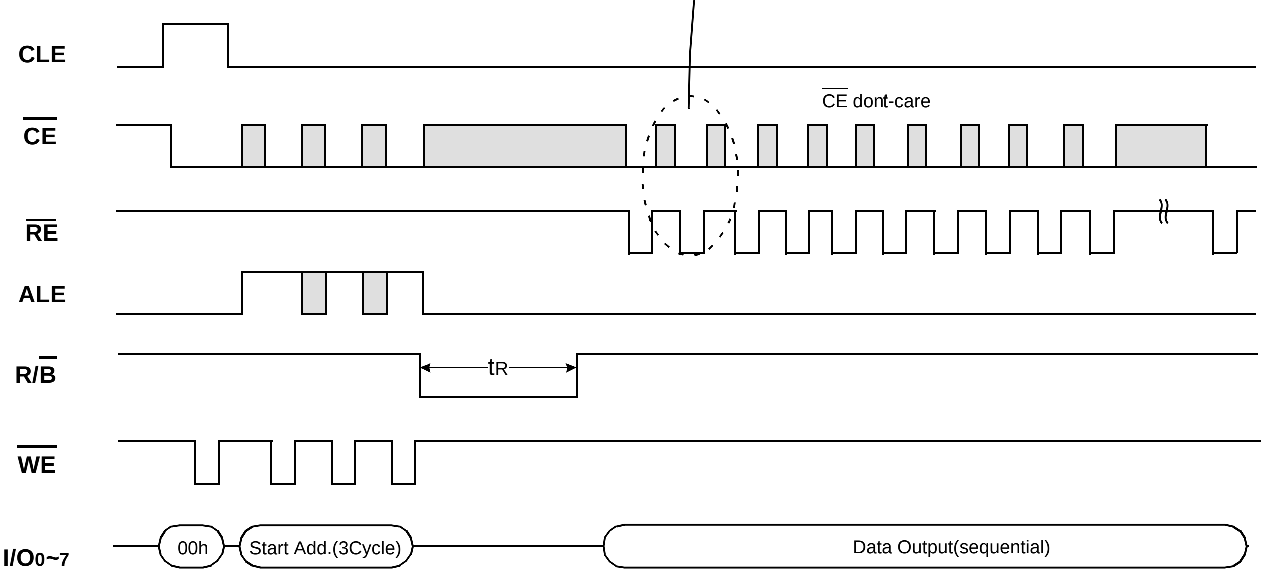


Figure 17. Read Operation with $\overline{CE}$ dont-care.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.2 to (Vccf,Vccu)+ 0.3	V
	V_{CCf}, V_{CCu}	-0.2 to 3.6V	V
	VccQf	-0.2 to 3.6V	°C
Temperature Under Bias	T_{BIAS}	-25 to + 85	
Storage Temperature	T_{STG}	-65 to + 150	°C

NOTE :
1. Minimum DC voltage is -0.2V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is V_{CCQ}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, T_A=-25 to 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CCf}, V_{CCU}	2.7	3.0	3.3	V
Supply Voltage	V_{CCQf}	2.7	3.0	3.3	V
Supply Voltage	V_{SS}	0	0	0	V

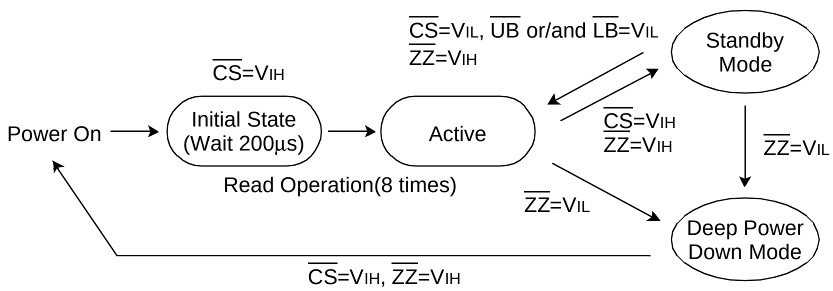
DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CCf},V_{CCU}=V_{CCf}Max.,V_{CCU}Max. V_{CCQf}=V_{CCQf}Max.,V_{IN}=V_{CCQf} or GND	-	±10	µA
Output Leakage Current	I_{LO}	V_{CCf},V_{CCU}=V_{CCf}Max.,V_{CCU}Max. V_{CCQf}=V_{CCQf}Max.,V_{IN}=V_{CCQf} or GND	-	±10	µA
Input Low Voltage Level, All inputs	V_{IL}		-0.4	0.4	V
Input High Voltage Level	V_{IH}		VccQf-0.4	VccQf+0.4	
Output Low Voltage Level	V_{OL}	Vccf=Vccf Min, Vccu=Vccu Min I_{OL} = 0.1mA	-	0.4	
Output High Voltage Level	V_{OH}	Vccf=Vccf Min, Vccu=Vccu Min. I_{OH} = -0.1mA	VccQf-0.3	-	

DC AND OPERATING CHARACTERISTICS(Continued)

Parameter		Symbol	Test Conditions	Typ	Max	Unit
Flash	Active Sequential Read Currnt	I_{CC1f}	tRC=50ns,$\overline{CEf}$=V_{IL}, I_{OUT}=0mA V_{CCf}=V_{CCf}Max,V_{CCQf}=V_{CCQf}Max	10	20	mA
	Active Program Current	I_{CC2f}	V_{CCf}=V_{CCf}Max,V_{CCQf}=V_{CCQf}Max	10	20	mA
	Active Erase Current	I_{CC3f}	V_{CCf}=V_{CCf}Max,V_{CCQf}=V_{CCQf}Max	10	20	mA
	Stand_by Current	I_{SB2f}	$\overline{CEf}$=VccQf, $\overline{WP}$=0V/V_{CCQf}	10	50	µA
UtRAM	Operating Current	I_{CC1u}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CSu}$≤0.2V, $\overline{ZZ}$≥V_{CCU}-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CCU}-0.2V	2	5	mA
		I_{CC2u}	Cycle time=Min, 100% duty, I_{IO}=0mA, $\overline{CSu}$=V_{IL}, $\overline{ZZ}$=V_{IH} , V_{IN}=V_{IL} or V_{IH}	18	25	mA
	Stand_by Current(CMOS)	I_{SB2u}	$\overline{CSu}$≥V_{CCU}-0.2V, $\overline{ZZ}$≥V_{CCU}-0.2V, Other inputs =0~V_{CCU}	120	150	µA
	Deep Power Down	I_{SBD}	$\overline{ZZ}$≤0.2V, Other input =0~V_{CCu}	5	20	µA

Standby Mode State Machines(UtRAM)



Standby Mode Characteristic(UtRAM)

Power Mode	Memory Cell Data	Standby Current(mA)	Wait Time(ms)
Standby	Valid	250	0
Deep Power Down	Invaild	20	200

CAPACITANCE (T_A = 25 °C, V_{CC} = 3.0V, f = 1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	C_{DQ}	V_{IL}=0V	-	20	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	18	pF

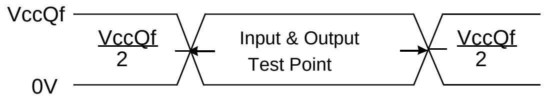
Note : Capacitance is periodically sampled and not 100% tested.

VALID BLOCK OF FLASH MEMORY(FLASH)

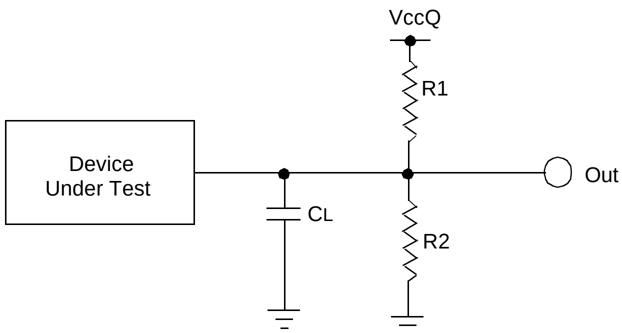
Parameter	Symbol	Min	Typ.	Max	Unit
Valid Block Number	N_{VB}	1014	1020	1024	Blocks

NOTE :
1. The Flash memory may include invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not try to access these invalid blocks for program and erase. Refer to the attached technical notes for a appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block.

Input / Output Reference Waveform



Test Configuration



Test Configuration	CL (pF)	R1(Ohm)	R2(Ohm)
2.7V - 3.3V Standard Test	50	25K	25K

Note : CL includes jig capacitance.

Flash Program/Erase Characteristics(Vcc=2.7~3.3V, TA=-25 to 85°C)

Parameter		Symbol	Min	Typ	Max	Unit
Program Time		t_{PROG}	-	300	600	µs
Number of Partial Program Cycles in the Same Page	Main Array	Nop	-	-	2	cycles
	Spare Array		-	-	3	cycles
Block Erase Time		t_{BERS}	-	2	4	ms

Flash AC Timing Characteristics for Command / Address / Data Input(Vcc=2.7~3.3V, TA=-25 to 85°C)

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	0	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
$\overline{\text{CE}}$ Setup Time	t_{CS}	0	-	ns
$\overline{\text{CE}}$ Hold Time	t_{CH}	10	-	ns
$\overline{\text{WE}}$ Pulse Width	t_{WP}	25	-	ns
ALE Setup Time	t_{ALS}	0	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data Setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	50	-	ns
$\overline{\text{WE}}$ High Hold Time	t_{WH}	15	-	ns

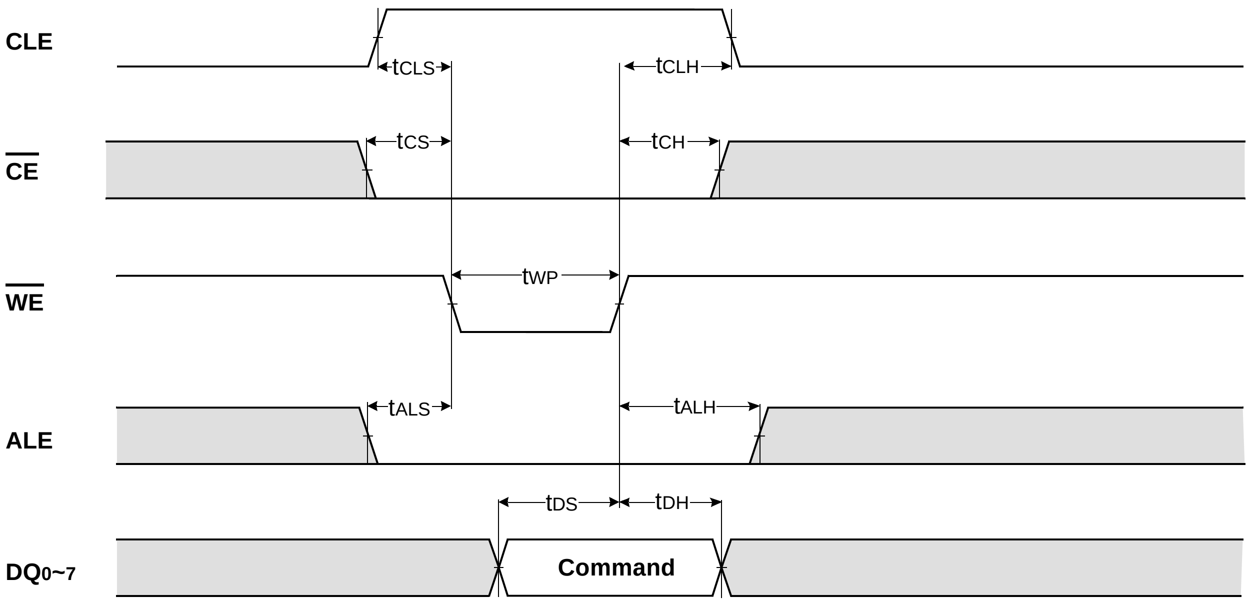
Flash AC Characteristics for Operation(Vcc=2.7~3.3V, TA=-25 to 85°C)

Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	t_R	-	10	µs
ALE to $\overline{\text{RE}}$ Delay(ID read)	t_{AR1}	20	-	ns
ALE to $\overline{\text{RE}}$ Delay(Read cycle)	t_{AR2}	50	-	ns
$\overline{\text{CE}}$ Access Time	t_{CEA}	-	45	ns
Ready to $\overline{\text{RE}}$ Low	t_{RR}	20	-	ns
$\overline{\text{RE}}$ Pulse Width	t_{RP}	30	-	ns
$\overline{\text{WE}}$ High to Busy	t_{WB}	-	100	ns
Read Cycle Time	t_{RC}	50	-	ns
$\overline{\text{RE}}$ Access Time	t_{REA}	-	35	ns
$\overline{\text{RE}}$ High to Output Hi-Z	t_{RHZ}	15	30	ns
$\overline{\text{CE}}$ High to Output Hi-Z	t_{CHZ}	-	20	ns
$\overline{\text{RE}}$ High Hold Time	t_{REH}	15	-	ns
Output Hi-Z to $\overline{\text{RE}}$ Low	t_{IR}	0	-	ns
$\overline{\text{WE}}$ High to $\overline{\text{RE}}$ Low	t_{WHR}	60	-	ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	5/10/500(1)	µs

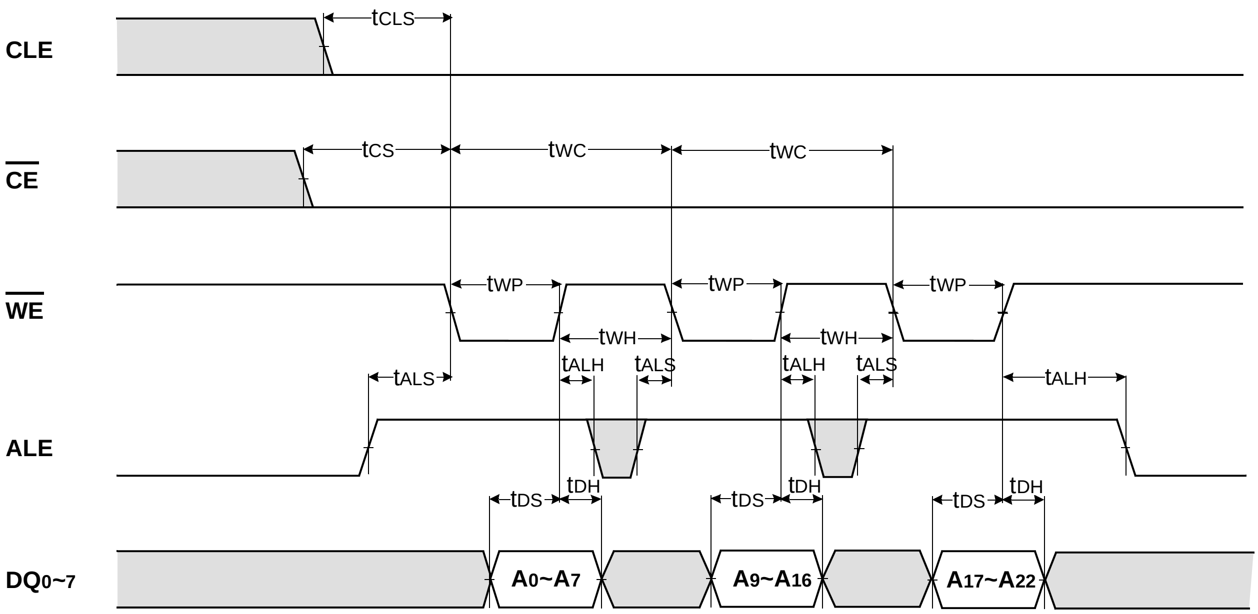
NOTE :

1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5us

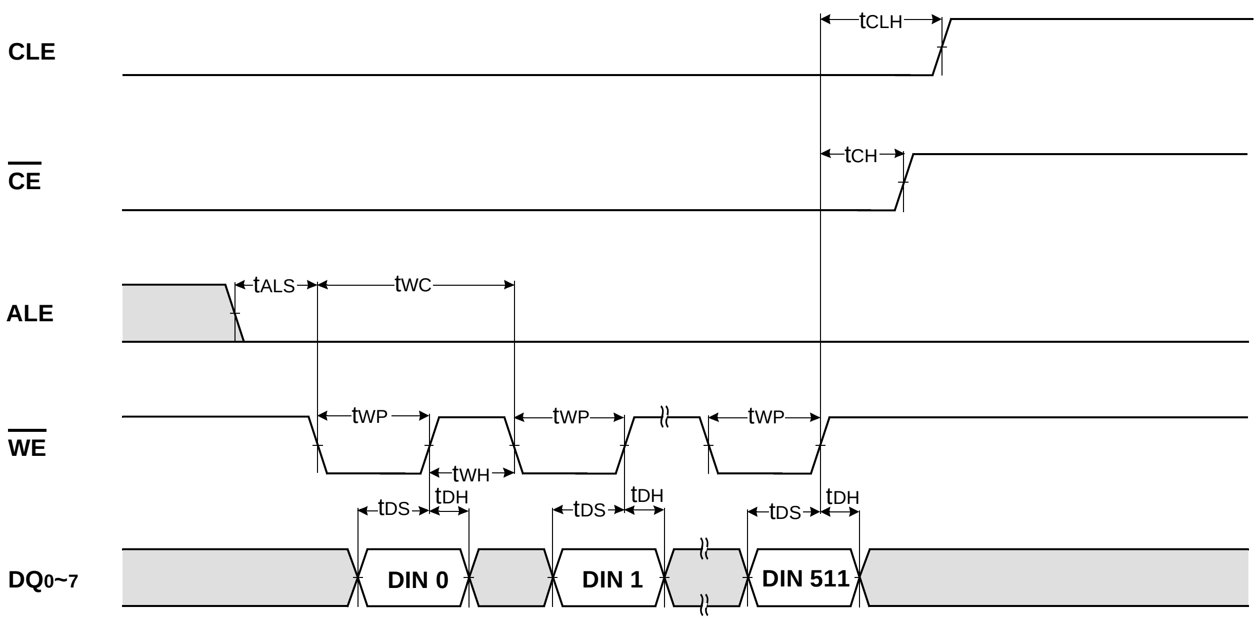
* Flash Command Latch Cycle



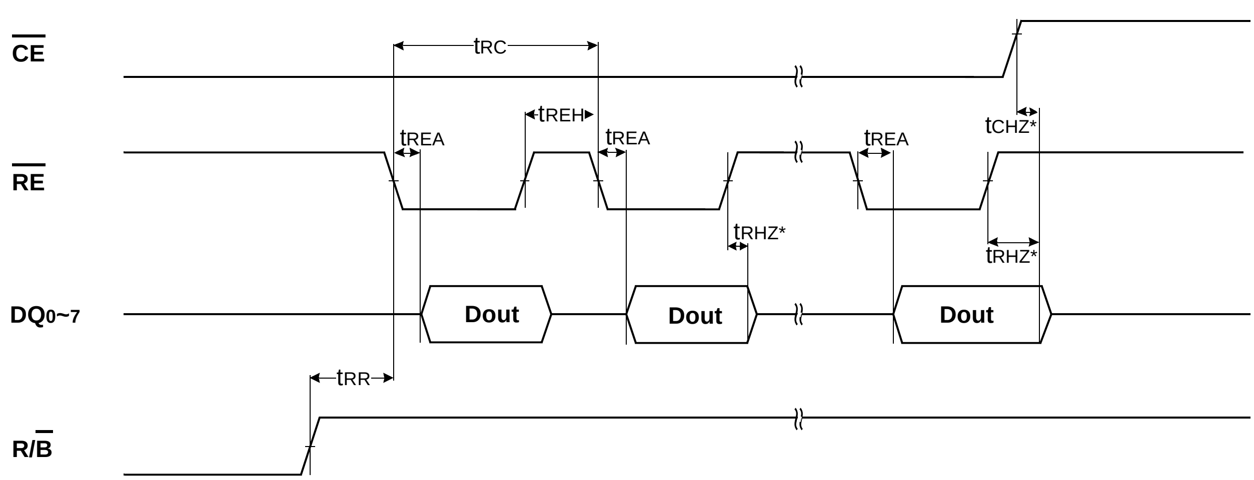
* Flash Address Latch Cycle



* Flash Input Data Latch Cycle

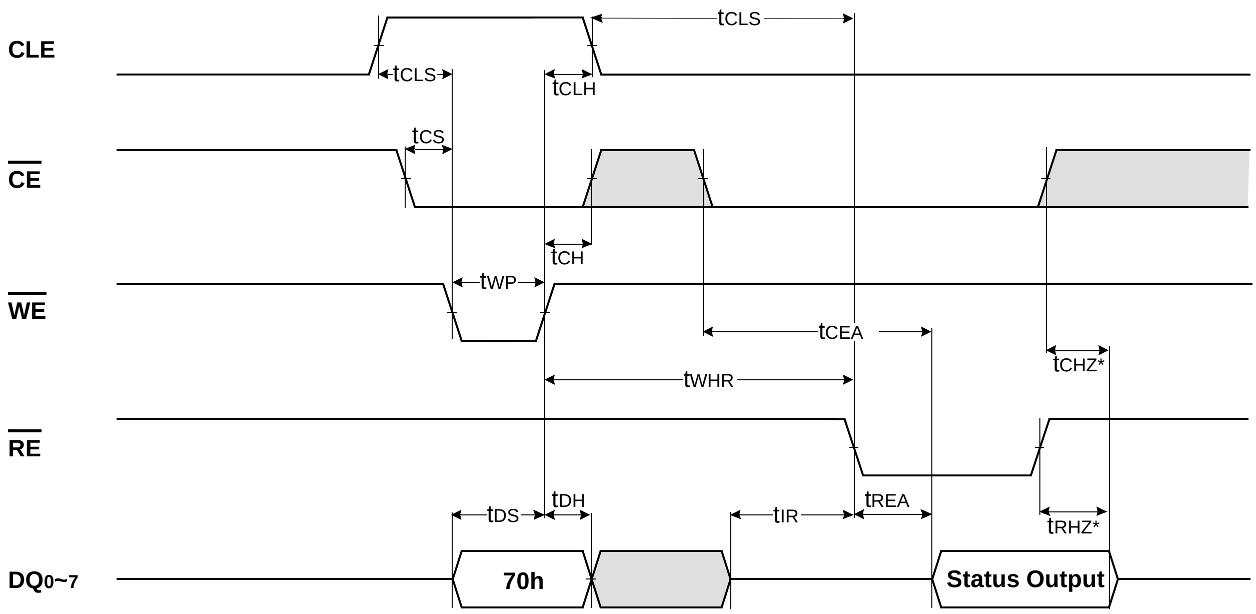


* Flash Sequential Out Cycle after Read(CLE=L, WE=H, ALE=L)

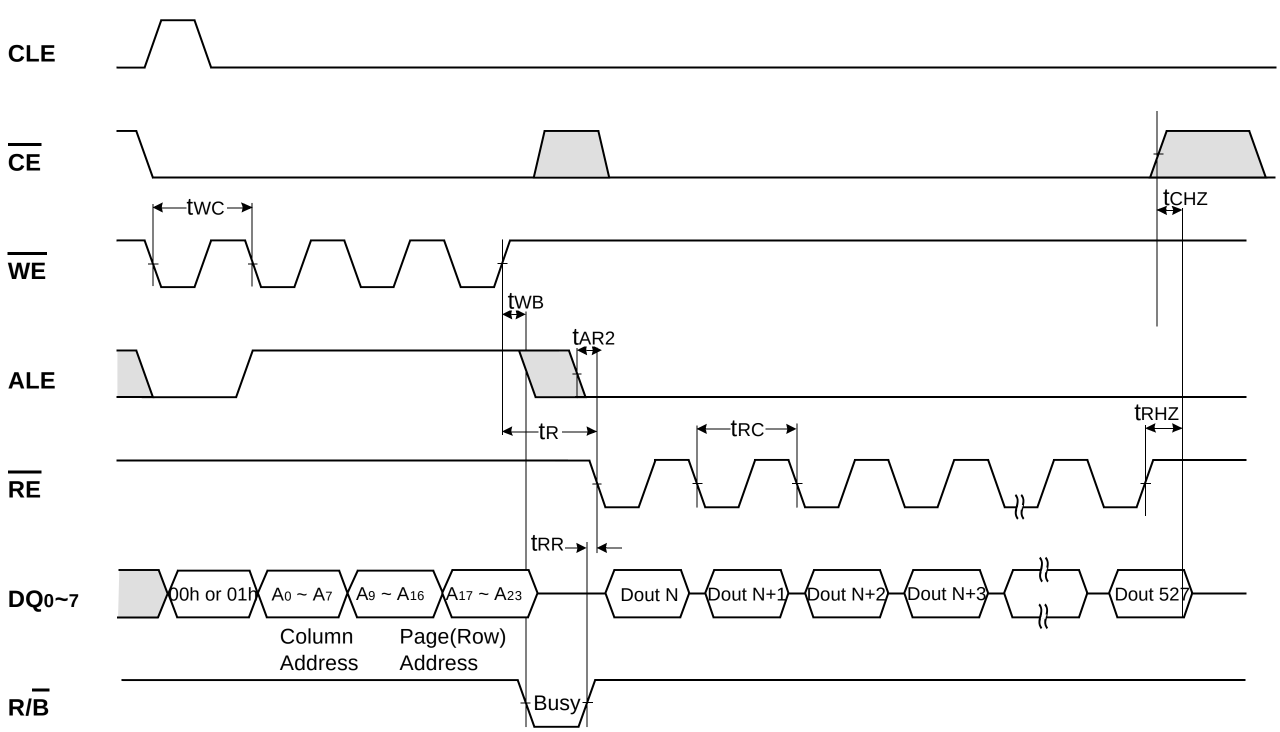


NOTES : Transition is measured ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

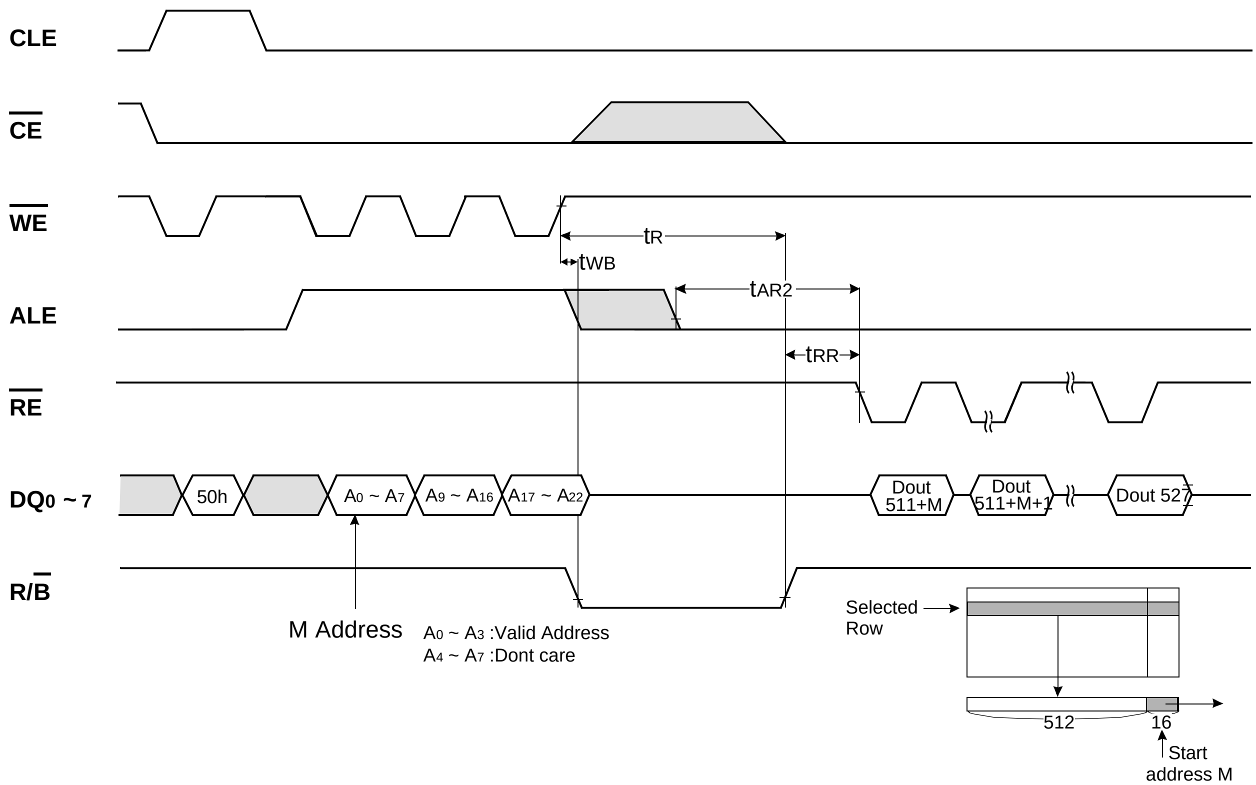
* Flash Status Read Cycle



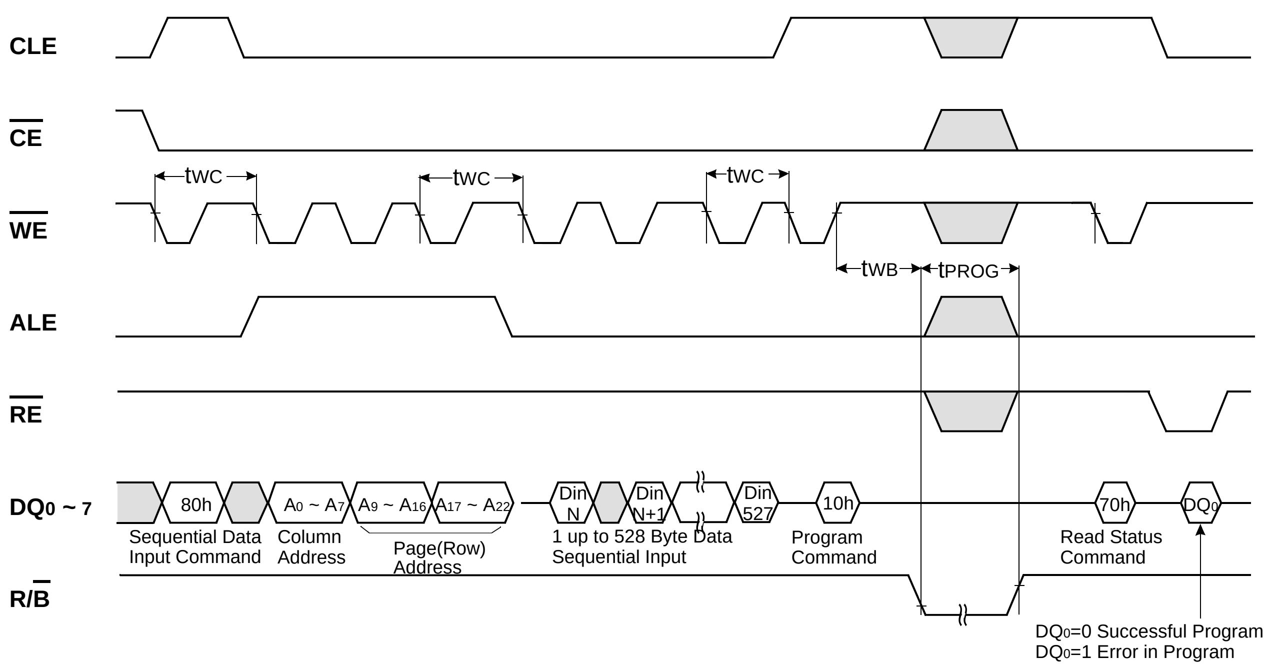
FLASH READ1 OPERATION(READ ONE PAGE)



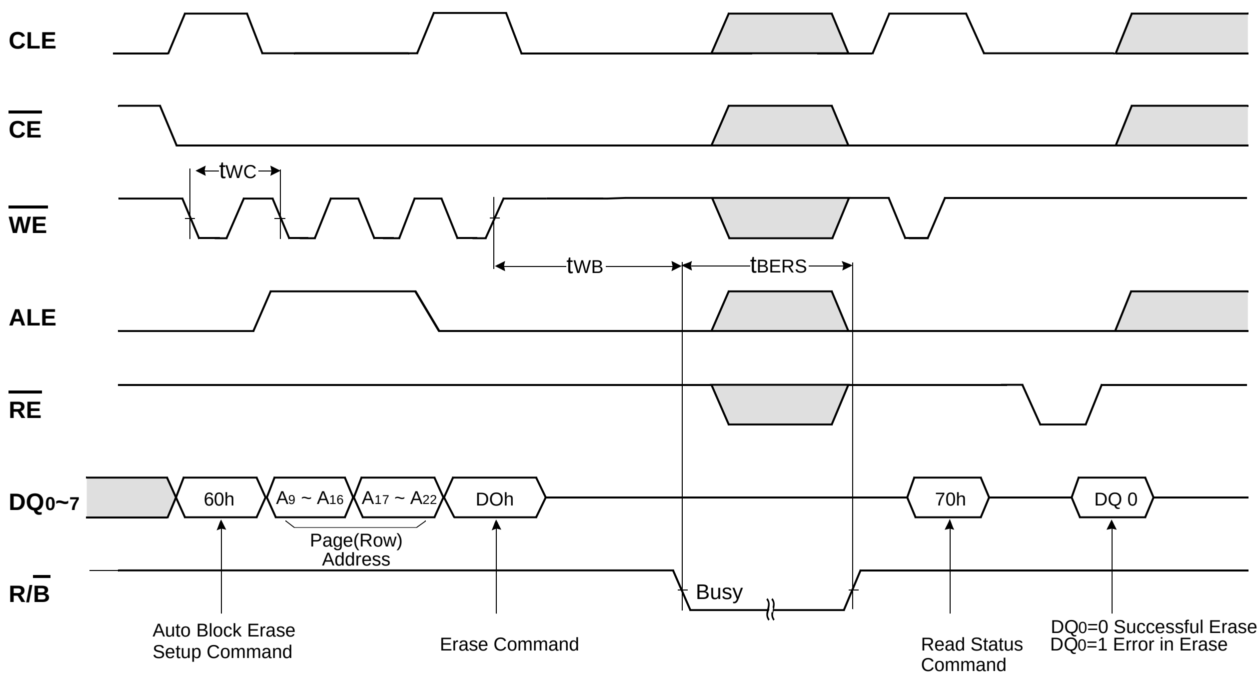
FLASH READ2 OPERATION(READ ONE PAGE)



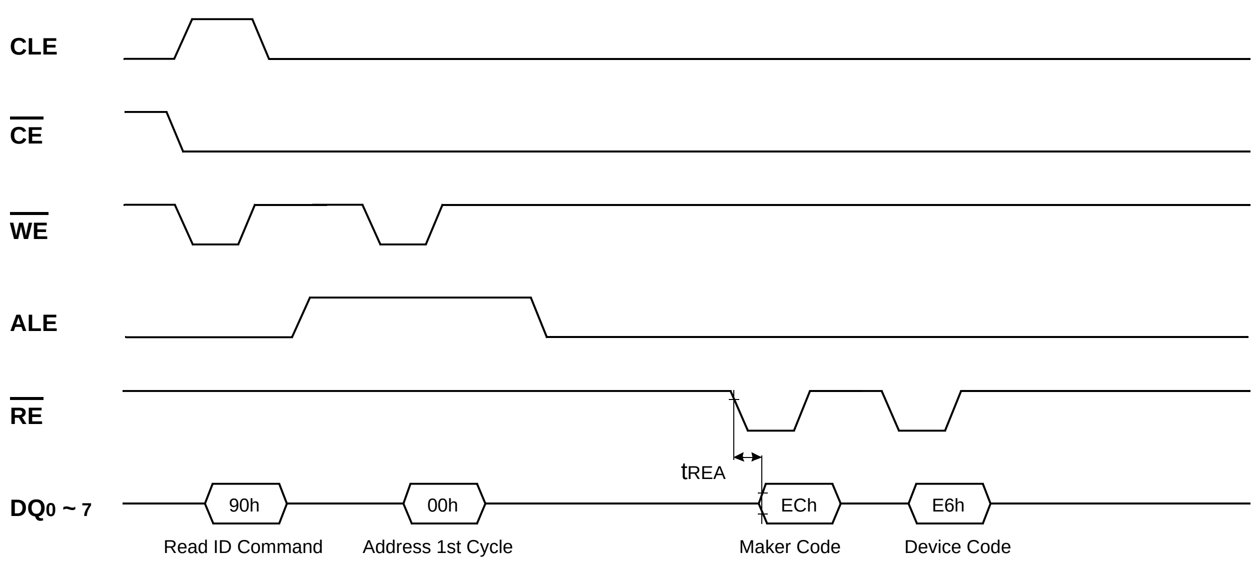
FLASH PAGE PROGRAM OPERATION



FLASH BLOCK ERASE OPERATION(ERASE ONE BLOCK)



FLASH MANUFACTURE & DEVICE ID READ OPERATION



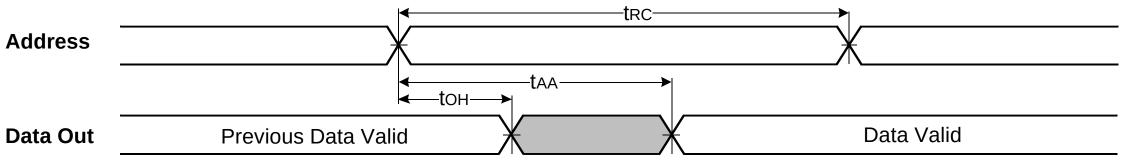
UtRAM AC CHARACTERISTICS(Vcc=2.7~3.3V, TA=-25 to 85°C)

Parameter List		Symbol	Speed Bins				Units
			100ns[1)]		100ns[2)]		
			Min	Max	Min	Max	
Read	Read Cycle Time	t_{RC}	100	-	100	-	ns
	Address Access Time	t_{AA}	-	100	-	100	ns
	Chip Select to Output	t_{CO}	-	100	-	100	ns
	Output Enable to Valid Output	t_{OE}	-	50	-	50	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	100	-	100	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	10	-	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	25	0	25	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	25	0	25	ns
	Output Disable to High-Z Output	t_{OHZ}	0	25	0	25	ns
	Output Hold from Address Change	t_{OH}	5	-	5	-	ns
Write	Write Cycle Time	t_{WC}	100	-	110	-	ns
	Chip Select to End of Write	t_{CW}	80	-	100	-	ns
	Address Set-up Time	t_{AS}	0	-	0	-	ns
	Address Valid to End of Write	t_{AW}	80	-	100	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	80	-	100	-	ns
	Write Pulse Width	t_{WP}	70	-	100	-	ns
	Write Recovery Time	t_{WR}	0	-	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	30	0	30	ns
	Data to Write Time Overlap	t_{DW}	40	-	40	-	ns
	Data Hold from Write Time	t_{DH}	0	-	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	5	-	ns

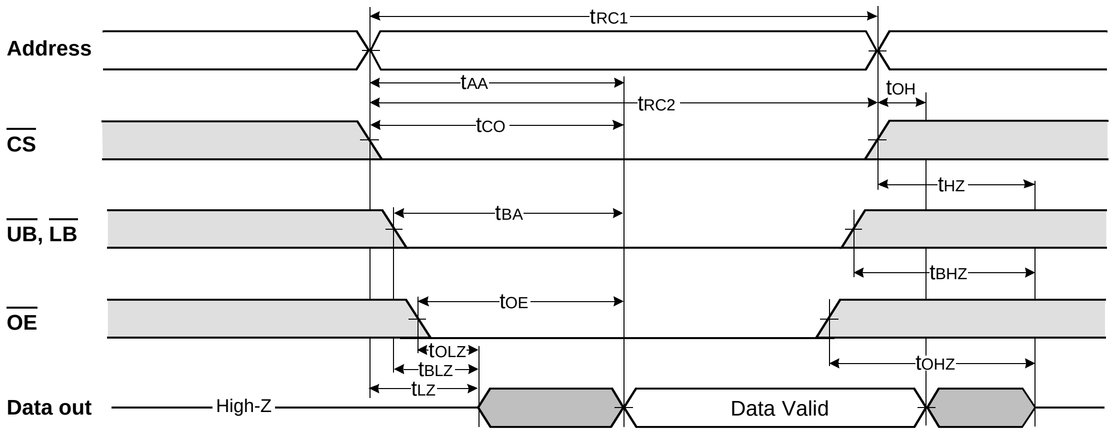
1. The characteristics which is restricted for continuous wirte operation over 20 times, please refer to technical note.
2. The characteristics for continuous wirte operation.

UtRAM TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{ZZ}$=$\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



TIMING WAVEFORM OF READ CYCLE(2)($\overline{ZZ}$=$\overline{WE}$=V_{IH})

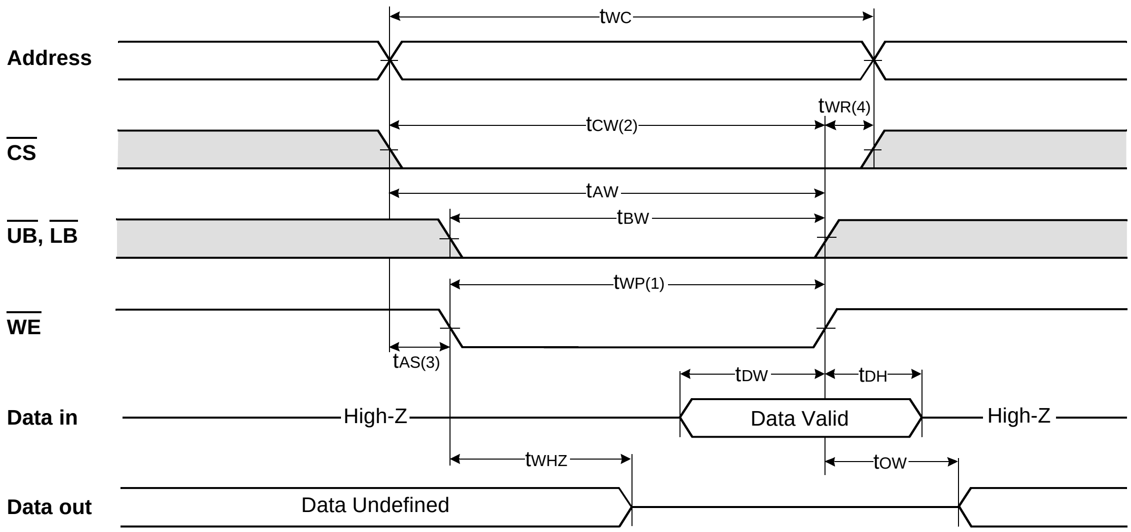


(READ CYCLE)

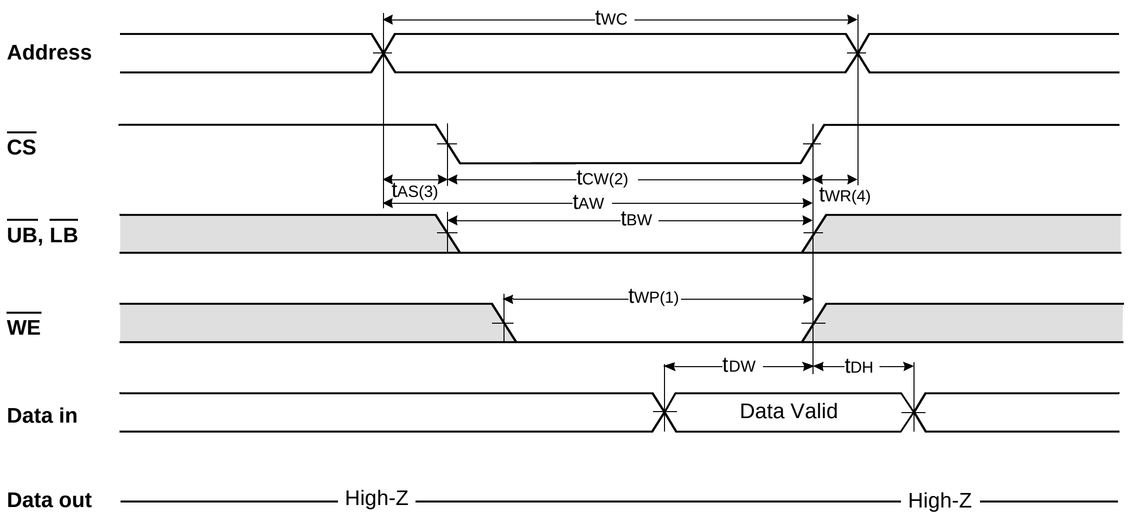
1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
3. The minimum read cycle(t_{RC}) is determined later one of the t_{RC1} and t_{RC2}.

SAMSUNG ELECTRONICS

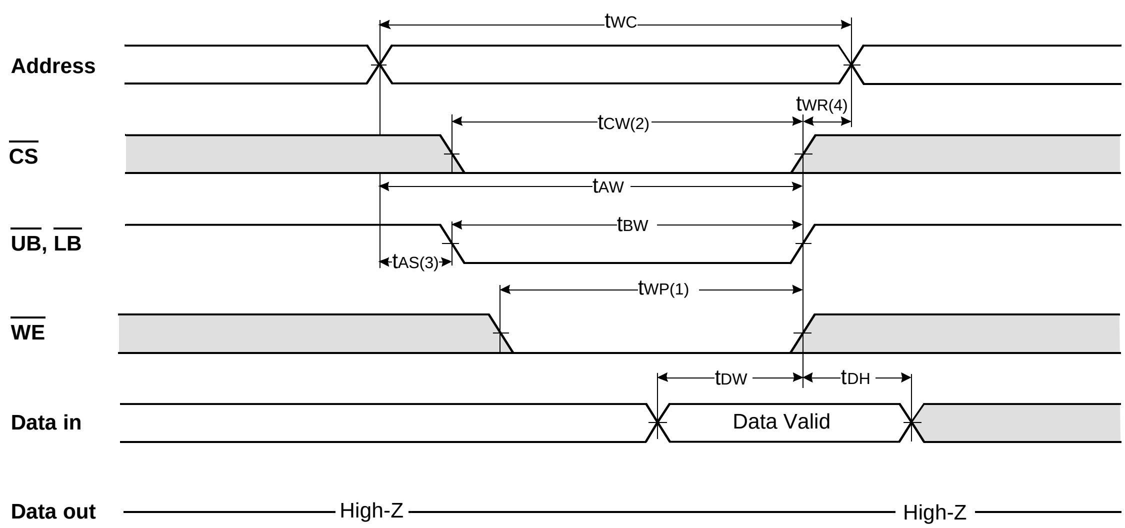
TIMING WAVEFORM OF WRITE CYCLE(1)(WE Controlled, ZZ=VIH)



TIMING WAVEFORM OF WRITE CYCLE(2)(CS Controlled, ZZ=VIH)



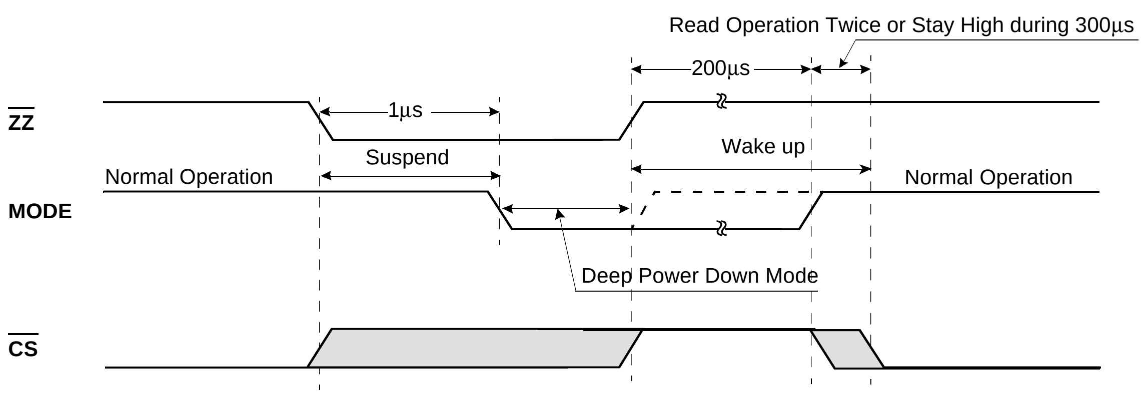
TIMING WAVEFORM OF WRITE CYCLE(3)(UB, LB Controlled, ZZ=VIH)



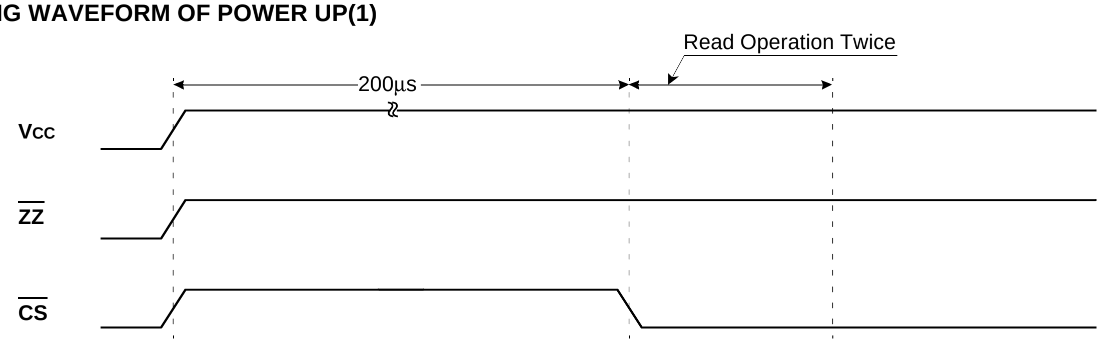
(WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low CS and low WE. A write begins when CS goes low and WE goes low with asserting UB or LB for single byte operation or simultaneously asserting UB and LB for double byte operation. A write ends at the earliest transition when CS goes high and WE goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the CS going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CS or WE going high.

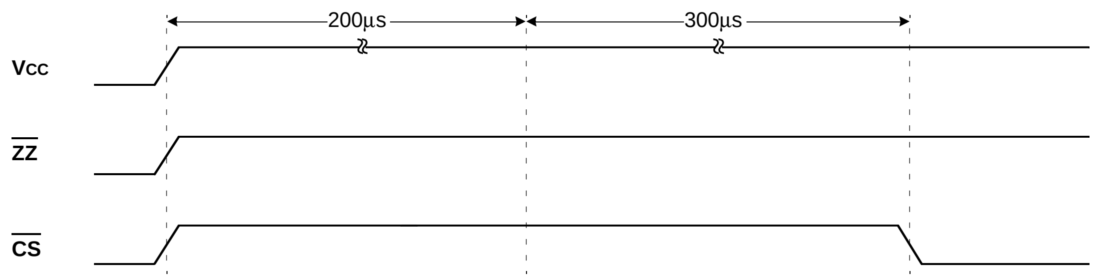
TIMING WAVEFORM OF DEEP POWER DOWN MODE



TIMING WAVEFORM OF POWER UP(1)



TIMING WAVEFORM OF POWER UP(2)(No Dummy Cycle)



INTRODUCTION

Ut*RAM is based on single-transistor DRAM cells. As with any other DRAM, the data in these cells must be periodically refreshed to prevent data loss. What makes the Ut*RAM unique is that it offers a true SRAM style interface that hides all refresh operations from the memory controller.

START WITH A DRAM TECHNOLOGY

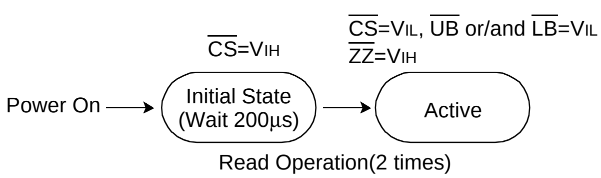
The key to the Ut*RAM is its high speed and low power. This speed comes from the use of many small blocks, often just 32Kbits each, to create Ut*RAM arrays. The small blocks have short word lines with little capacitance, eliminating a major source of operating current in conventional DRAM blocks.

Each independent macro-cell on a Ut*RAM device consists of a number of these blocks. Each chip has one or more macro.

The address decoding logic is also fast. Ut*RAM perform a complete read operation in every tRC, but Ut*RAM needs power up sequence like a DRAM.

Power Up Sequence and Diagram

1. Apply power.
2. Maintain stable power for a minium 200µs with $\overline{CS}$=high.
3. Issue read operation at least 2 times.



DESIGN ACHIEVES SRAM SPECIFIC OPERATIONS

The Ut*RAM design works just like an SRAM, with no wait states or other overhead for precharging or refreshing its internal DRAM cells. SAMSUNG Electronics(SAMSUNG) hides these operations with advanced design. Precharging takes place during every access, overlapped with the end of the cycle and the decoding portion of the next cycle.

Hiding refresh is more difficult, Every row in every block must be refreshed at least once during the refresh interval to prevent data loss. SAMSUNG provides a internal refresh controller for devices. When all accesses during a refresh interval are directed to one macro-cell, as can happen in signal processing applications, a more sophisticated approach is required to hide refresh. The pseudo SRAM, sometimes used on these applications, which is required a memory controller that can hold off accesses when a refresh operation is needed. SAMSUNG unique qualitative advantage over these parts(in addition to quantitative improvements in access speed and power consumption) is that the Ut*RAM never needs to hold off accesses, and indeed it has no hold off signal. The circuitry that gives SAMSUNG this advantage is fairly simple but has not previously been disclosed.

AVOID TIMING

Following figures are show you a abonormal timing which is not supported on Ut*RAM and their solution.

At read operation, if your system have a timing which sustain invalid states over 4us at read mode like Figure 1. There are some guide line for proper operation of Ut*RAM.

When your system have multiple invalid address signal shorter than tRC on the timing which showed in Figure 1, Ut*RAM need a normal read timing during that cycle(Figure 2) or toggle the $\overline{CS}$ to high'about tRC(Figure 3).

Figure 1.

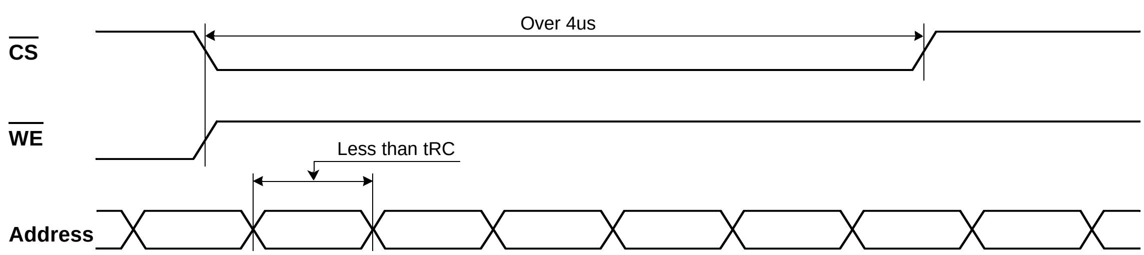


Figure 2.

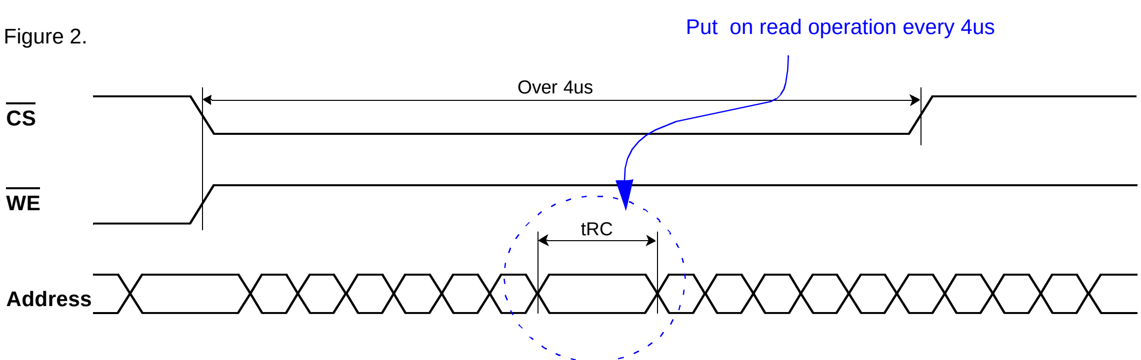
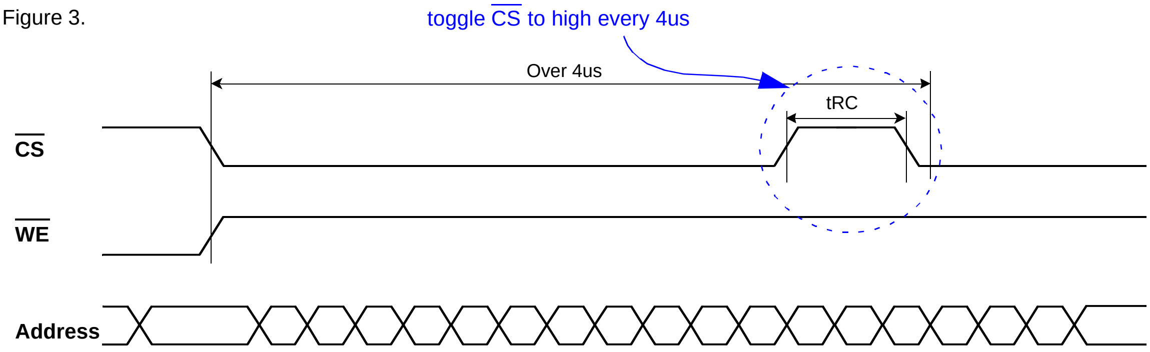


Figure 3.



Write operation have similar restricted operation with Read. If your system have a timing which sustain invalid states over 4us at write mode and system have continuous write signal with Min. tWC over 4us like Figure 4.

You must put read timing on the cycle(Figure 5) or toggle the CS to high about tRC(Figure 6).

Figure 4.

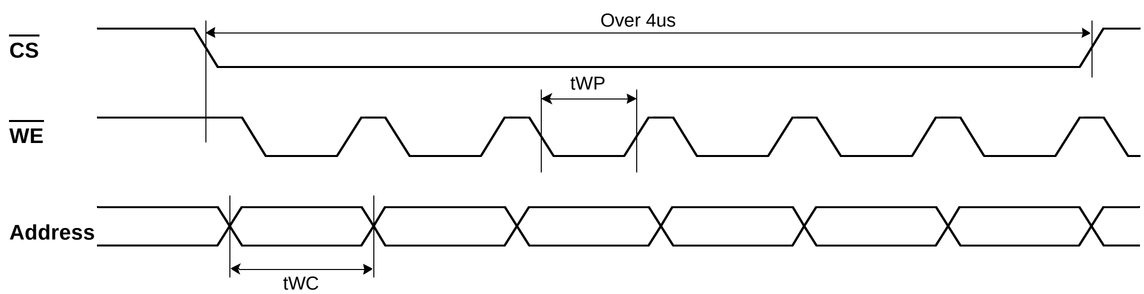


Figure 5.

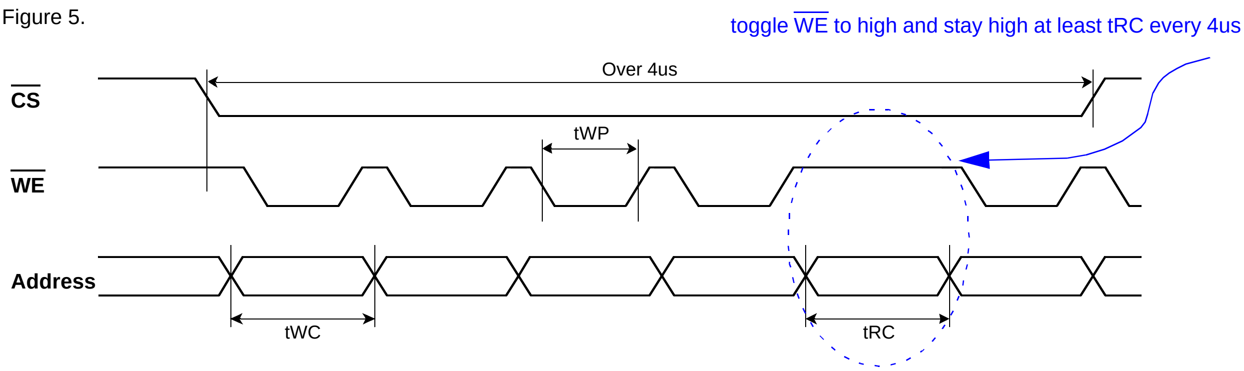
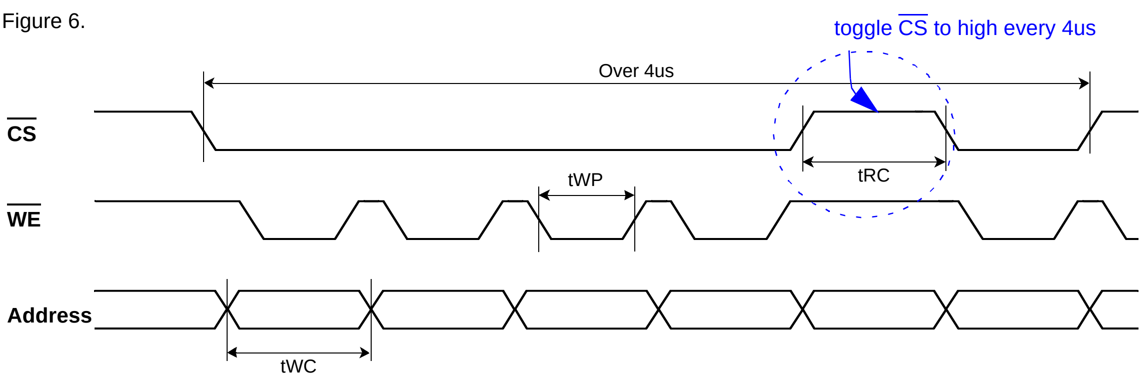


Figure 6.



PACKAGE DIMENSION

69-Ball Tape Ball Grid Array Package (measured in millimeters)