64-Channel Serial To Parallel Converter With P-Channel Open Drain Outputs

Ordering Information

Device	Package Options	
	80-Lead Quad Plastic Gullwing	Die
HV4937	HV4937PG	HV4937X

Features

- HVCMOS® Technology
- Output voltages up to -375V
- Source current minimum 0.25mA
- Shift register speed 6 MHz
- Latched outputs
- CMOS compatible inputs
- Forward and reverse shifting options

General Description

Not recommended for new designs.

The HV49 is a low voltage serial to high voltage parallel converter with open drain outputs. It has been designed especially for use as a driver for electrostatic printers.

This device consists of a 64-bit shift register, 64 latches, a latch enable ($\overline{LE}$), and an output enable (OE). Data is shifted through the shift register on the high to low transition of the clock. When the DIR pin is set high, the HV49 shifts in the counterclockwise direction when viewed from the top of the package. When the DIR pin is set low, the HV49 shifts in the clockwise direction. A serial data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register. Operation of the shift register is not affected by the $\overline{LE}$ or the OE inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ input is high. The data in the latch is stored when $\overline{LE}$ is low.

12

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}	+0.5V to -9V
Supply voltage, V_{PP}	+0.5V to -400V
Logic input levels	+0.5V to V_{DD} -0.5V
Ground current	0.75A
Continuous total power dissipation[2]	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to +150°C

Notes:
1. All voltages are referenced to V_{SS}.
2. For operation above 25°C ambient derate linearly by 20mW/°C up to 85°C.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				-15	mA	f_{CLK} = 6MHz, f_{DATA} = 3MHz $\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				-250	µA	All V_{IN} = 0V
$I_{O(OFF)}$	Off State Output Current at 25°C, per Switch				-100	nA	Output high, and at -375V
I_{IH}	High-Level Logic Input Current				-10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current				+10	µA	V_I = 0V
V_{OH}	High-Level Data Out				V_{DD} +1	V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}	-10			V	IHV_{OUT} = -0.25mA
		Data Out	-1			V	ID_{OUT} = 100µA
V_{OC}	HV_{OUT} Clamp Voltage				-3.0	V	I_{OL} = 1mA
C_{HVO}	Output Capacitance per Channel				3	pF	V_{DS} = 100V

AC Characteristics (For V_{DD} = -5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			6	MHz	
t_W	Clock Width High or Low	83			ns	
t_{SU}	Data Setup Time Before Clock Falls	35			ns	
t_H	Data Hold Time After Clock Falls	15			ns	
t_{WLE}	Width of Latch Enable Pulse	83			ns	
t_{DLE}	$\overline{LE}$ Delay Time After Falling Edge of Clock	35			ns	
t_{SLE}	$\overline{LE}$ Setup Time Before Falling Edge of Clock	40			ns	
t_{DHL}	Clock Delay Time Data High to Low			160	ns	
t_{DLH}	Clock Delay Time Data Low to High			160	ns	

Recommended Operating Conditions

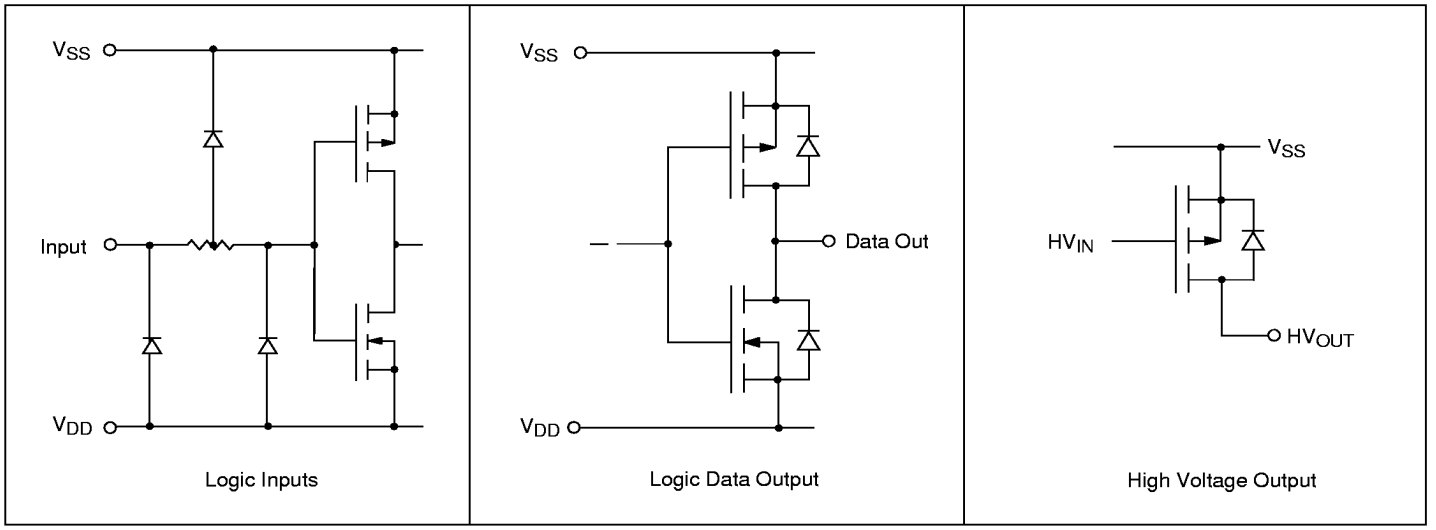
Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	-4.5	-5.0	-5.5	V
HV_{OUT}	High voltage output	+0.3		-375	V
V_{IH}	High-level input voltage	-3.5		V_{DD}	V
V_{IL}	Low-level input voltage	0		-0.8	V
T_A	Operating free-air temperature	-40		+85	°C

Notes:
All voltages are referenced to V_{SS}.
Power-up sequence should be the following:

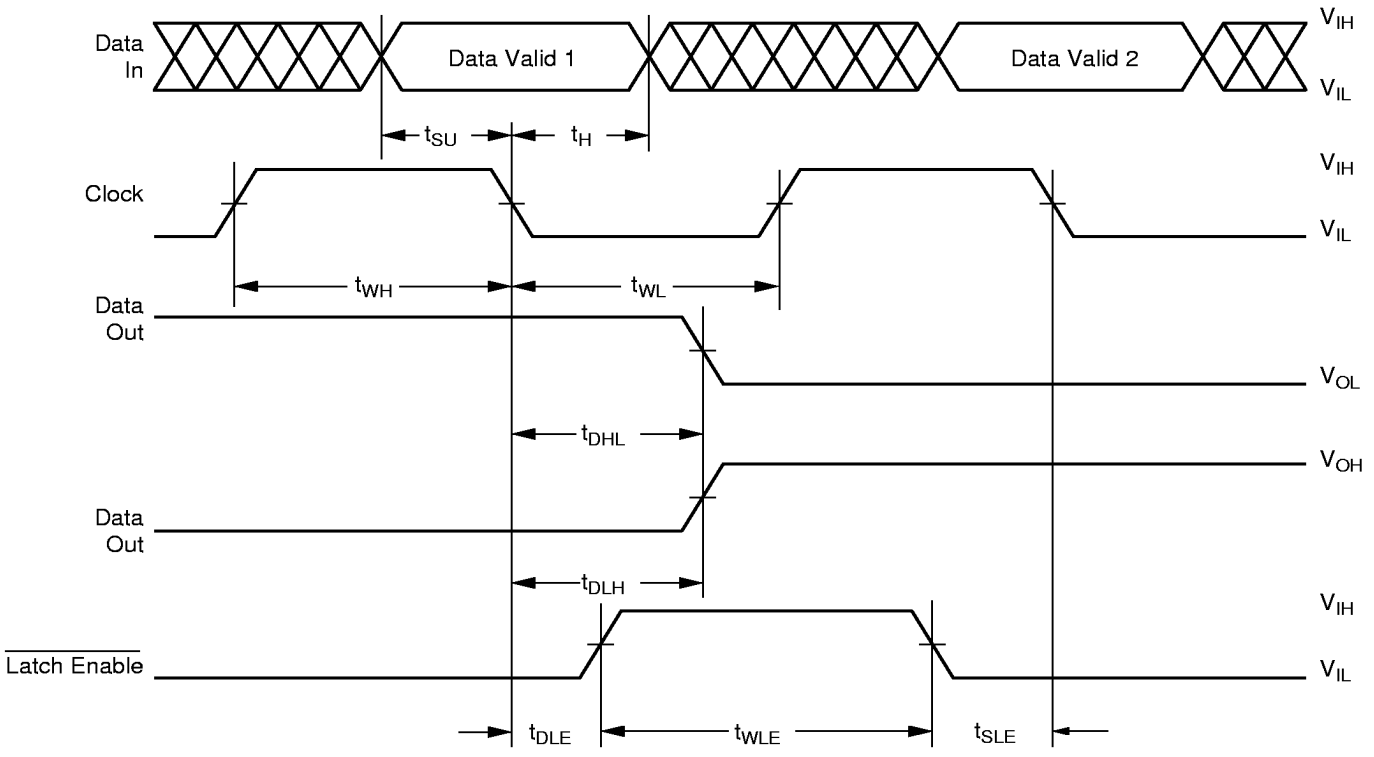
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

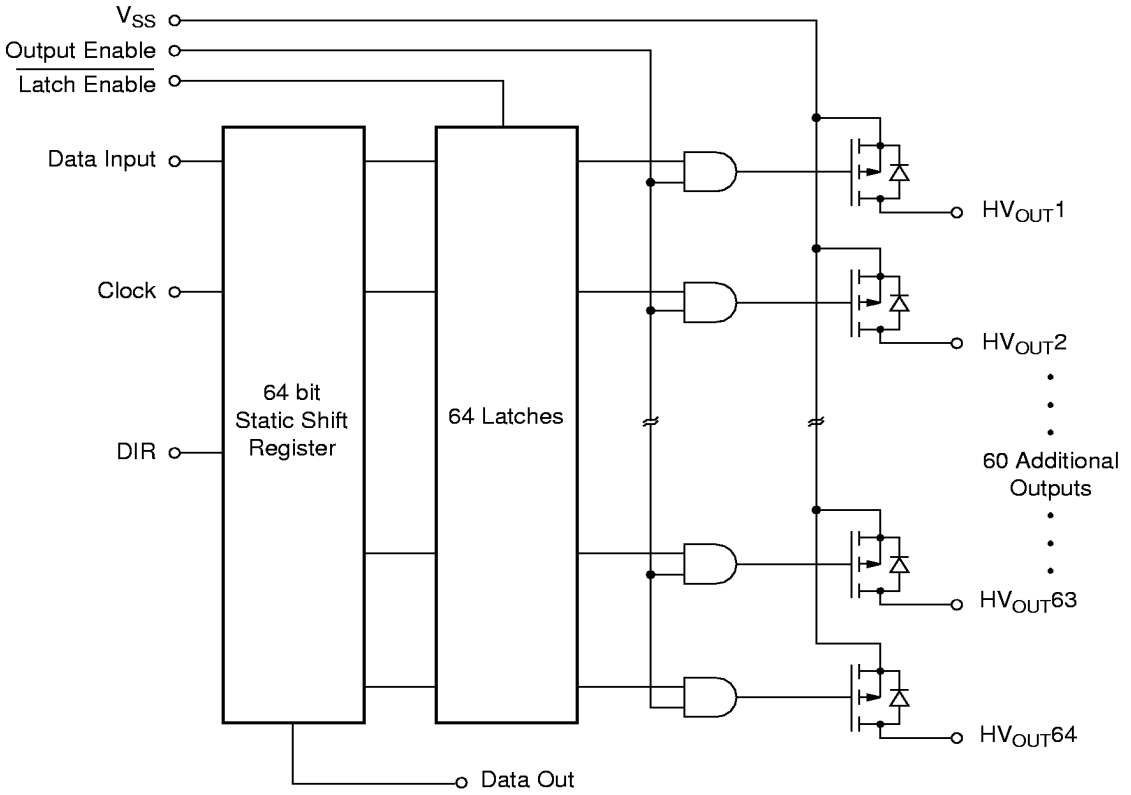
Input and Output Equivalent Circuit



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs						Outputs		
	Data	CLK	LE	OE	DIR	Shift Reg 1 2 … 64	Latch 1 2 … 64	HV_{OUT} 1 2 … 64	D_{OUT}
All off	X	X	X	L	X	*…*	*…*	H…H	*
Load S/R	H or L	↓	L	L	H	H or L…Qn → Qn+1	*…*	H…H	*
	H or L	↓	L	L	L	H or L…Qn → Qn-1	*…*	H…H	*
Load Latch	H or L	↓	H	L	X	H or L…*	H or L…*	H…H	*
Output Enable Transparent Latch Mode	X	H or L	H	H	X	H or L…*	H or L…*	L or H…*	*
	H	↓	H	H	X	H…*	H…*	L …*	*
	L	↓	H	H	X	L …*	L…*	H…*	*

Notes:

X = Don't care

* = Dependent on previous stage's state before the last CLK : High to low transition.

↓ = -5V to V_{SS} transition

H = V_{DD}

L = V_{SS}

Pin Configurations

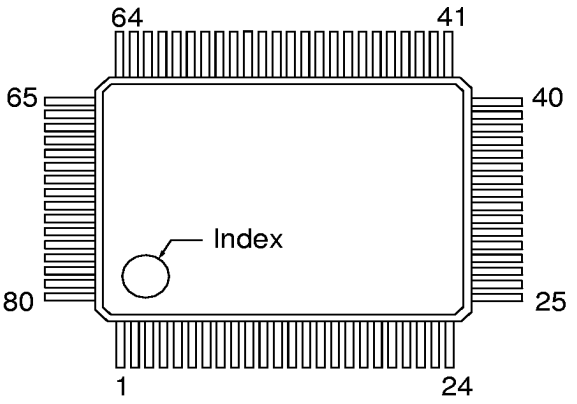
PG Package

HV49

Pin	Function	Pin	Function
1	V_{SS}	41	N/C
2	N/C	42	N/C
3	HV_{OUT} 59/6	43	HV_{OUT} 23/42
4	HV_{OUT} 60/5	44	HV_{OUT} 24/41
5	HV_{OUT} 61/4	45	HV_{OUT} 25/40
6	HV_{OUT} 62/3	46	HV_{OUT} 26/39
7	HV_{OUT} 63/2	47	HV_{OUT} 27/38
8	HV_{OUT} 64/1	48	HV_{OUT} 28/37
9	DIR	49	HV_{OUT} 29/36
10	Data Out	50	HV_{OUT} 30/35
11	CLK	51	HV_{OUT} 31/34
12	V_{SS}	52	HV_{OUT} 32/33
13	V_{DD}	53	HV_{OUT} 33/32
14	$\overline{LE}$	54	HV_{OUT} 34/31
15	Data In	55	HV_{OUT} 35/30
16	OE	56	HV_{OUT} 36/29
17	HV_{OUT} 1/64	57	HV_{OUT} 37/28
18	HV_{OUT} 2/63	58	HV_{OUT} 38/27
19	HV_{OUT} 3/62	59	HV_{OUT} 39/26
20	HV_{OUT} 4/61	60	HV_{OUT} 40/25
21	HV_{OUT} 5/60	61	HV_{OUT} 41/24
22	HV_{OUT} 6/59	62	HV_{OUT} 42/23
23	N/C	63	N/C
24	V_{SS}	64	N/C
25	HV_{OUT} 7/58	65	HV_{OUT} 43/22
26	HV_{OUT} 8/57	66	HV_{OUT} 44/21
27	HV_{OUT} 9/56	67	HV_{OUT} 45/20
28	HV_{OUT} 10/55	68	HV_{OUT} 46/19
29	HV_{OUT} 11/54	69	HV_{OUT} 47/18
30	HV_{OUT} 12/53	70	HV_{OUT} 48/17
31	HV_{OUT} 13/52	71	HV_{OUT} 49/16
32	HV_{OUT} 14/51	72	HV_{OUT} 50/15
33	HV_{OUT} 15/50	73	HV_{OUT} 51/14
34	HV_{OUT} 16/49	74	HV_{OUT} 52/13
35	HV_{OUT} 17/48	75	HV_{OUT} 53/12
36	HV_{OUT} 18/47	76	HV_{OUT} 54/11
37	HV_{OUT} 19/46	77	HV_{OUT} 55/10
38	HV_{OUT} 20/45	78	HV_{OUT} 56/9
39	HV_{OUT} 21/44	79	HV_{OUT} 57/8
40	HV_{OUT} 22/43	80	HV_{OUT} 58/7

Note:
Pin designation DIR = H or L
Example: For DIR = H, Pin 3 is HV_{OUT} 59
For DIR = L, Pin 3 is HV_{OUT} 6

Package Outline



top view

80-pin Gullwing Package