Main Features

- **High Sensitivity Full Frame CCD Sensor**
- **2300 x 3500 Resolution with 10 µm Square Pixels**
- **Bayer Color Mosaic**
- **12-bit Dynamic Range**
- **Very Low Noise: 65 dB SNR**
- **Binning and ROI Modes**
- **LVDS or CameraLink Data Format (Base Configuration)**
- **High Data Rate: 25 Mpixels/s**
- **Flexible and Easy to Operate via RS-232 Control**
  - **Trigger Mode: Free Run or External Trigger Modes**
  - **Binning 2 x 2 and 4 x 4, Up to 5 ROI**
  - **Exposure Time**
  - **Gain: -5 to 29 dB by Steps of 0.04 dB**
  - **Offset: 0 to 255 LSB**
  - **White Balance Adjustment**
  - **Test Pattern Generation**
- **Single Power Supply: 24V_{DC}**
- **High Reliability – CE and FCC Compliant**
- **F (Nikon) Mount Adapter (Lens Not Supplied)**

Product Description

This camera is designed to meet high performance and quality requirements while providing ease of use.

- Atmel manages the entire process, from the sensor to the camera. The result is a camera able to work in 12 bits, with dedicated electronics that provides excellent signal to noise ratio.
- High sensitivity and excellent color reproduction.
- The programmable settings let the user work with different integration times, gains and offsets. The external trigger allows the user to synchronize the camera on an external event while the hardware white balance adjustment avoids subsequent software processing.

Applications

The performance and reliability of this camera make it well suited for the most demanding applications such as film and document scanning, semiconductor and PCB inspection, DNA analysis, metrology, X-ray imaging, etc...

Color 8 Megapixels LVDS and CameraLink™ Digital Cameras

CAMELIA C1 LV 8M
CAMELIA C1 CL 8M

Preliminary

Rev. 5320A–IMAGE–04/03

Improvements

The Camelia 8M has been redesigned:

- To add new features:
  - Gain: 928 steps from -5 to 29 dB
  - Offset: 0 to 255 LSB
  - Test pattern: ramps up from 0 to 2298 pixel values on each line
  - White balance: by separate gain adjustment for the 4 colors of the 2 x 2 Bayer mosaic
- To improve the electro-optical performances, in particular by:
  - Reducing power consumption from 8.5W down to 5.5W, using a new front panel and internal heat sink. This lowers the CCD temperature by 5°C thus decreasing the magnitude of “white pixels”.
  - Decreasing the typical temporal noise from 2.7 to 2.4 LSB
  - Implementing new color filter
- To interface with more standard and cheaper cables
- To improve reliability
- Camelia C1 8M is CE and FCC compliant

What changes for the user?

- New additional commands for gain, offset and test pattern
- RS-232 transmission speed increased from 9600 to 19200 bauds for LVDS cameras (9600 bauds for CameraLink cameras)
- Interface connectors:
  - DATA & SYNC is a 3M MDR connector with better availability, the same pinout but different mechanics
  - RS-232 is a D-Sub 9 female for full-duplex transmission
  - The power supply connector has a camera standard pinout
  - TTL CONTROL is a new D-Sub 9 male connector avoiding the use of a Y cable
- New rear panel (see position of connectors)
- Increased sensitivity: blue x3.5, green x3, red x5 at 3200K on 400 to 700 nm

Imaging System Description

Figure 1. LVDS Camera Imaging System

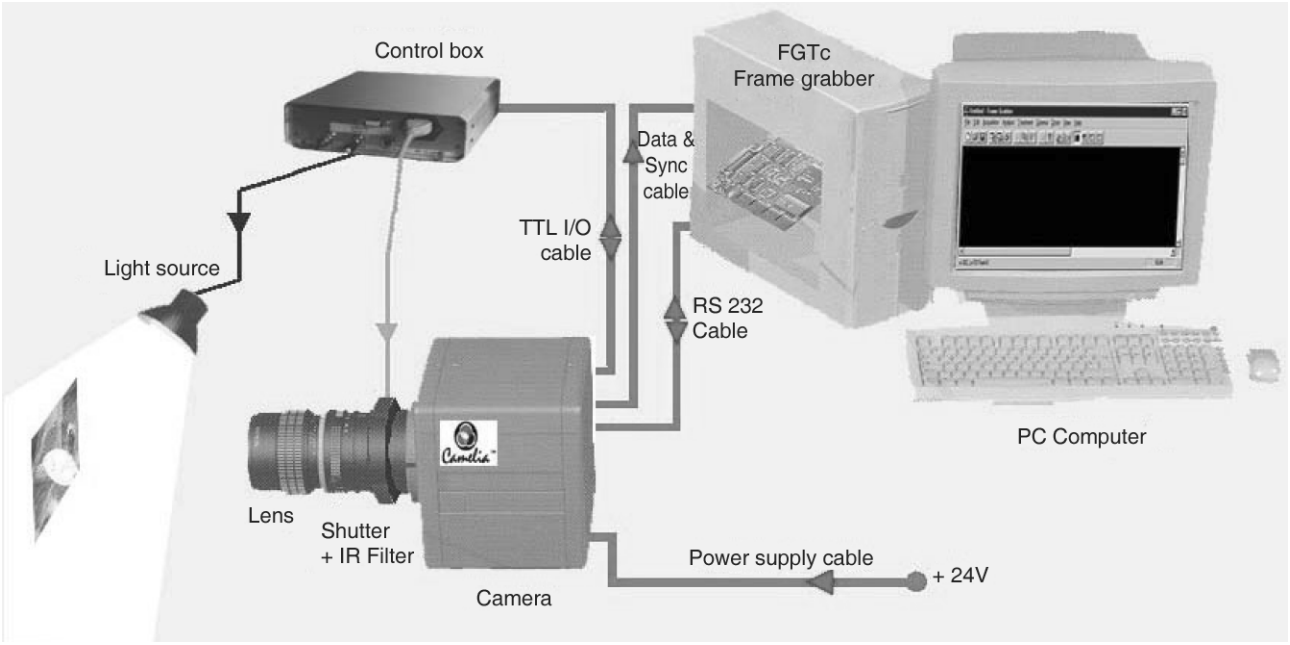
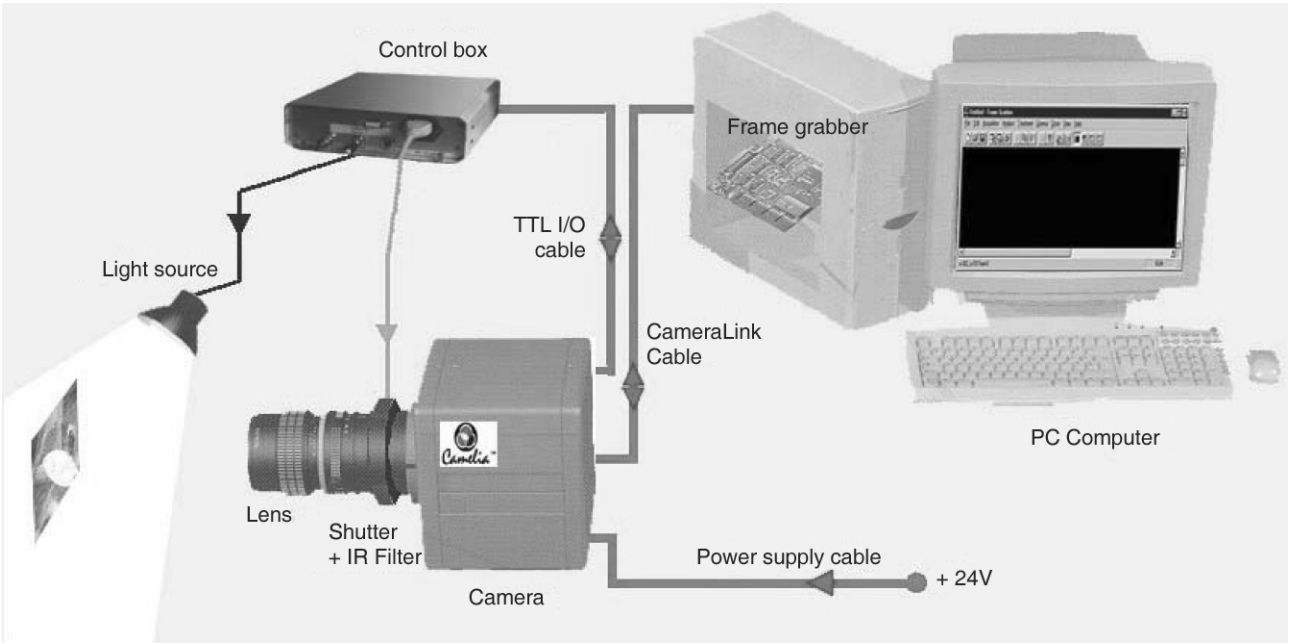


Figure 2. CameraLink Camera Imaging System



The Camelia camera is powered by a single +24V power supply. It is configurable via the serial port of the computer (by using either CommCam software or standard RS-232 communicator as TTY or Hyperterminal) for LSD cameras. Camelia is configurable via the serial communication of CameraLink for CameraLink cameras. It also can send digital video.

As Camelia's CCD is a full frame sensor, the user must use either pulsed lighting or a chopper/shutter in front of the camera in order to have only incident lighting on the CCD during integration time. The user must design an electro-optical interface to drive the camera, the shutter/chopper or lighting by using the SHUTTER signal delivered by the camera. If required, the system can send an external trigger or external ITC (integration time control signal) to the camera.

The BG38 Filter is essential to achieve a correct white balance on Color Cameras and for use with standard optics (for achromaticity purpose).

Note that the following Elements are not provided by Atmel:

- Shutter (LCD or Mechanical)
- BG38 (Anti-infra Red) Filter
- Control Box
- Lens
- Light Source
- +24V Power Supply
- Computer

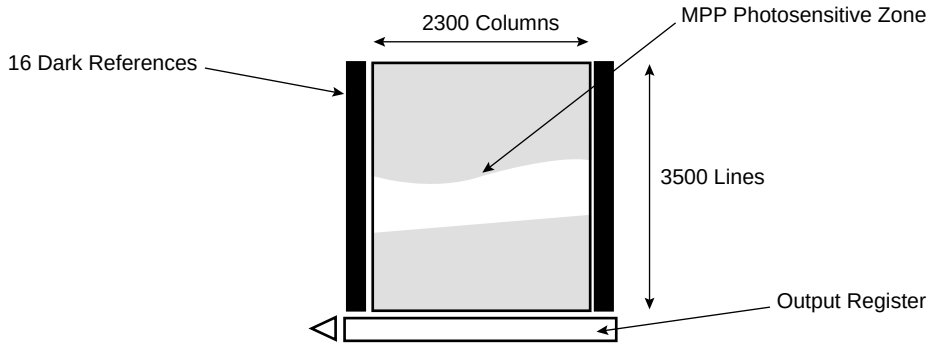
For a complete explanation of the utility of the BG38 Filter and the Shutter, please consult the associated FAQ and the sample images on the Atmel’s "Camera Documentation & Software" CD-Rom.

CCD Description

Image Format

35.0 mm (V) x 23.0 mm (H)

Figure 3. Sensor Organization



Note: The camera does not output to the 16 dark references.

Active Pixels

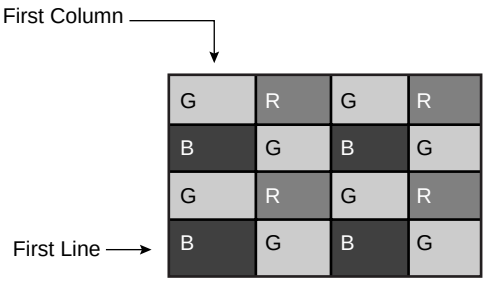
Table 1. Active Pixels

Mode (set via serial com)	Image Size (H x V)	Timing Diagram Correspondence
No binning	2300 x 3500	H = M V = N
2 x 2 pixel binning	1150 x 1750	
4 x 4 pixel binning	574 x 875	

Pixel Geometry

Pixel pitch is 10 µm x 10 µm.

Figure 4. Filter Mosaic (BAYER Pattern)



Note: The first active pixel of first active line is blue.

Antiblooming by Clocking

Antiblooming can be activated or inhibited (see “Serial Communication” on page 13):

- Antiblooming OFF: antiblooming inhibited. This position is recommended if antiblooming is not required for the application.
- Antiblooming ON: antiblooming activated.
- When binning is disabled, the antiblooming is typically efficient up to 8 times saturation light.

Camera Specifications

LSB (Least Significant Bit): 12-bit corresponds to 4095 LSB.

Absolute Maximum Ratings

Storage temperature:	-20 to +70°C
Operating temperature:	0 to +50°C
Operating humidity (non condensing):	< 80% at +35°C
Vibration:	2 g sinusoidal, from 10 to 100 Hz
Power supply:	+20 to +28V

Weight

- Camera with F mount ring: 1400 g
- Camera without F mount ring: 1200 g

Electro-optical Performance

Conditions:

- Camera operating at ambient temperature: 20°C.
- Camera operating in binning 1 x 1 mode and nominal gain 0 dB (G = 173).

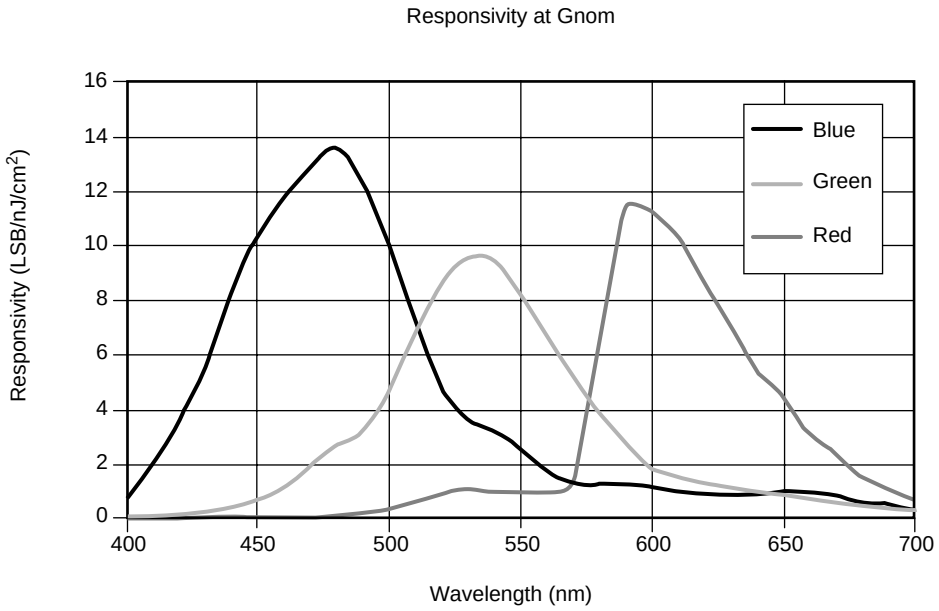
Table 2. Electro-optical Performance

Parameter	Symbol	Typical Value	Unit
Full scale value(1)	VPE	4095	LSB
Temporal noise(2)(3)	VN	2.4	LSB
Dark signal non-uniformity(3)(4)	DSNU	2	LSB.s
Dynamic range(5)	DY	1700 64.6	 dB
Responsivity(6)	R-Blue R-Green R-Red	6.24 5.99 7.85	LSB/(nJ/cm^2)
Responsivity(6)	R-Blue R-Green R-Red	1760 1690 2220	LSB/(lux.s)
Resolution(7) Horizontal Transfer function at Nyquist Vertical Contrast Transfer function at Nyquist	 CTFh CTFv	 20% 20%	 – –
Antiblooming (over illumination capability)(8)	–	8x	–
Electrons to LSB conversion	–	15	e-/LSB
Current consumption(9)	I	230	mA

Notes:
1. Full scale value VPE: maximum digital video signal
2. Temporal noise VN: rms value in darkness; measured by subtracting 2 images, pixel to pixel, at 40 ms of integration time
3. This parameter depends on integration time and on the CCD temperature. Thermal noise doubles with every increase of 16°C temperature. Dark signal doubles with every increase of 8°C temperature. But a internal clamp can correct the mean value of this phenomena.
4. Dark signal non-uniformity: rms value; excludes blemishes
5. Dynamic range DY = VPE/VN measured at 40 ms of integration time
6. Responsitivity conditions: 3200K, with BG38 2 mm, light source powered between 400 and 700 nm, measured on the sensor
7. Resolution conditions: VIDEO = 2000 LSB and red light source used
8. Antiblooming ON and integration time = 100 ms
9. Measured at 24V

Spectral Responsivity

Figure 5. Spectral Responsivity



Note: nJ/cm^2 measured on the sensor

Image Grade Specification

- Defect Sizes
  - Blemish: 1 x 1 defect
  - Cluster: blemish grouping of not more than a given number of adjacent defects:
    1 x 1 < cluster 1 size ≤ 2 x 2
    2 x 2 < cluster 2 size ≤ 5 x 5
  - Column: one-pixel-wide column with more than 7 contiguous defective pixels
  - Defect separation: defects are separated by no less than D min pixels in any direction
- Defects in Darkness
  - Blemish or cluster: pixel(s) whose signal deviate(s) more than 150 LSB
  - Column: column whose signal deviates more than 15 LSB
- Defects under Illumination
  - Blemish or cluster: pixel(s) that deviate(s) by more than +20% or -30% from the *average* pixel
  - Column: column which deviates by more than 10% from the *average* column

Defect Test Conditions

- Room temperature = 20°C
- Integration time in darkness = 100 ms
- Camera operating in binning 1 x 1 mode
- Light source: Halogen 3200K with BG38 (2 mm thick) IR cut- off with f/11 aperture
- Test under illumination at 50% saturation level
- No software correction performed

Classifications

Table 3. Image Grade Classifications

Grade	Blemishes		Cluster 1		Cluster 2		Column	
	Total	D min	Total	D min	Total	D min	Total	D min
E	≤ 500	3	≤ 30	50	≤ 6	100	≤ 5	150
H	≤ 300	3	≤ 10	50	0	–	0	–

CCD Window Specification

- Thickness = 1.2 mm ± 0.05
- Glass index at 588 nm: n = 1.5255
- Admitted defects rate: 0 inclusions > 10 µm
- Transmittance > 98% in the range of 400-700 nm
- Transmittance > 82% in the range of 700-1000 nm
- Flatness of the CCD Window < 100 um (concave)
- Flatness of the CCD chip must be within 30 µm

Camera Features

Regions Of Interest (ROI)

Caution: This function has been available since October 2001 starting with Camera S/N: 01321093. For older Cameras, these commands aren't available and can corrupt the EEPROM (see "Camera Identification" on page 15).

Camelia 8M can operate in multi ROI mode, allowing masking of regions of the image and thus increasing frame rate by a reduced readout time.

The user defines up to 5 windows to be masked. In addition the starting and ending addresses for each window can be specified.

Time reduction: about 92 µs per masked line.

Two steps (under serial communication):

- Enter the list of starting and ending addresses with the command: Y=ssss/eeee/ssss/eeee/…/eeee/
- Enter the number of regions masked with the command: F=X (X=0 to 5)

Rules

The line addresses must be a multiple of 4 (to be compliant with the binning).

The Image starts at Line 0 and ends at Line 3499 and the smallest area consists of 4 lines.

The commands must be send in the following order: "Y=…" then "F=…".

For FGT software users, the user has to resize the number of lines in the FGT settings.

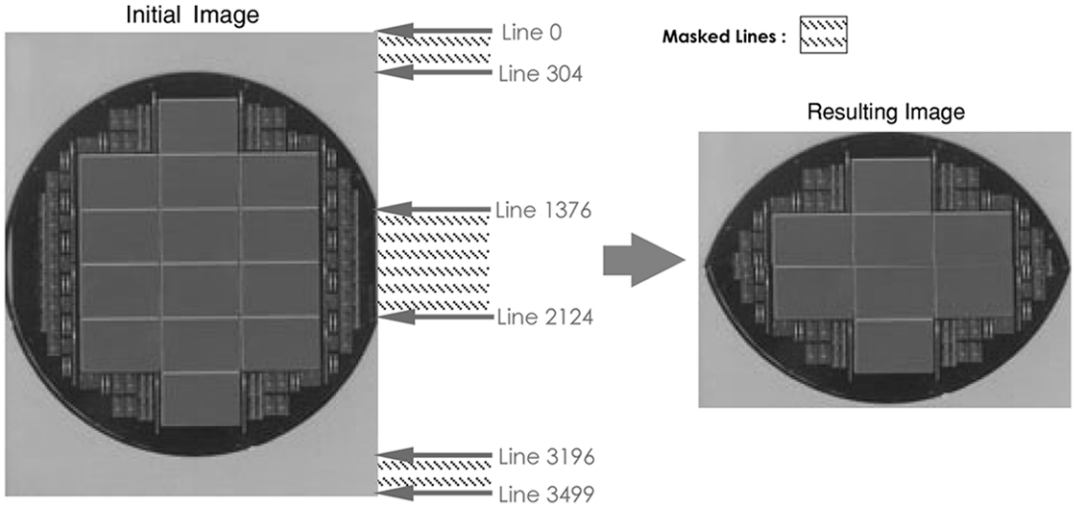
Example

In order to mask 3 regions in the wafer image defined as follows:

- The first 304 lines at the top of the image (blue background)
- 748 lines in the center of the image (two center lines of the wafer)
- The last 304 lines of the image (blue background):
  - "Y=0/304/1376/2124/3196/3499/"
  - "F=3"

In this example readout time will be reduced by 1356 lines which are equivalent to 125 ms.

Figure 6. Readout Time



Gain & Offset

Video signal processing gain and offset can be adjusted by setting the Gain and the Offset via serial communication:

- Gain adjusted from -5.1 to 28.9 dB: G = code 0 to 928
- Nominal gain (factory configuration) is 0 dB: G = code 173
- Offset adjusted from 0 to 255 LSB: O = code 0 to 255
- Gain is applied to the video signal before the addition of offset

Antiblooming by Clocking

Antiblooming can be activated or inhibited (set via serial communication):

- Antiblooming OFF: this position is recommended if antiblooming is not required for the application.
- Antiblooming ON: antiblooming is activated and is effective up to 8 times the saturation level of the sensor.

Test Pattern

In normal mode, the digital video signal from the CCD sensor is available at the LVDS output interface.

For test purpose a fixed digital pattern is generated and can be available instead of the video signal at the LVDS output interface.

The digital pattern is ramped up from 0 to 2298 LSB code (line width); each line presents the same pattern:

This is useful to validate the connection to the acquisition system before adjustment operations relative to image capture.

Selection is set by the Test Pattern Generation command:

- CCD sensor : M = 0
- Test Pattern : M = 1

Color Gain Adjustment

The Camelia 8M Color allows the user to adjust the white balance with on board programmable gains. This function provides separate gain adjustment for the four color pixels of the 2 x 2 Bayer mosaic. Gain is applied to the analog signal.

The four gains are individually programmable by serial communication between -2 and 10 dB by steps of 0.2 dB.

Table 4. Color Gain Definition

Color	Command
Red	**X** = code 0 to 63
Green (red)	**W** = code 0 to 63
Green (blue)	**V** = code 0 to 63
Blue	**U** = code 0 to 63

The gain curve is linear through 63 steps between -2 and 10 dB.

Table 5. Gain Value in dB

Gain Code	Gain Value in dB
63	10 dB
31	4 dB
0	-2 dB

Serial Communication

Serial Configuration

The camera configuration is set by an RS-232 or CameraLink serial interface.

The RS-232 configuration is:

- Full duplex/without handshaking (the camera is configured in DCE/Modem)
- 19200 baud, 8-bit data, no parity bit, 1 stop bit

The CameraLink configuration is:

- 9600 baud, 8-bit data, no parity bit, 1 stop bit

Serial Commands

The following features are available:

Table 6. Serial Commands

Function	Serial Configuration	Comment	Serial Command
Timing mode	3 modes: - continuous (free running) - external trigger - external ITC		T=0 T=1 T=2
Binning	3 modes: - no binning - 2 x 2 pixel binning - 4 x 4 pixel binning	Image size: 2300 (H) x 3500 (V) Image size: 1150 (H) x 1750 (V) Image size: 574 (H) x 875 (V)	B=0 B=1 B=2
Gain	Range from: - G = 5.1 dB - G = 28.9 dB	Steps of around 37 mdB (gain curve is not fully linear)	G=0 G=928
Offset	Range from: - 0 LSB - 255 LSB	Steps of 1 LSB	O=0 O=255
Blue gain	Range from: - U = -2 dB - U = 10 dB	Steps of around 0.19 dB (gain curve is fully linear)	U=0 U=63
Green (blue) gain	Range from: - V = -2 dB - V = 10 dB	Steps of around 0.19 dB (gain curve is fully linear)	V=0 V=63
Green (red) gain	Range from: - W = -2 dB - W = 10 dB	Steps of around 0.19 dB (gain curve is fully linear)	W=0 W=63
Red gain	Range from: - X = -2 dB - X = 10 dB	Steps of around 0.19 dB (gain curve is fully linear)	X=0 X=63

Table 6. Serial Commands (Continued)

Function	Serial Configuration	Comment	Serial Command
Shutter	3 modes: - inactive (always open) - active - inactive (always closed)		 S=0 S=1 S=2
Shutter delay	4 positions: - 1 ms - 10 ms - 20 ms - 40 ms		 D=0 D=1 D=2 D=3
Antiblooming control	2 modes: - active - inactive		 A=0 A=1
Integration time	Integration time value in ms from 1 to 2000 ms	Must be an integer Ex: 120 for 120 ms	Ex: I=120
ROI: number of windows	0 to 5 windows		Ex: F=2
ROI: windows addresses	Line start/Line Stop …	Must be an integer divisible by 4 Line Stop >3 First Line = 0; Last Line = 3499	Ex: Y=1824/2252/ 3156/3499/
Test pattern generation	M=0: Sensor Image M=1: Pattern Image	 To check power, transmission...	M=0 M=1
Special commands		Camera identification readout User camera identification readout Software version readout Camera configuration readout Current camera configuration record Default camera configuration restoration	!=0 !=1 !=2 !=3 !=4 !=5
User camera ID	$= String of Char	Writing and record of the user camera identification	$=

Note: ROI commands have been available since October 2001 starting with Camera S/N: 01321093. For older Cameras, these commands aren't available and can corrupt the EEPROM. If in doubt, please contact our hotline before using ROI function (See "Camera Identification" on page 15).

Command Syntax

- Valid syntax is: S=n(CR) where:
  - S: command identification (S is a single character in upper case)
  - n: setting value
  - (CR): means "carriage return" (ASCII code = 13)
  - No spaces, nor tabs may be inserted between S, =, n and (CR)
  - For the Camelia 8M only, each address value is followed by “/”: Y=ssss/eeee/….eeee/
- Example of a valid command: I=500(CR) (sets the integration time to 500 ms)
- Example of non valid commands:
  - I=500(CR): no space
  - i=500(CR): i instead of I
  - I=3000(CR): 3000 is out of range
  - Y=ssss/eeee/ssssseeee/: a “/” is missing

Settings Validation

New settings are clocked and become valid for the camera at the end of the readout phase. This means that new settings written before the end of readout of image N will be used for image N+1. New settings written after the readout of image N and before the end of readout of image N+1 will be used for image N+2.

Camera Identification

A character string stored in the EEPROM contains the product model, its version and its serial number.

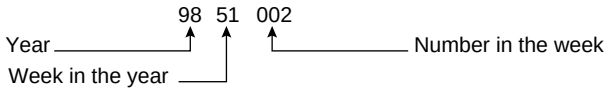
Example: CAMEL_COL_8M_LV_01_9851002

stands for: CAMELIA C1 8M LV, version 01, serial number 9851002

It is read by sending: !=0(CR)

The serial number is detailed as follows:

Figure 7. Serial Number



Customer Identification

Customer identification is a character string (25 characters max).

- It is set and stored in the EEPROM by sending $=xx..xx
- It is read by sending !=1(CR)

Reading Firmware Version

When receiving !=2(CR) the camera returns the version of the firmware.

Reading Current Settings

When receiving !=3(CR) the camera returns its current settings.

Storing the Current Configuration

When receiving !=4(CR) the camera stores the current configuration in the EEPROM.

Factory Configuration

When receiving !=5(CR), the camera sends back its factory configured settings:

A=0(CR)
G=173(CR)
U=0(CR)
V=0(CR)
W=0(CR)
X=0(CR)
O=16(CR)
S=1(CR)
B=0(CR)
T=0(CR)
I=0100(CR)
D=2(CR)
M=0(CR)
F=0(CR) (Yis not set)
>OK(CR)

Timing

2 x 2 and 4 x 4 pixel binning can be used to enable previewing modes. The preview mode is only available in black and white, otherwise the user has to use Overlay mode (correction and software LUT are not applicable on displayed images).

Table 7. Timing Mode

Mode	Frame Readout Time	Line Readout Time	Max Frame Rate
No binning B=0	370 ms	104 µs	2.67 f/s
2 x 2 pixel binning B=1	200 ms	114 µs	4.91 f/s
4 x 4 pixel binning B=2	110 ms	134 µs	8.82 f/s

LVDS Camera Timing

Three timing modes are available: continuous, external triggered and Integration Time Control (ITC).

The signals in the following drawings are described in Table 8:

Table 8. LVDS Frame Timing

Signal	Name	Description	Cam. In/Out	DATA & SYNC Pins	TTL CONTROL Pins
LEN	Line ENable	Low state active when pixel is part of line	Out	26/27	–
FEN	Frame ENable	Low state active when lines are part of frame	Out	3/4	–
SHUTTER	SHUTTER sync	External shutter Trig output Signal (high level active)	Out	21/22(1)	1(1)
TRIG	TRIGger	External Trigger Input Signal (Rising Edge)	In	46/47(1)	2(1)
ITC	Integration Time Control	External ITC Input Signal (Falling/Rising Edges)	In	46/47(1)	2(1)
PCK	Pixel ClocK	Internal Master Data Clock Signal at 25 MHz	Out	1/2	–

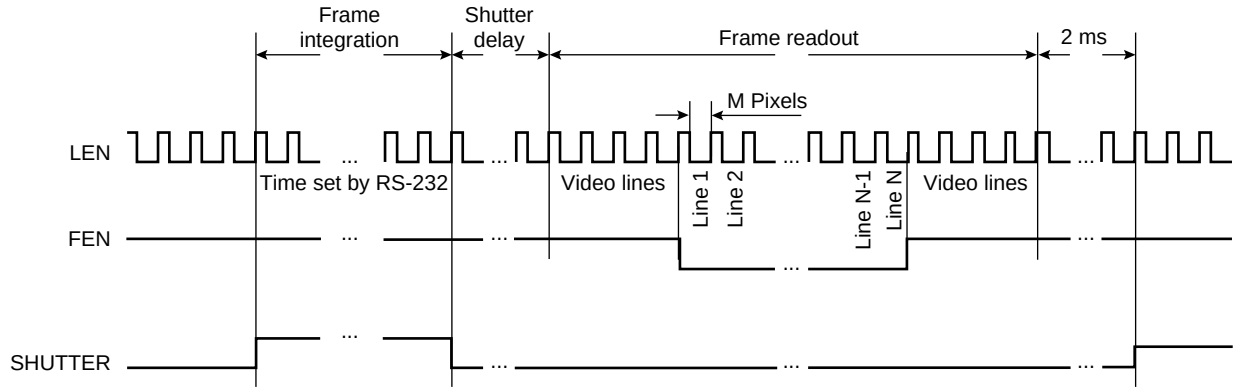
Notes:
1. Signal present on both connectors.
2. Pixel is defined as valid (part of the Frame) when both LEN and FEN signals are at a low level.
3. The maximum latency (called Td) after of 1 readout line time defined below depends on the binning mode. In binning 1 x 1 mode, this delay is around 104 µs.
4. Minimum time at high level of the LEN signal is 10 µs (transfer time between two lines).
5. Minimum time at high level of the FEN signal is 4 lines readout time (around 416 µs).
6. Shutter delay is adjustable via Commcam or RS-232 commands (1, 5, 10 or 20 ms).

Continuous: T=0

The camera delivers frames continuously:

- Frame N+1 integration starts as soon as frame N readout has been completed.
- Integration time is set by RS-232.
- Video Lines (before and after valid frame) are 4 + 4 for Binning 1 x 1 (and also 1 + 1 for Binning 4 x 4).

Figure 8. LVDS Continuous Timing Diagram

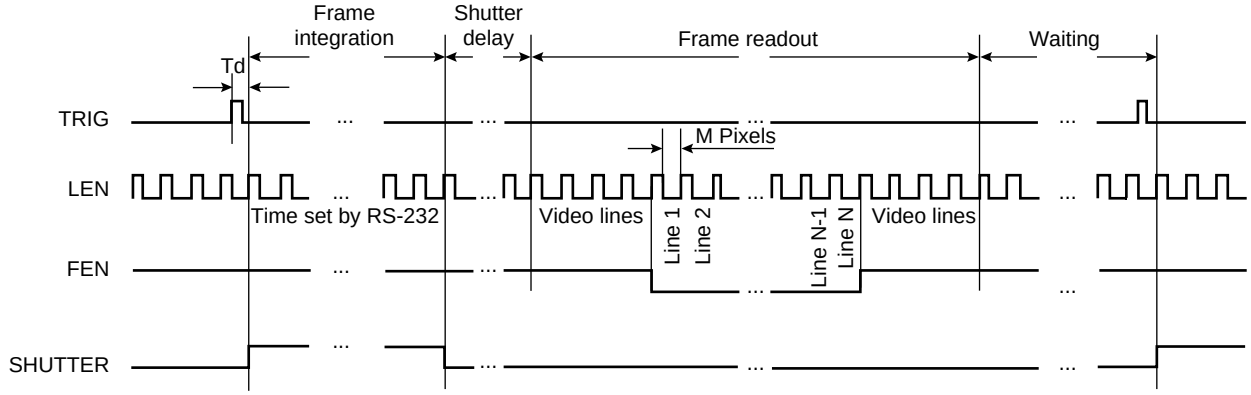


Operation with External Trigger: T=1

Integration start is controlled by the user by the external signal TRIG:

- The rising edge of TRIG activates the start of frame integration. This rising edge is synchronized by the camera with a latency of Td (time delay equivalent to a readout time for a line: see notes in Table 8 on page 17).
- Integration time is set by RS-232.
- Note: The TRIG signal period must be greater than the sum of the integration time and frame readout time.
- Video Lines (before and after valid frame) are 4 + 4 for Binning 1 x 1 (and also 1 + 1 for Binning 4 x 4).

Figure 9. LVDS External Trigger Timing Diagram

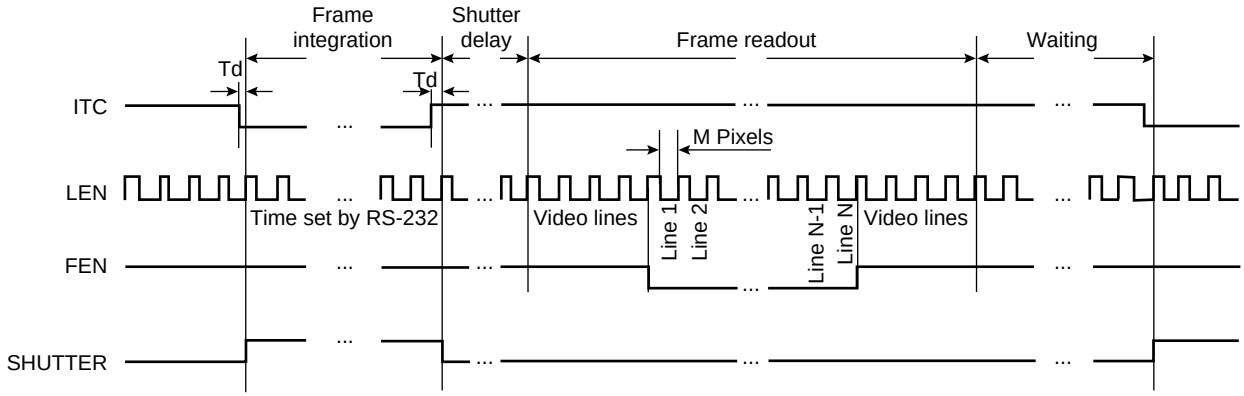


Operation with Integration Time Control: T=2

Integration is fully controlled by the user by the external signal ITC:

- The falling edge of ITC activates the start of frame integration. This falling edge is synchronized by the camera with a latency of Td (time delay equivalent to a readout time for a line: see notes in Table 8 on page 17).
- The rising edge of ITC activates the stop of frame integration. This rising edge is synchronized by the camera with the same latency as Td.
- Note: The ITC signal period must be greater than the sum of the integration time (defined by ITC low) and frame readout time.
- Video Lines (before and after valid frame) are 4 + 4 for Binning 1 x 1 (and also 1 + 1 for Binning 4 x 4).

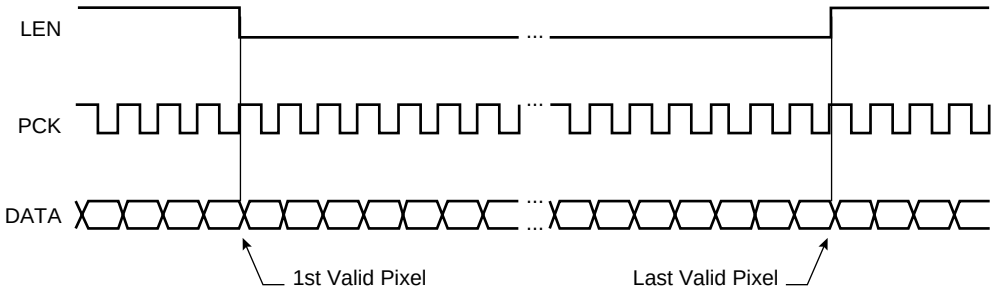
Figure 10. LVDS Integration Time Control Timing Diagram



Line Timing

- Duty cycle of the PCK is 50%
- Rising and falling edges: 1.5 ns
- Pixel clock PCK and Data rate are: 25 MHz in binning mode 1 x 1, 12.5 MHz in binning mode 2 x 2 and 6.25 MHz in binning mode 4 x 4
- Minimum setup time of Data, LEN and FEN, to the rising edge of PCK: 10 ns
- Minimum hold time of Data, LEN and FEN, after the rising edge of PCK: 10 ns

Figure 11. LVDS Line Timing Diagram



CameraLink Camera Timing

Three timing modes are available: continuous, external triggered and Integration Time Control (ITC).

The signals in the following drawings are described in Table 9:

Table 9. CameraLink Frame Timing

Signal	Name	Description	Cam. In/Out	Camera Link Connector	TTL CONTROL Connector
LVAL	Line VALid	High state active when pixel is part of line	Out	yes	no
FVAL	Frame VALid	High state active when lines are part of frame	Out	yes	no
SHUTTER	SHUTTER sync	External shutter Trig output Sig. (high level active)	Out	no	Pin 1
TRIG	TRIGger	External Trigger Input Signal (Rising Edge)	In	CC1+/ CC1-(1)	Pin 2(1)
ITC	Integration Time Control	External ITC Input Signal (Falling/Rising Edges)	In	CC1+/ CC1-(1)	Pin 2(1)
PCK	Pixel ClocK	Internal Master Data Clock Signal at 25 MHz	Out	yes	no

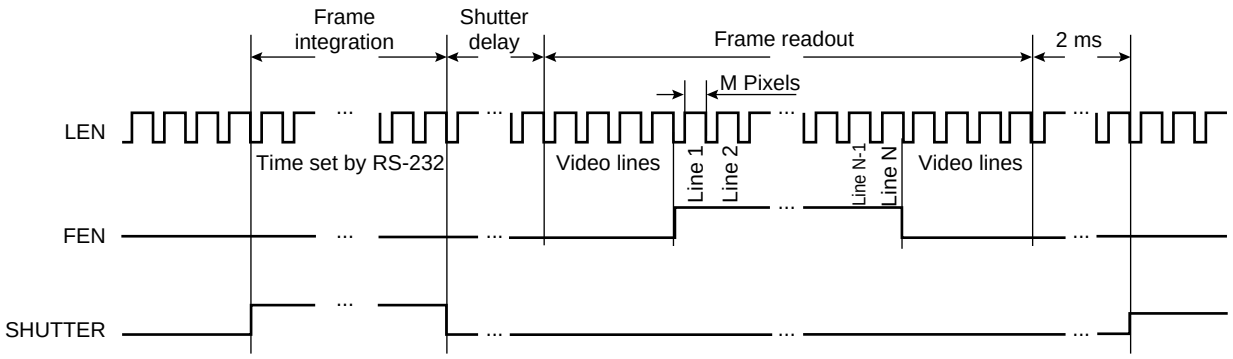
Notes:
1. Signal present on both connectors.
2. Pixel is defined as valid (part of the Frame) when both LVAL and FVAL signals are at a high level.
3. The maximum latency (Td) of 1 readout line time defined below depends on the binning mode. In binning 1 x 1 mode, this delay is around 104 µs.
4. Minimum time at low level of LVAL signal is 10 µs (transfer time between two lines).
5. Minimum time at low level of FVAL signal is 4 lines readout time (around 416 µs).
6. Shutter delay is adjustable via serial communication commands (1, 5, 10 or 20 ms).

Continuous: T=0

The camera delivers frames continuously:

- Frame N+1 integration starts as soon as frame N readout has been completed.
- Integration time is set by serial communication.
- Video Lines (before and after valid frame) are 4 + 4 for Binning 1 x 1 (and also 1 + 1 for Binning 4 x 4).

Figure 12. CameraLink Continuous Timing Diagram

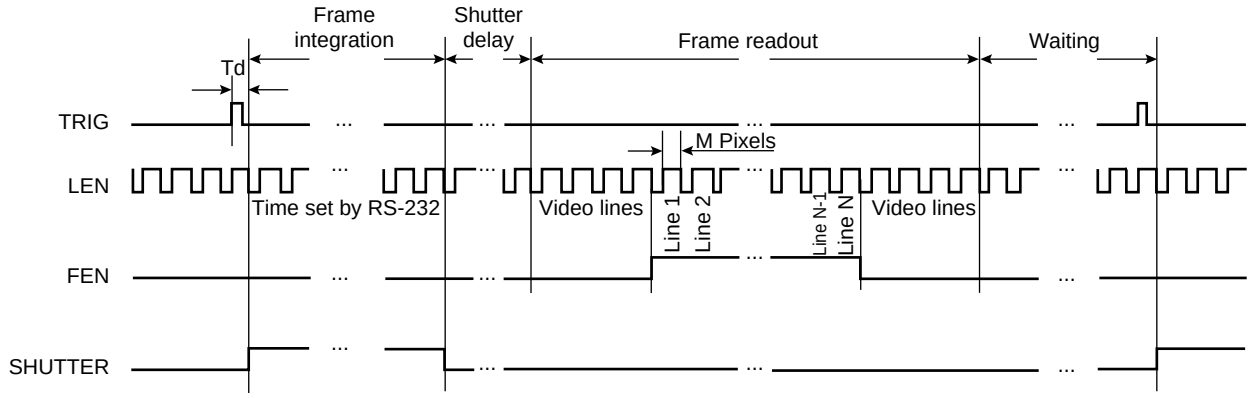


Operation with External Trigger: T=1

Integration start is controlled by the user with the external signal TRIG:

- The rising edge of TRIG activates the start of frame integration. This rising edge is synchronized by the camera with a latency of Td (time delay equivalent to a readout time for a line: see notes in Table 9 on page 20).
- Integration time is set by serial communication.
- Note: The TRIG signal period must be greater than the sum of the integration time and frame readout time.
- Video Lines (before and after valid frame) are 4 + 4 for Binning 1 x 1 (and also 1 + 1 for Binning 4 x 4).

Figure 13. CameraLink External Trigger Timing Diagram

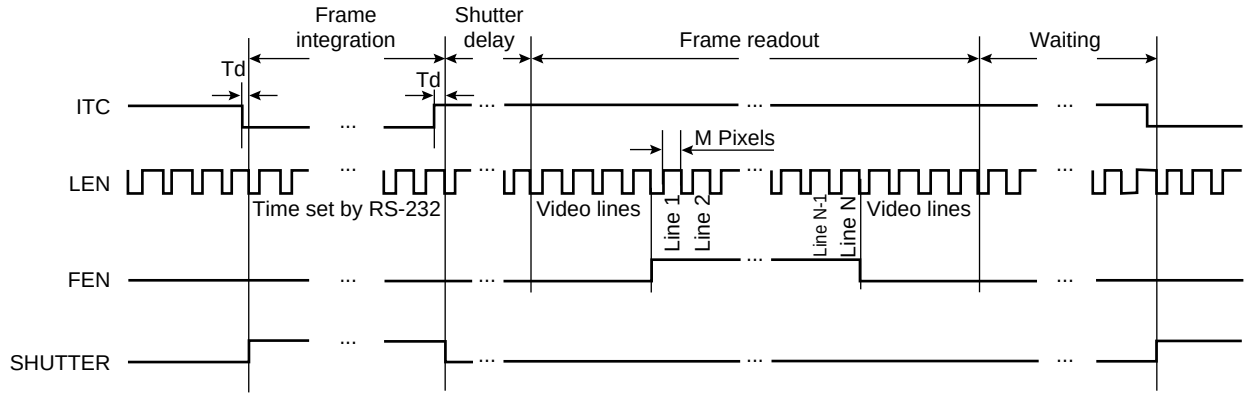


Operation with Integration Time Control: T=2

Integration is fully controlled by the user with the external signal ITC:

- The falling edge of ITC activates the start of frame integration. This falling edge is synchronized by the camera with a latency of Td (time delay equivalent to a readout time for a line: see notes in Table 9 on page 20).
- The rising edge of ITC activates the stop of the frame integration. This rising edge is synchronized by the camera with the same latency of Td.
- Note: The ITC signal period must be greater than the sum of the integration time (defined by ITC low) and frame readout time.
- Video Lines (before and after valid frame) are 4 + 4 for Binning 1 x 1 (and also 1 + 1 for Binning 4 x 4).

Figure 14. CameraLink Integration Time Control Timing Diagram

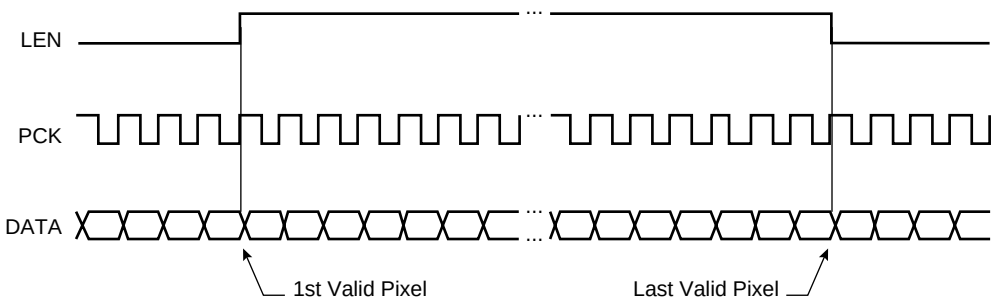


Line Timing

- Duty cycle of the PCK is 50%
- PCK clock rate is 25 MHz
- Data rate (Internal pixel clock) is 25 MHz in binning mode 1 x 1

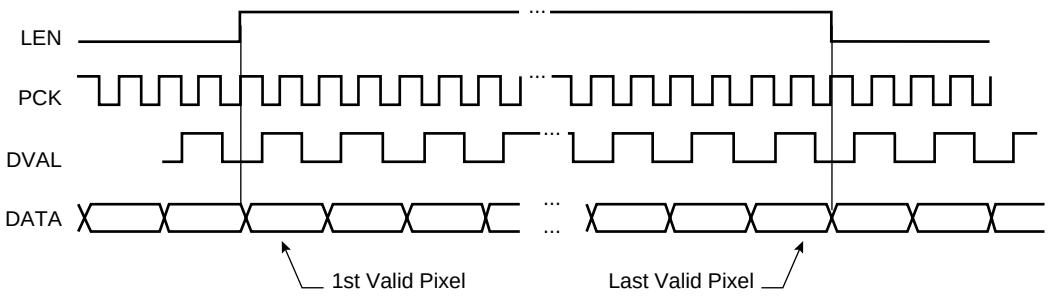
- Mode binning 1 x 1:
  - Data rate is 25 MHz
  - DVAL always in high state

Figure 15. CameraLink Line Timing Diagram for Binning 1 x 1



- Mode binning 2 x 2 (and 4 x 4):
  - Data rate is 12.5 MHz (or 6.25 MHz)

Figure 16. CameraLink Line Timing Diagram for Binning 2 x 2 (and 4 x 4)



Electrical Interfaces

DATA & SYNC and TTL CONTROL for LVDS Camera

Table 10. Specifications

Symbol	I/O	Definition	Level
TRIG_ITC	I	Timing control: - TRIG_ITC is either an external trigger or integration time control (ITC) depending on the timing mode configured via RS-232. Operation with external trigger: - TRIG_ITC = TRIG Operation with ITC: - TRIG_ITC = ITC - TRIG_ITC is synchronized by the camera line clock (jitter: 104 µs)	LVDS(1) and TTL
PDATA(11..0)	O	Digital video output: 12-bit	LVDS
FEN	O	Frame enable: - FEN = 0: frame data valid: active lines - FEN = 1: frame data not valid	LVDS
LEN	O	Line enable: - LEN = 0: line data valid: active pixels - LEN = 1: line data not valid	LVDS
PCK	O	Pixel clock	LVDS
SHUTTER	O	Shutter open/close: - shutter open = 1 - shutter closed = 0 Delay between the falling edge of SHUTTER and the start of readout: - 4 positions: 1, 10, 20 or 40 ms (set via RS-232)	LVDS and TTL

Note: 1. LVDS (Low Voltage differential Signal): EIA 644 standard.

All digital I/Os are differential: (signal+, signal-). Specifications are given for signal +.
LVDS drivers/receivers:

- Manufacturer NS
- Driver: DS90LVO47ATMTC (SO16 package)
- Receiver: DS90LVO48ATMTC (SO16 package)

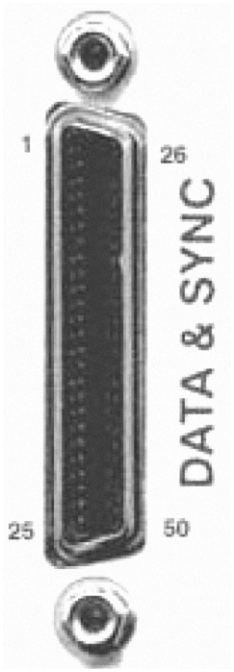
DATA & SYNC Cabling

50-pin connector:

- Connector reference on camera: 3M 10250-6212JL (or 3M 10250-6212VC)
- Mating connector on cable side: 3M 10150-6000EL; shell: 3M 10350-A200-00
- We recommend using a twisted pair shielded cable.

Table 11. Pinout

Pin Number	Signal	I/O	Pin Number	Signal	I/O	
1	PCK+	O	26	LEN+	O	
2	PCK-	O	27	LEN-	O	
3	FEN+	O	28	Do Not Connect	O	
4	FEN-	O	29	Do Not Connect	O	
5	Do Not Connect	O	30	GROUND	O	
6	Do Not Connect	O	31	GROUND	O	
7	PDATA0+	O	32	PDATA1+	O	
8	PDATA0-	O	33	PDATA1-	O	
9	PDATA2+	O	34	PDATA3+	O	
10	PDATA2-	O	35	PDATA3-	O	
11	PDATA4+	O	36	PDATA5+	O	
12	PDATA4-	O	37	PDATA5-	O	
13	PDATA6+	O	38	PDATA7+	O	
14	PDATA6-	O	39	PDATA7-	O	
15	PDATA8+	O	40	PDATA9+	O	
16	PDATA8-	O	41	PDATA9-	O	
17	PDATA10+	O	42	PDATA11+	O	
18	PDATA10-	O	43	PDATA11-	O	
19	GROUND	–	44	NC	–	
20	GROUND	–	45	NC	–	
21	SHUTTER+	O	46	TRIG_ITC+	I	
22	SHUTTER-	O	47	TRIG_ITC-	I	
23	Do Not Connect	I	48	Do Not Connect	I	
24	Do Not Connect	I	49	Do Not Connect	I	
25	NC	–	50	NC	–	

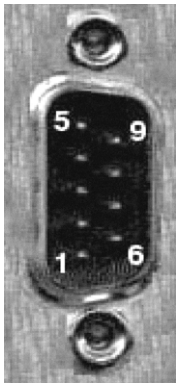


Note: NC: not connected

TTL CONTROL Cabling

The connector on the camera is D-sub 9 pins male.

Table 12. Pinout

Pin Number At Camera Output	Signal	Direction	
1	SHUTTER	Out	
2	TRIG-ITC	In	
3	Do Not Connect	In	
4	Do Not Connect	In	
5	NC	–	
6	NC	–	
7	Do Not Connect	Out	
8	Do Not Connect	Out	
9	GROUND	–	

Notes:
1. TRIG-ITC is provided by the DATA & SYNC (MDR50) Connector in LVDS format or by the TTL CONTROL connector; the two different signals are logically “anded” as follows: TRIG-ITC from LVDS and TRIG-ITC from TTL. The inputs left open are internally tied to a high level.
2. The SHUTTER Output is available on both DATA & SYNC and TTL Output Connectors.

CAMERALINK and TTL CONTROL for CameraLink Camera

Table 13. Specifications

Symbol	I/O	Definition	Level
TRIG_ITC(1)	I	Timing control: - TRIG_ITC is either an external trigger or integration time control (ITC) depending on the timing mode configured via serial communication. Operation with external trigger: - TRIG_ITC = TRIG Operation with ITC: - TRIG_ITC = ITC - TRIG_ITC is synchronized by the camera line clock (jitter: 104 µs)	LVDS(2) and TTL
PDATA(11..0)	O	Digital video output: 12-bit	LVDS
FVAL	O	Frame enable: - FVAL = 1: frame data valid: active lines - FVAL = 0: frame data not valid	LVDS
LVAL	O	Line enable: - LVAL = 1: line data valid: active pixels - LVAL = 0: line data not valid	LVDS
DVAL	O	Data Strobe: - DVAL = 1: pixel data valid - DVAL = 0: pixel data not valid	LVDS
PCK	O	Pixel clock	LVDS
SHUTTER	O	Shutter open/close: - shutter open = 1 - shutter closed = 0 Delay between the falling edge of SHUTTER and the start of readout: - 4 positions: 1, 10, 20 or 40 ms (set via serial communication)	TTL

Notes: 1. TRIG_ITC signal is connected on CC1 differential inputs
2. LVDS (Low Voltage differential Signal): EIA 644 standard

All digital I/Os are differential: (signal+, signal-). Specifications are given for signal +.

CameraLink drivers/receivers:

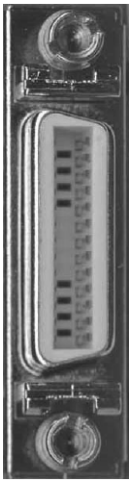
- Driver: NS DS90CR285MTD (SO56 package)
- Receiver: NS DS90LVO48ATMTC (SO16 package)

CAMERALINK Cabling

26-pin connector:

- Connector reference on camera: 3M 10226-2210VE
- We recommend using a CameraLink Standard shielded cable such as the 3M 14X26-SZLB-XXX-0LC.

Table 14. Pinout

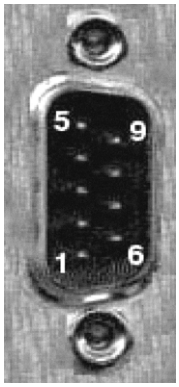
Pin Number	Signal	I/O	Pin Number	Signal	I/O	
1	GROUND	–	14	GROUND	–	
2	X0-	O	15	X0+	O	
3	X1-	O	16	X1+	O	
4	X2-	O	17	X2+	O	
5	XCLK-	O	18	XCLK+	O	
6	X3-	O	19	X3+	O	
7	SERTC+	I	20	SERTC-	I	
8	SERTFG-	O	21	SERTFG+	O	
9	CC1-	I	22	CC1+	I	
10	CC2+	I	23	CC2-	I	
11	CC3-	I	24	CC3+	I	
12	CC4+	I	25	CC4-	I	
13	GROUND	–	26	GROUND	–	

Note: NC: not connected

TTL CONTROL Cabling

The connector on the camera is D-sub 9 pins male.

Table 15. Pinout

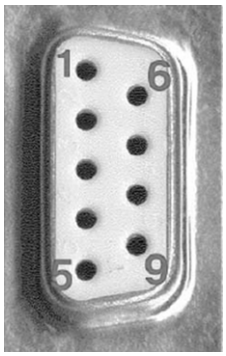
Pin Number At Camera Output	Signal	Direction	
1	SHUTTER	Out	
2	TRIG-ITC	In	
3	Do Not Connect	In	
4	Do Not Connect	In	
5	NC	–	
6	NC	–	
7	Do Not Connect	Out	
8	Do Not Connect	Out	
9	GROUND	–	

Notes: 1. TRIG-ITC is provided by the DATA & SYNC (MDR26) connector in LVDS format or by the TTL CONTROL connector; the two different signals are logically “anded” as follows: TRIG-ITC from LVDS and TRIG-ITC from TTL. The inputs left open are internally tied to a high level.

RS-232 for LVDS Camera

- On camera side: D-sub 9 pins female
- On computer side: Dsub9 male, pinout compatible with computer serial port
- Note: the cable to be used is a straight pin to pin male-female

Table 16. Pinout

Pin Number At camera output	Signal	
1	NC	
2	TX	
3	RX	
4	NC	
5	GROUND	
6	NC	
7	NC	
8	NC	
9	NC	

Notes: 1. NC: not connected
2. Pin 7 and 8 are internally shorted.

Power Supply

Specifications

Table 17. Power Supply Specifications

Parameter	Nominal Value	Min Value	Max Value
Voltage	+24V	+20V	+28V
Current	0.23A	0.26A	0.20A

Cabling

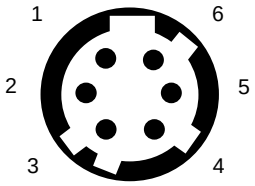
- Camera connector type: Hirose HR10A-7R-6PB (male)
- Cable connector type: Hirose HR10A-7P-6S (female)

Table 18. Pinout

Pin Number	Signal	Pin Number	Signal
1	PWR	4	GND
2	NC	5	NC
3	PWR	6	GND

Note: NC: not connected

Figure 17. Receptacle Viewed from behind the Camera



Caution: Power supply cabling is fully compatible with Atmel's AviivA Linescan Cameras. The cabling is NOT compatible with old Camelia 8M.

An internal 1A fuse protects the camera against high currents.

An internal diode protects the camera against cabling inversion.

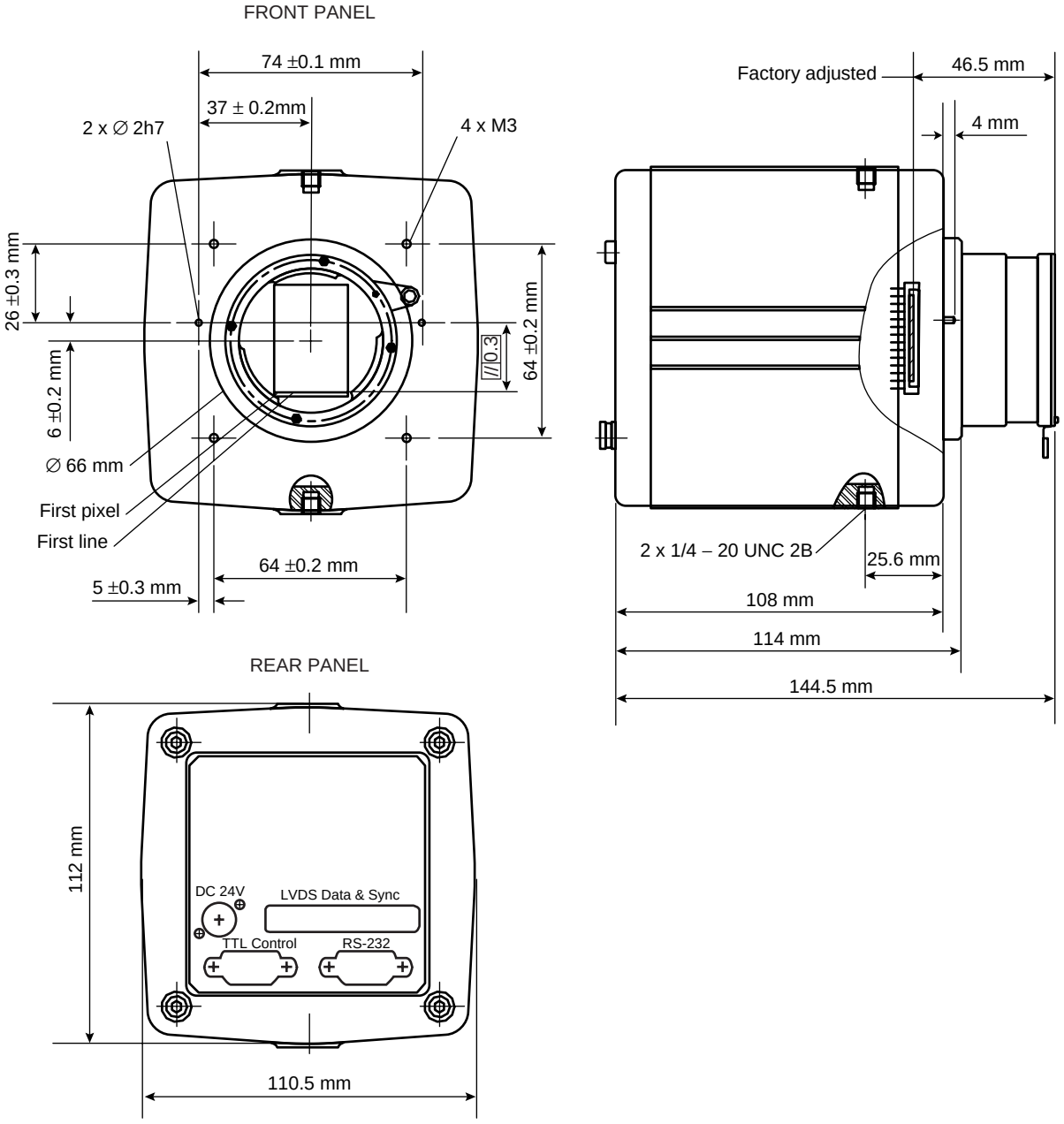
Kits of Cable

- LVDS-FGT: FGT frame grabber color + DATA & SYNC for FGT frame grabber (length 3 meters) + Power Supply (length 10 meters, open on power supply side) + RS-232 (length 3 meters)
- CameraLink: CameraLink (length 5 meters) + Power Supply (length 10 meters, open on power supply side)
- Connectors LVDS: 3M MDR 50 + HR10A-7P-6S + D-Sub9 male

Mechanical Interface

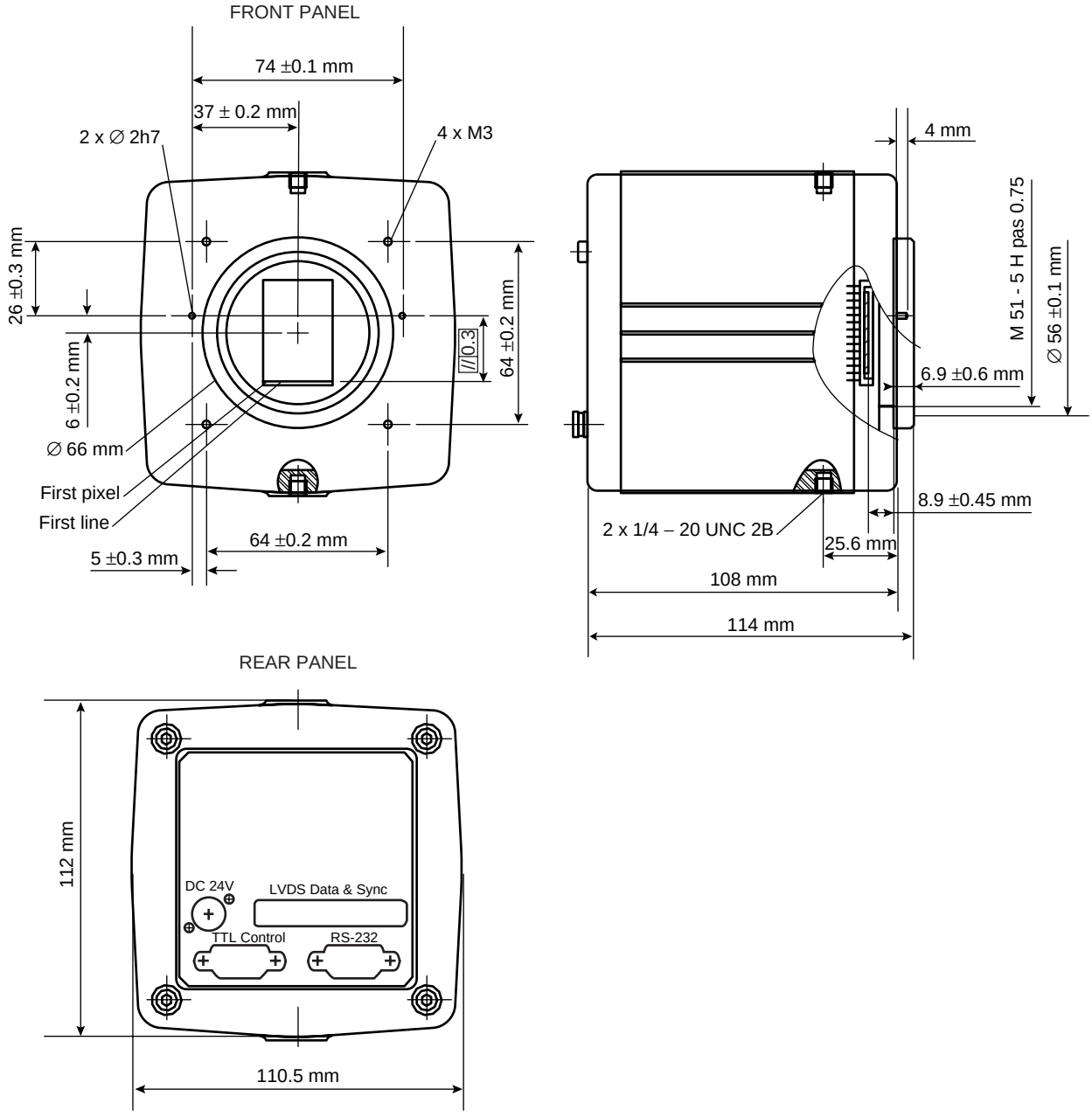
LVDS Camera with F Mount Ring

Figure 18. With F Mount Ring



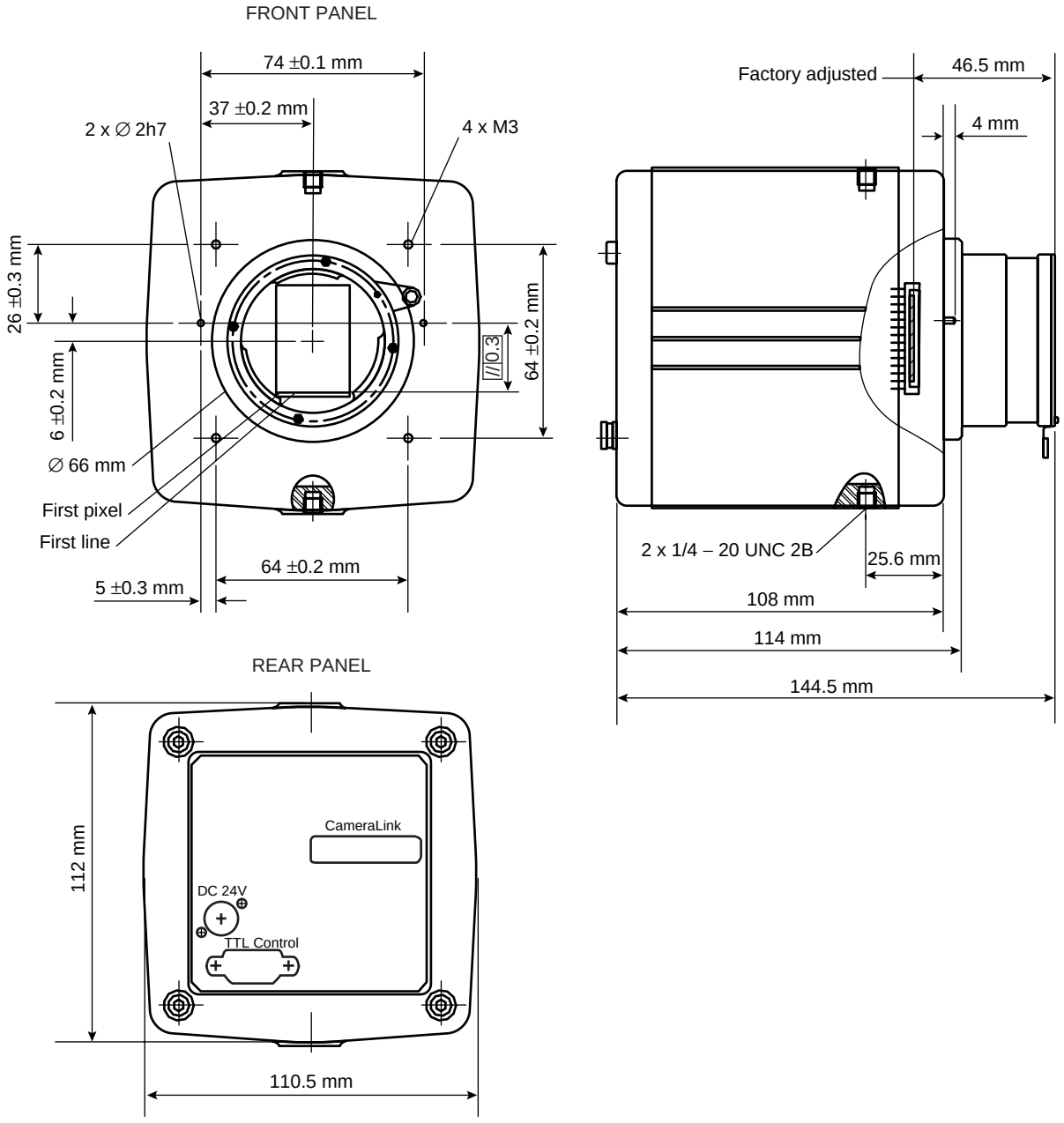
LVDS Camera without F Mount Ring

Figure 19. Without F Mount Ring



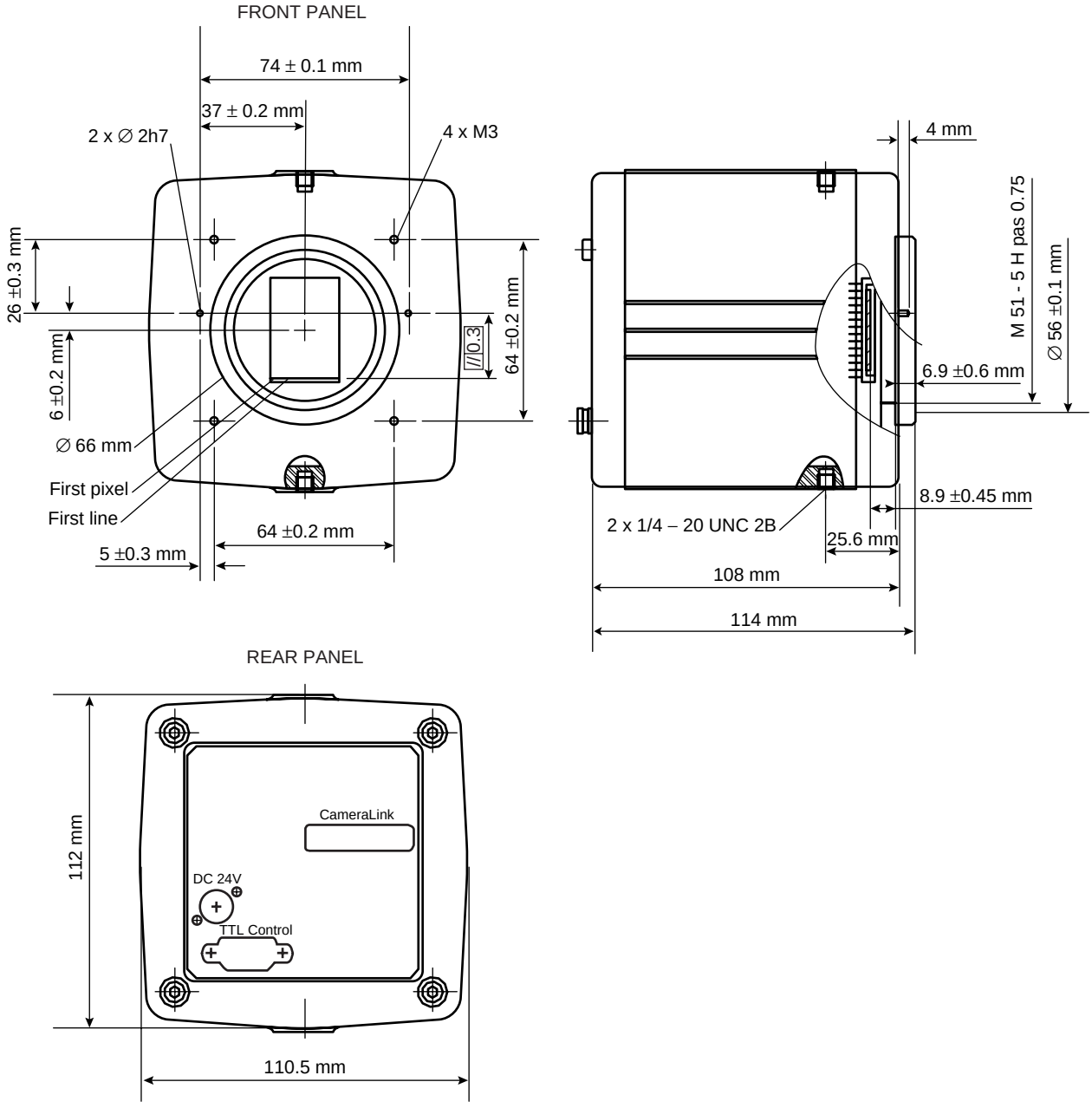
CameraLink Camera with F Mount Ring

Figure 20. With F Mount Ring



CameraLink Camera without F Mount Ring

Figure 21. Without F Mount Ring



Mechanical Mounting References

- Position in the X, Y plan:
  - The center pixel of the CCD sensor is positioned within a circle centered on the optical axis and with a diameter of 0.35 mm. The optical axis is defined by the mechanical thread for the optical adapter.
  - The center pixel of the CCD sensor is referenced to the two needles on the front panel with a tolerance of ±0.125 mm.
- Position in the Z plan:
  - For cameras delivered with an F mount ring, the distance from the CCD sensor plan to the Nikon mount is adjusted in factory at 46.5 mm.
  - For cameras delivered without the F mount ring, the distance from the CCD sensor plan to the front plan of the thread is 8.9 ±0.45 mm.
- Tilt around the Z axis:
  - All the pixels of the CCD sensor are located between two plans, perpendicular to the optical axis and separated by a maximum distance of 0.26 mm.

Standard Conformity

The cameras have been tested in the following conditions:

- Camera with complete Atmel housing
- Shielded power supply cable
- Shielded and twisted pair data transfer cable
- TTL CONTROL cable
- Linear AC-DC power supply

We recommend using the same configuration to ensure compliance with the following standards.

CE conformity

The Camelia Camera complies with the European directive 89/336/CEE (EN55022 A/CISPR22, EN55024).

Class A of EN55022 is obtained without condition. Class B of EN55022 is obtained with ferrite beads on the DATA/SYNC and TTL CONTROL cables.

FCC conformity

The Camelia Camera complies with Part 15 of FCC rules.

Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Warning: Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

Ordering Information

Table 19. Ordering Code

Part Number	Description
AT71XC1LV8MFERCB0	CAMELIA 8M C1 LVDS Grade E with Housing and F-Mount
AT71XC1LV8MFERCA0	CAMELIA 8M C1 LVDS Grade E with Housing and no F-Mount
AT71XC1LV8MFERAA0	CAMELIA 8M C1 LVDS Grade E without Mechanics
AT71XC1CL8MFERCB0	CAMELIA 8M C1 CameraLink Grade E with Housing and F-Mount
AT71XC1CL8MFERCA0	CAMELIA 8M C1 CameraLink Grade E with Housing and no F-Mount
AT71XC1CL8MFERAA0	CAMELIA 8M C1 CameraLink Grade E without Mechanics
AT71-LV-P2C1D1C2	LVDS-FGT Kit (see “Kits of Cable” on page 29)
AT71-LV-P8C8D8A0	Set of LVDS connectors (see “Kits of Cable” on page 29)
AT71-CL-P2C0D3A0	CL Kit (see “Kits of Cable” on page 29)

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