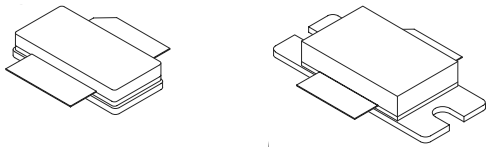
TriQuint SEMICONDUCTOR

AGR21060E
60 W, 2.110 GHz—2.170 GHz, N-Channel E-Mode, Lateral MOSFET

Introduction

The AGR21060E is a high-voltage, gold-metalized, enhancement-mode, laterally diffused metal oxide semiconductor (LDMOS) RF power transistor suitable for wideband code division multiple access (W-CDMA), single and multicarrier class AB wireless base station power amplifier applications.



AGR21060EU (unflanged) **AGR21060EF (flanged)**

Figure 1. Available Packages

Features

Typical performance for two carrier 3GPP W-CDMA systems. F1 = 2135 MHz and F2 = 2145 MHz with 3.84 MHz channel bandwidth (BW), adjacent channel BW = 3.84 MHz at F1 – 5 MHz and F2 + 5 MHz. Third-order distortion is measured over 3.84 MHz BW at F1 – 10 MHz and F2 + 10 MHz. Typical P/A ratio of 8.5 dB at 0.01% (probability) CCDF:

- — Output power: 13.5 W.
- — Power gain: 14.5 dB.
- — Efficiency: 26%.
- — IM3: –34 dBc.
- — ACPR: –37 dBc.
- — Return loss: –12 dB.

High-reliability gold-metalization process.

Low hot carrier injection (HCI) induced bias drift over 20 years.

Internally matched.

High gain, efficiency, and linearity.

Integrated ESD protection.

Device can withstand a 10:1 voltage standing wave ratio (VSWR) at 28 Vdc, 2140 MHz, 60 W continuous wave (CW) output power.

Large signal impedance parameters available.

Table 1. Thermal Characteristics

Parameter	Sym	Value	Unit
Thermal Resistance, Junction to Case:			
AGR21060EU	$R_{\theta JC}$	1.0	°C/W
AGR21060EF	$R_{\theta JC}$	1.0	°C/W

Table 2. Absolute Maximum Ratings*

Parameter	Sym	Value	Unit
Drain-source Voltage	V_{DSS}	65	Vdc
Gate-source Voltage	V_{GS}	–0.5, 15	Vdc
Total Dissipation at T_C = 25 °C:			
AGR21060EU	P_D	175	W
AGR21060EF	P_D	175	W
Derate Above 25 °C:			
AGR21060EU	—	1.0	W/°C
AGR21060EF	—	1.0	W/°C
Operating Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	–65, 150	°C

* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating*

AGR21060E	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1500	4

* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. PEAK Devices employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Electrical Characteristics

Recommended operating conditions apply unless otherwise specified: T_C = 30 °C.

Table 4. dc Characteristics

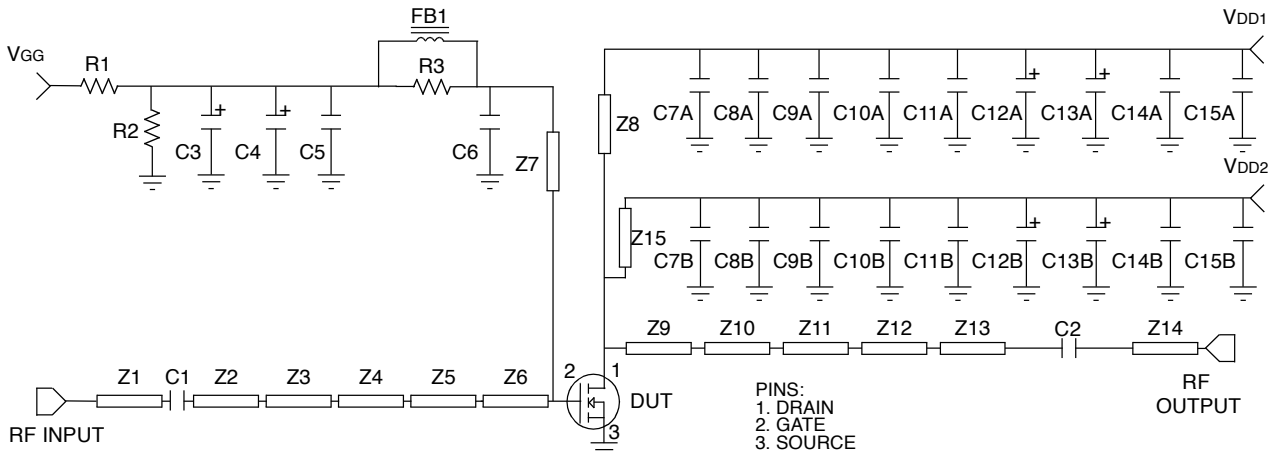
Parameter	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-source Breakdown Voltage (V_{GS} = 0, I_D = 300 μA)	$V_{(BR)DSS}$	65	—	—	Vdc
Gate-source Leakage Current (V_{GS} = 5 V, V_{DS} = 0 V)	I_{GSS}	—	—	1.8	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	—	—	100	μAdc
On Characteristics					
Forward Transconductance (V_{DS} = 10 V, I_D = 1 A)	G_{FS}	—	4.0	—	S
Gate Threshold Voltage (V_{DS} = 10 V, I_D = 180 μA)	$V_{GS(TH)}$	—	—	4.8	Vdc
Gate Quiescent Voltage (V_{DS} = 28 V, I_D = 500 mA)	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain-source On-voltage (V_{GS} = 10 V, I_D = 0.45 A)	$V_{DS(ON)}$	—	0.08	—	Vdc

Table 5. RF Characteristics

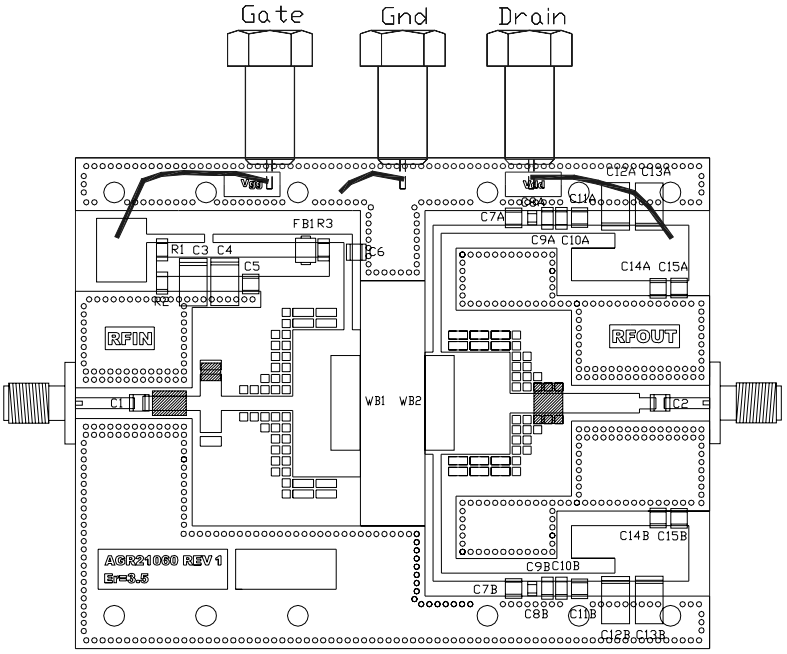
Parameter	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics					
Reverse Transfer Capacitance (V_{DS} = 28 V, V_{GS} = 0, f = 1.0 MHz) (This part is internally matched on both the input and output.)	C_{RSS}	—	1.3	—	pF
Functional Tests (in Supplied Test Fixture)					
Common-source Amplifier Power Gain*	G_{PS}	—	14.5	—	dB
Drain Efficiency*	η	—	26	—	%
Third-order Intermodulation Distortion* (IMD3 measured over 3.84 MHz BW @ f1 – 10 MHz and f2 + 10 MHz)	IM3	—	–34	—	dBc
Adjacent Channel Power Ratio* (ACPR measured over BW of 3.84 MHz @ f1 – 5 MHz and f2 + 5 MHz)	ACPR	—	–37	—	dBc
Output Power, 1 dB Compression Point (V_{DD} = 28 V, P_{OUT} = 60 W (CW), f_C = 2140.0 MHz)	P_{1dB}	—	60	—	W
Input Return Loss*	IRL	—	–12	—	dB
Output Mismatch Stress (V_{DD} = 28 V, P_{OUT} = 60 W (CW), I_{DQ} = 500 mA, f_C = 2140.0 MHz VSWR = 10:1; [all phase angles])	ψ	No degradation in output power.			

* 3GPP W-CDMA, typical P/A ratio of 8.5 dB at 0.01% CCDF, f1 = 2135.0 MHz, and f2 = 2145 MHz. V_{DD} = 28 Vdc, I_{DQ} = 500 mA, and P_{OUT} = 13.5 W avg.

Test Circuit Illustrations for AGR21060E



A. Schematic



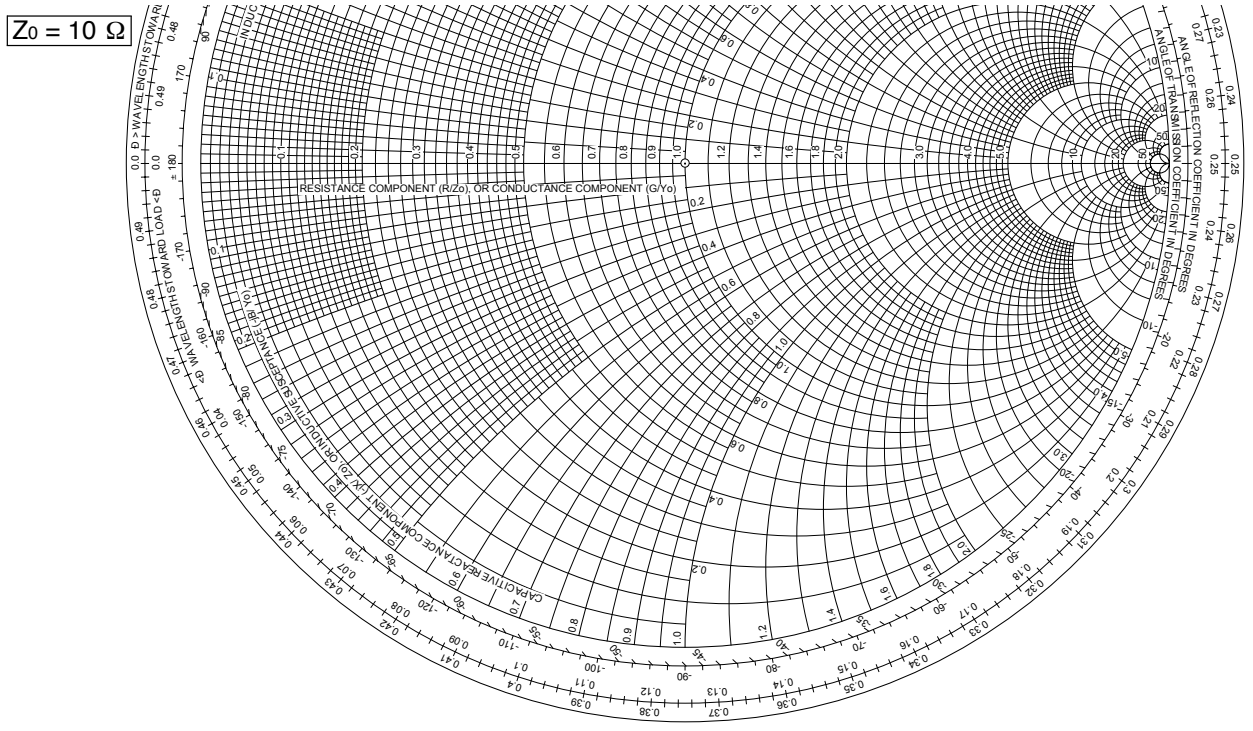
Parts List:

- Microstrip Line: Z1 0.361 in. x 0.065 in.; Z2 0.207 in. x 0.150 in.; Z3 0.085 in. x 0.087 in.; Z4 0.130 in. x 0.357 in.; Z5 0.436 in. x 0.087 in.; Z6 0.414 in. x 0.900 in.; Z7 0.424 in. x 0.050 in.; Z8 1.170 in. x 0.050 in.; Z9 0.520 in. x 0.624 in.; Z10 0.120 in. x 0.147 in.; Z11 0.180 in. x 0.250 in.; Z12 0.469 in. x 1.200 in.; Z13 0.068 in. x 0.068 in.; Z14 0.278 in. x 0.065 in.; Z15 1.170 in. x 0.050 in
- *ATC*® chip capacitor: C1, C2: 15 pF 100B150JCA500X; C6, C7: 8.2 pF 100B8R2JCA500X; C11: 1.2 pF 100B1R2JCA500X; C14, C15: 5.6 pF 100B5R6JCA500X.
- *Sprague*® tantalum surface-mount chip capacitor: C3, C4, C12, C13: 22 µF, 35 V, T491D226K035AS.
- *Vitramon*® chip capacitor: C5, C9: 22000 pF.
- 0805 size chip capacitor: C8 0.01 µF.
- 1206 size chip capacitor: C10 0.1 µF.
- 1206 size 0.25 W chip resistors: R1 1 kΩ; R2 560 kΩ; R3 4.7 Ω.
- *Fair-Rite*® ferrite bead: FB1 2743019447.
- *Taconic*® ORCER RF-35: board material, 1 oz. copper, 30 mil thickness, εr = 3.5.

B. Component Layout

Figure 2. AGR21060E Test Circuit

Typical Performance Characteristics



MHz (f)	ZS Ω (Complex Source Impedance)	ZL Ω (Complex Optimum Load Impedance)
2110 (f1)	TBD	TBD
2140 (f2)	TBD	TBD
2170 (f3)	TBD	TBD

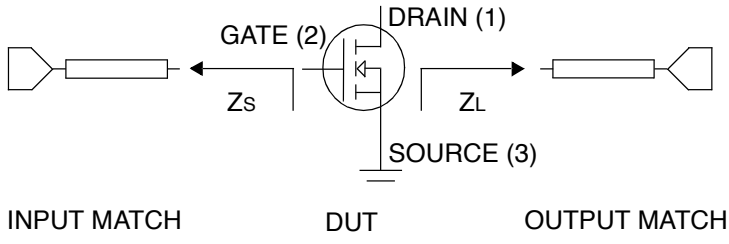
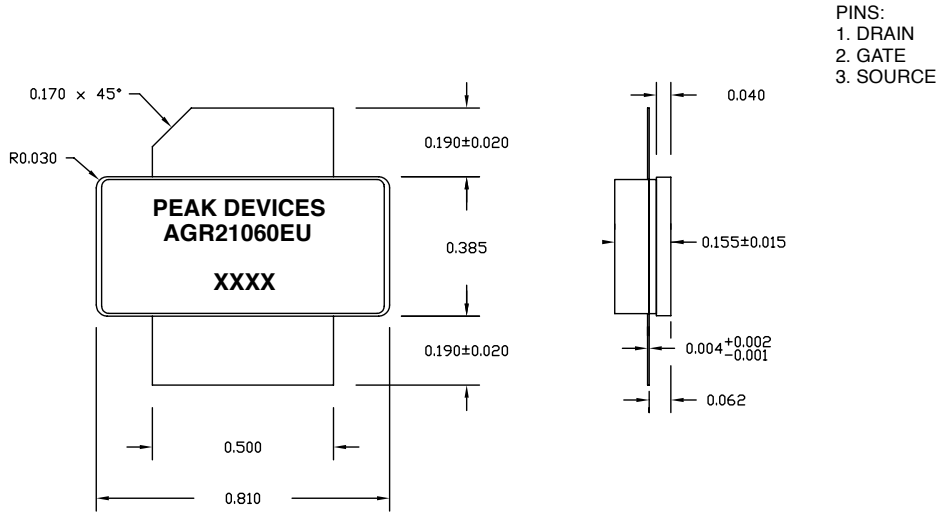


Figure 3. Series Equivalent Input and Output Impedances

Package Dimensions

All dimensions are in inches. Tolerances are ±0.005 in. unless specified.

AGR21060EU



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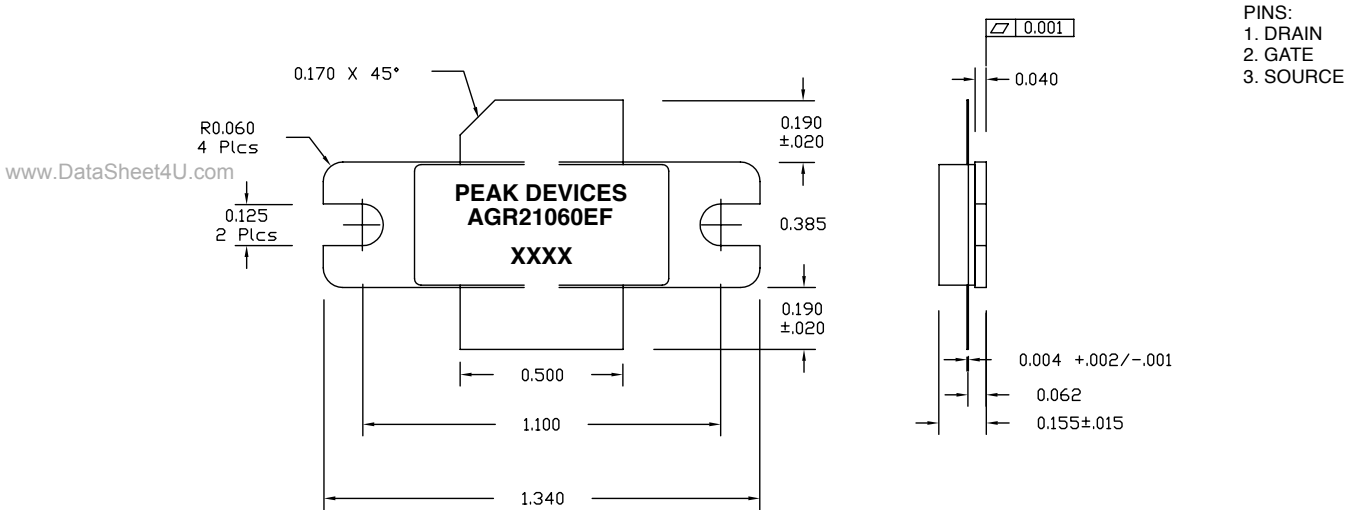

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