

74AC573 • 74ACT573

Octal Latch with 3-STATE Outputs

General Description

The 74AC573 and 74ACT573 are high-speed octal latches with buffered common Latch Enable (LE) and buffered common Output Enable (\overline{OE}) inputs.

The 74AC573 and 74ACT573 are functionally identical to the 74AC373 and 74ACT373 but with inputs and outputs on opposite sides.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 74AC373 and 74ACT373
- 3-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 74ACT573 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74AC573SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC573SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC573MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC573PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT573SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT573SCX_NL (Note 1)	M20B	Pb-Free 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT573SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT573MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT573PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

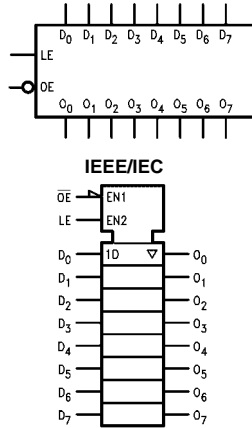
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

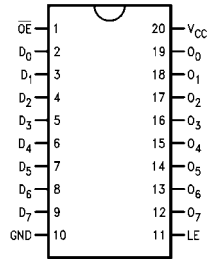
FACT™ is a trademark of Fairchild Semiconductor Corporation.

74AC573 • 74ACT573 Octal Latch with 3-STATE Outputs

Logic Symbols



Connection Diagram



Pin Descriptions

Pin Names	Description
D ₀ -D ₇	Data Inputs
LE	Latch Enable Input
\overline{OE}	3-STATE Output Enable Input
O ₀ -O ₇	3-STATE Latch Outputs

Truth Table

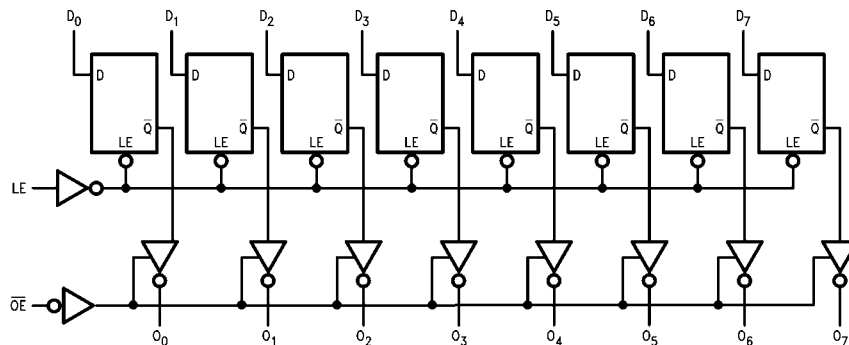
Inputs			Outputs
\overline{OE}	LE	D	O _n
L	H	H	H
L	H	L	L
L	L	X	O ₀
H	X	X	Z

H = HIGH Voltage
 L = LOW Voltage
 Z = High Impedance
 X = Immaterial
 O₀ = Previous O₀ before HIGH-to-LOW transition of Latch Enable

Functional Description

The 74AC573 and 74ACT573 contain eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D-type input changes. When LE is LOW the latches store the information that was present on the D-type inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are enabled. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J) (PDIP)	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 2: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12$ mA $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 3)
		4.5		3.86	3.76		
		5.5		4.86	4.76		
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 3)
		4.5		0.36	0.44		
		5.5		0.36	0.44		
I_{IN} (Note 4)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}, GND$
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}	Output Current (Note 5)	5.5			-75	mA	$V_{OHD} = 3.85V$ Min
I_{CC} (Note 4)	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum 3-STATE Leakage Current	5.5		± 0.25	± 2.5	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}, GND$ $V_O = V_{CC}, GND$

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

Note 5: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V) (Note 6)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PHL}	Propagation Delay	3.3	0.5	8.5	10.5	2.5	11.0	ns
t _{PLH}	D _n to O _n	5.0	1.5	5.5	7.0	1.5	7.5	
t _{PLH}	Propagation Delay	3.3	2.5	8.5	12.0	2.5	12.5	ns
t _{PHL}	LE to O _n	5.0	2.0	6.0	8.0	2.0	8.5	
t _{PZL}	Output Enable Time	3.3	2.5	8.5	13.0	2.5	13.5	ns
t _{PZH}		5.0	1.5	6.0	8.5	1.5	9.0	
t _{PHZ}	Output Disable Time	3.3	1.0	9.0	14.5	1.0	15.0	ns
t _{PLZ}		5.0	1.0	6.0	9.5	1.0	10.0	

Note 6: Voltage Range 5.0 is 5.0V ± 0.5V

Voltage Range 3.3 is 3.3V ± 0.3V

AC Operating Requirements for AC

Symbol	Parameter	V _{CC} (V) (Note 7)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF	Units
			Typ	Guaranteed Minimum		
t _S	Setup Time, HIGH or LOW	3.3	0	3.0	3.0	ns
	D _n to LE	5.0	0	3.0	3.0	
t _H	Hold Time, HIGH or LOW	3.3	0	1.5	1.5	ns
	D _n to LE	5.0	0	1.5	1.5	
t _W	LE Pulse Width, HIGH	3.3	2.0	4.0	4.0	ns
		5.0	2.0	4.0	4.0	

Note 7: Voltage Range 5.0 is 5.0V ± 0.5V

Voltage Range 3.3 is 3.3V ± 0.3V

DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V _{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} - 0.1V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA I _{OH} = -24 mA (Note 8)	
V _{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA I _{OL} = 24 mA (Note 8)	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND	
I _{OZ}	Maximum 3-STATE Leakage Current	5.5		±0.25	±2.5	μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND	
I _{CC}	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	V _I = V _{CC} - 2.1V	
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max	
I _{OHD}	Output Current (Note 9)	5.5			-75	mA	V _{OHD} = 3.85V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V _{IN} = V _{CC} or GND	

Note 8: All outputs loaded; thresholds on input associated with output under test.

Note 9: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V) (Note 10)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay D _n to O _n	5.0	2.5	6.0	10.5	2.0	12.0	ns
t _{PHL}	Propagation Delay LE to O _n	5.0	3.0	6.0	10.5	2.5	12.0	ns
t _{PHL}	Propagation Delay LE to O _n	5.0	2.5	5.5	9.5	2.0	10.5	ns
t _{PZH}	Output Enable Time	5.0	2.0	5.5	10.0	1.5	11.0	ns
t _{PZL}	Output Enable Time	5.0	1.5	5.5	9.5	1.5	10.5	ns
t _{PHZ}	Output Disable Time	5.0	2.5	6.5	11.0	1.5	12.5	ns
t _{PLZ}	Output Disable Time	5.0	1.5	5.0	8.5	1.0	9.5	ns

Note 10: Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for ACT

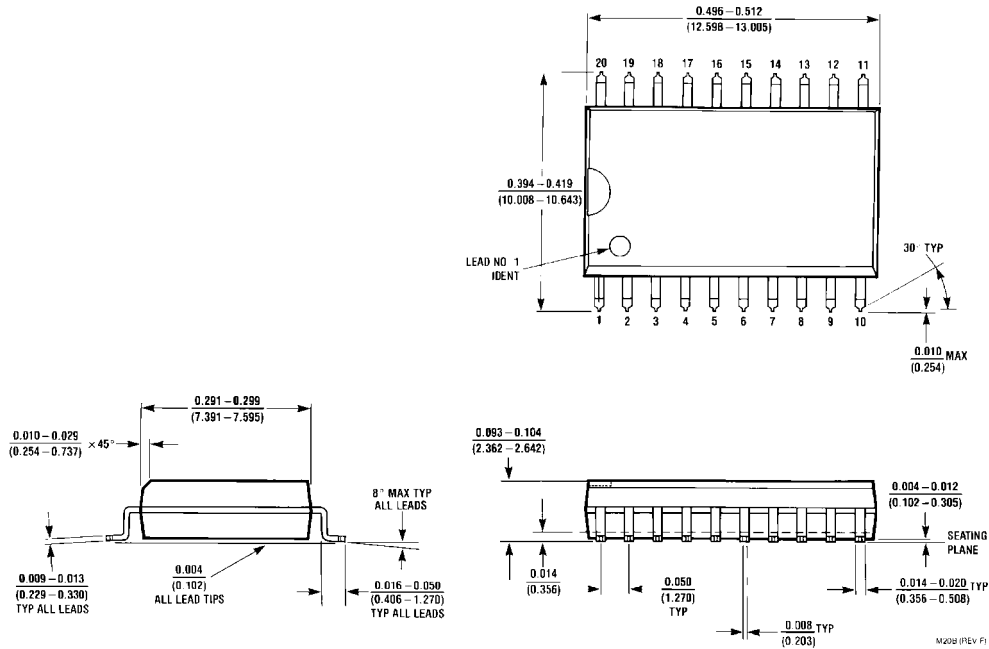
Symbol	Parameter	V _{CC} (V) (Note 11)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF	Units
			Typ	Guaranteed Minimum		
t _S	Setup Time, HIGH or LOW D _n to LE	5.0	1.5	3.0	3.5	ns
t _H	Hold Time, HIGH or LOW D _n to LE	5.0	-1.5	0	0	ns
t _W	LE Pulse Width, HIGH	5.0	2.0	3.5	4.0	ns

Note 11: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

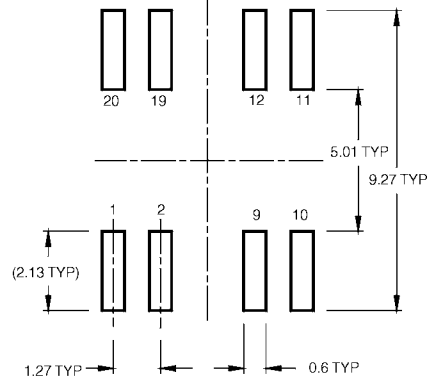
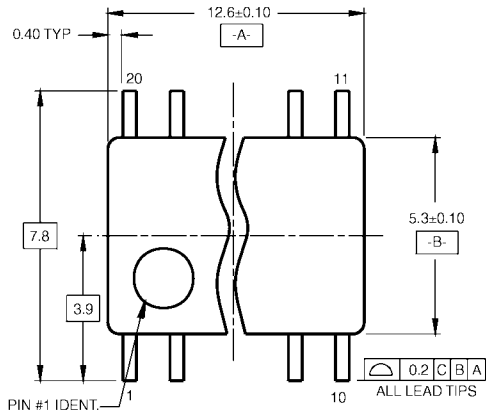
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	5.0	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance for AC for ACT	25.0	pF	V _{CC} = 5.0V
		42.0		

Physical Dimensions inches (millimeters) unless otherwise noted

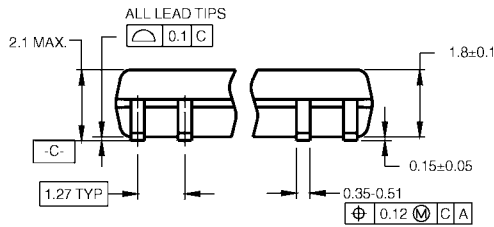


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

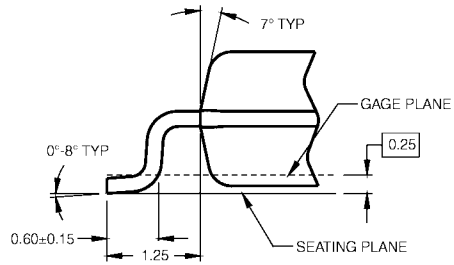
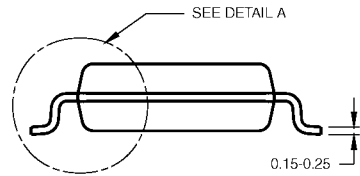
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



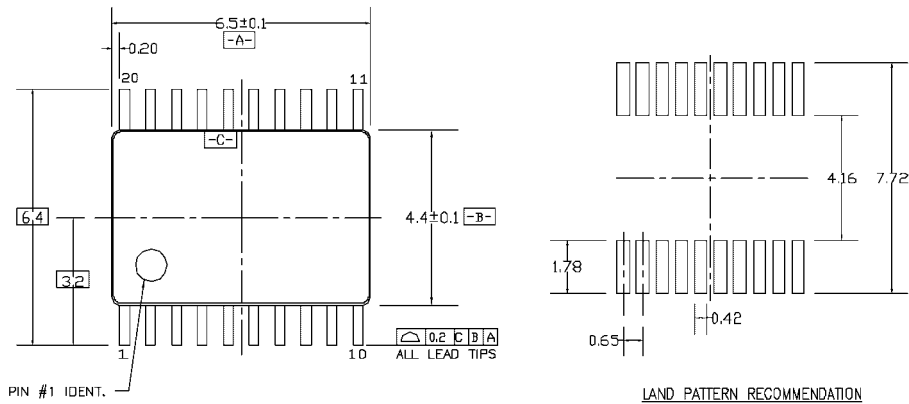
DETAIL A

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

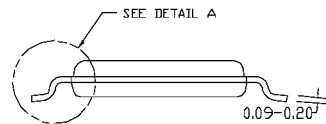
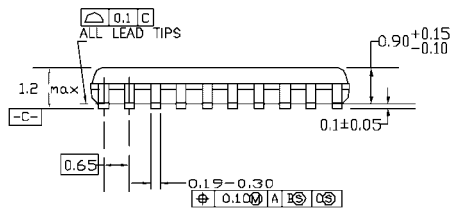
Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

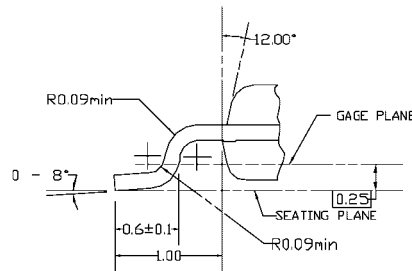


PIN #1 IDENT.

LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

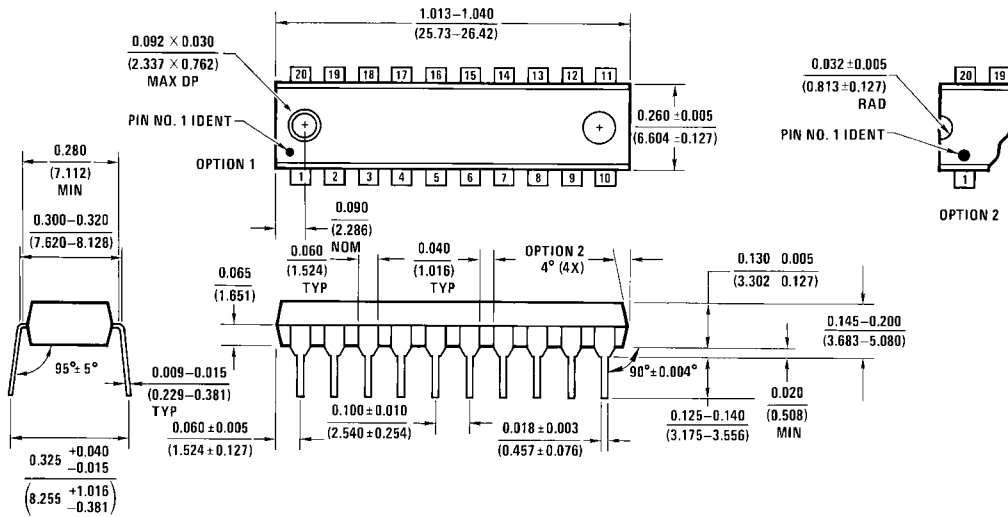
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com