PRELIMINARY DATA SHEET

NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT

# μPD16406

## SOURCE DRIVER FOR TFT LCD PANEL (120-OUTPUT HOLIZONTAL DRIVER)

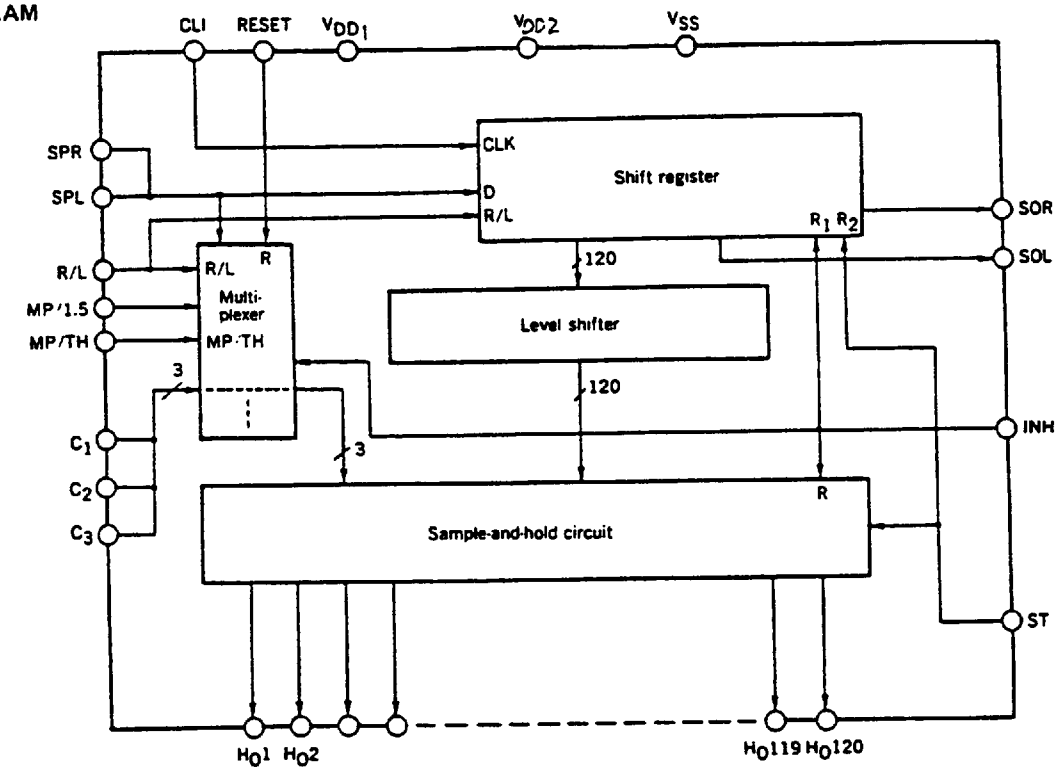
The μPD16406 is a horizontal (source) driver for TFT LCD panel. It contains two sample-and-hold circuits; it is optimum as the horizontal driver for linear sequential scanning color LCD TV. The shift clock circuit and output driver circuit are designed considering low power consumption.

The μPD16406 can drive a TFT LCD panel when combined with vertical (gate) driver μPD16402 or μPD16404.

### FEATURES

- Operating clock frequency: Max. 15 MHz
- Number of output pins: 120
- Supply voltage ($V_{DD2}$): Absolute maximum rating of 23 V
- Difference between pin outputs: Max. ± 50 mV
- Cascade connection enabled
- Selection of stripe, mosaic, or delta layout
- Structure: CMOS (low power consumption)

### BLOCK DIAGRAM



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## ORDER INFORMATION

| Part No. | Package | Quarity Grade |
|---|---|---|
| uPD16406N-xxx | TCP(TAB Package) | Standard |

## ABSOLUTE MAXIMUM RATINGS ($T_a$=25±2℃, $V_{SS}$=0V)

| | | | | |
|---|---|---|---|---|
| Supply Voltage | $V_{DD2}$ | -0.5 to 23 | V | |
| Supply Voltage | $V_{DD1}$ | -0.5 to 7 | V | |
| Input Voltage | $V_I$ | -0.5 to $V_{DD2}$+0.5 | V | Video Input pins |
| Input Voltage | $V_C$ | -0.5 to $V_{DD1}$+0.5 | V | Control Input (Logic) pins |
| Input Current | $I_I$ | ±10 | mA | |
| Output Current | $I_O$ | ±5 | mA | |
| Operating Temperature | $T_{opt}$ | -40 to +85 | ℃ | |
| Storage Temperature | $T_{stg}$ | -65 to +125 | ℃ | |

## RECOMMENDED OPERATING CONDITIONS ($V_{SS}$=0V)

| ITEM | SYMBOL | MIN. | TYP. | MAX. | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD1}$ | 4.5 | 5.0 | 5.5 | V | |
| Supply Voltage | $V_{DD2}$ | 12 | | 18 | V | |

ELECTRICAL CHARACTERISTICS ($T_a$ = 0 to 70 °C, $V_{DD2}$ = 15 V, $V_{DD1}$ = 5 V, $V_{SS}$ = 0 V)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| Video signal maximum output voltage | $V_{VOH}$ | $V_{DD2}$ – 2 | | | V | $V_{VI}$ = $V_{DD2}$ |
| Video signal minimum output voltage | $V_{VOL}$ | | | 2.5 | V | $V_{VI}$ = 0 V |
| SO pin high-level output voltage | $V_{POH}$ | $V_{DD1}$ –0.05 | | $V_{DD1}$ | V | |
| SO pin low-level output voltage | $V_{POL}$ | 0 | | 0.05 | V | |
| Control signal high-level input voltage | $V_{IH}$ | 3.5 | | $V_{DD1}$ | V | |
| Control signal low-level input voltage | $V_{IL}$ | 0 | | 1.5 | V | |
| Video signal high-level output voltage | $I_{VOH1}$ | –13 | –8 | –2 | μA | INH = "L"<br>$V_{of}$ = 6 V, $V_o$ = 8 V |
| Video signal high-level output voltage | $I_{VOH2}$ | | –0.7 | –0.3 | mA | INH = "H"<br>$V_{of}$ = 10 V |
| Video signal low-level output voltage | $I_{VOL}$ | 1 | 2.5 | | mA | INH = "L"<br>$V_{of}$ = 11 V, $V_o$ = 8 V |
| SO pin high-level output current | $I_{POH}$ | | –5 | –2 | mA | $V_o$ = 4 V |
| SO pin low-level output current | $I_{POL}$ | 2 | 5 | | mA | $V_o$ = 1 V |
| Voltage difference between video signal outputs | $\Delta V_{VO1}$ | | | ± 50 | mV | $V_{VI}$ = 2.5 V,<br>$T_a$ = 25 °C |
| Voltage difference between video signal outputs | $\Delta V_{VO2}$ | | | ± 50 | mV | $V_{VI}$ = 7.5 V,<br>$T_a$ = 25 °C |
| Voltage difference between video signal outputs | $\Delta V_{VO3}$ | | | ± 50 | mV | $V_{VI}$ = 12.5 V,<br>$T_a$ = 25 °C |
| Control pin input leakage current | $I_{LC}$ | | | ±1 | μA | |
| Video input pin input leakage current | $I_{VC}$ | | | ±10 | μA | |
| Control pin input capacity | $C_{CI1}$ | | 11 | | pF | Exact of SP pin, $T_a$ = 25 °C |
| Control pin input capacity | $C_{CI2}$ | | 28 | | pF | SP pin only $T_a$ = 25 °C |
| Video pin input capacity | $C_{VON}$ | | 24 | 50 | pF | $V_{VI}$ = 7.5 V |
| Supply current | $I_{DD1}$ | | 3.2 | 5.0 | mA | f = 4 MHz,<br>$V_I$ = 7.5 V |
| Supply current | $I_{DD2}$ | | 1.8 | 3.6 | mA | f = 4 MHz,<br>INH = "H" |
| Supply current | $I_{CC1}$ | | 0.5 | 2.5 | mA | f = 4 MHz |
| Supply current | $I_{CC2}$ | | 0.2 | 0.5 | mA | f = 4 MHz, $C_L$ = 50 pF<br>INH = "H" |
| Operating clock frequency | $f_{OP}$ | | | 15 | MHz | |
| CLI – SO propagation delay | $t_{PHL}$, $t_{PLH}$ | | | 46 | ns | |
| Setup time | $t_{SU}$ | 20 | | | ns | |
| Hold time | $t_h$ | 20 | | | ns | |

## PIN FUNCTIONS

| PIN NAME | SIGNAL LEVEL | PIN FUNCTION | DESCRIPTION |
|---|---|---|---|
| $C_1$, $C_2$, $C_3$ | IA | Video signal input pins | These pins are used to input video signals (R, G, and B). Input video signals are sent to the sample-and-hold circuit through the multiplexer. Then, these signals are output from video signal output pins $H_o1$ to $H_o120$. |
| $H_o1$ to $H_o120$ | OA | Video signal output pins | These pins are used to output video signals. Video signals input from $C_1$, $C_2$, and $C_3$ pins are output to these pins via the sample-and-hold circuit. These pins are connected to the TFT (Thin Film Transistor) source. |
| SPR, SPL | IC | Horizontal start pulse input pins | These pins are used to input start pulses of the shift register for generating sample-and-hold timings.<br>SPR: Inputs a start pulse at right shift.<br>SPL: Inputs a start pulse at left shift.<br>(Note: These pins are held open when not in use.) |
| CLI | IC | Shift clock input pin | This pin is used to input a shift register transfer clock. |
| RESET | IC | Reset signal input pin | When the level of this pin becomes high, the selection counter and sample-and-hold switching counter is reset. |
| INH | IC | Inhibit signal input pin | When the level of this pin becomes high, the levels of pins $H_o1$ to $H_o120$ are made high, the output load (TFT panel) is precharged, and the shift register is reset.<br>The inhibit signal is used sent to the multiplexer circuit (selection counter) and sample-and-hold circuit (control clock). States of these circuit change at the rising edge of the inhibit signal. |
| ST | IC | Power saving signal input pin | This pin is used to input a power saving signal.<br>When the level of this pin becomes high, video output pin levels are made high, the output buffer operating current is reduced, and the shift register is reset (stopped). If the power saving input signal is input during the vertical blanking period, current consumption can be reduced. |
| SOR, SOL | OC | Next horizontal driver start pulse output pins | These pins are used to output a shift register transfer end signal. When the driver is connected to the cascade, these pins are connected to the SP pins of the next driver.<br>SOR: Outputs a shift end signal at right shift.<br>SOL: Outputs a shift end signal at left shift.<br>(Note: These pins are held open when not in use.) |
| MP/TH | IC | Multiplexer circuit switching pin (1) | Mode / MP/TH / MP/1.5<br>Mosaic layout (1-pixel shift) / H / L<br>Delta layout (1.5-pixel shift) / H / H<br>Stripe layout (fixed) / L / L |
| MP/1.5 | IC | Multiplexer circuit switching pin (2) | |
| R/L | IC | Right/left shift selection pin | This pin is used for selecting right or left shift.<br>Right shift ($H_o1 \rightarrow H_o120$): "H"<br>Left shift ($H_o120 \rightarrow H_o1$): "L" |
| $V_{DD1}$ | – | Logic power supply pin | Supply +5 V (standard voltage). |
| $V_{DD2}$ | – | Driver Power Supply | Supply +15 V (standard voltage). |
| | – | | Supply +15 V (standard voltage). |
| $V_{SS}$ | – | Ground pin | Connect this pin to the system ground. |
| | – | | Connect this pin to the system ground. |

Notes: Signal levels are as follows:

IC --------Logic input signal. $V_{DD1}$: H-level $V_{SS}$: L-level
IA --------Video input signal. Voltage range: $V_{SS}$ to $V_{DD2}$
OC --------Logic output signal. $V_{DD1}$: H-level $V_{SS}$: L-level
OA --------Video output signal.
MP/TH ---Selection of through Mode
MP/1.5 ----Selection of delta Mode

## FUNCTIONS

1. Multiplexer Circuit

Video signals (R, G, and B) input to pins $C_1$, $C_2$, and $C_3$ are switched according to the LC pixel layout, then output pins $H_o1$ to $H_o120$. A stripe, mosaic, or delta layout mode can be selected according to the combination of signal levels of MP/TH and MP/1.5 pins.

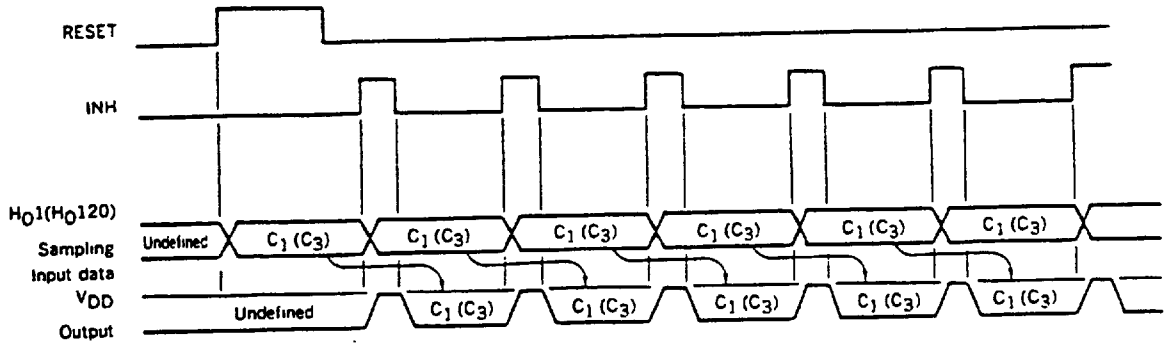
(1) Stripe layout mode ⇨ MP/TH pin —— L-level
Stripe layout is selected. MP/1.5 pin —— L-level
The multiplexer circuit is made through.

Output states (operation table)

| Line No. | Pin name | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | RESET | INH  | $H_o1$ ($H_o120$) | $H_o2$ ($H_o119$) | $H_o3$ ($H_o118$) | ··· | $H_o119$ ($H_o2$) | $H_o120$ ($H_o1$) |
| – | "H" |  | Sampling $C_1$ ($C_3$) | Sampling $C_2$ ($C_2$) | Sampling $C_3$ ($C_1$) | ··· | Sampling $C_2$ ($C_3$) | Sampling $C_3$ ($C_1$) |
| 1 | "L" |  | Output $C_1$ ($C_3$) | Output $C_2$ ($C_2$) | Output $C_3$ ($C_1$) | ··· | Output $C_2$ ($C_3$) | Output $C_3$ ($C_1$) |
| 2 | "L" |  | Output $C_1$ ($C_3$) | Output $C_2$ ($C_2$) | Output $C_3$ ($C_1$) | ··· | Output $C_2$ ($C_3$) | Output $C_3$ ($C_1$) |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |

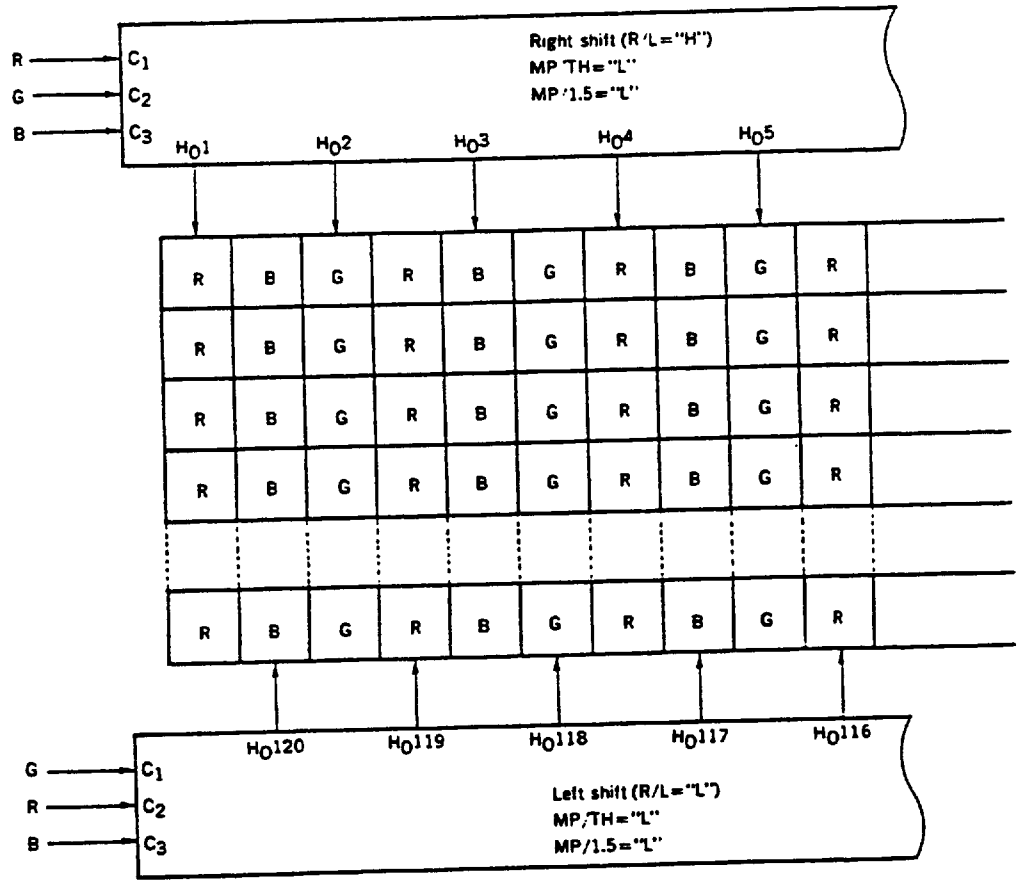
This table indicates output states in the right shift mode. Pin numbers in ( ) indicate output states in the right shift mode.

### Timing Chart in Stripe Layout Mode




For pins other than $H_O1$ ($H_O120$), the timings are the same. For data, see the above operation table (output states).

### Example of Multiplexer Operation in Stripe Layout Mode



(2) Mosaic layout mode ⇨ MP/TH pin H-level
MP/1.5 pin L-level

A mosaic mode (1-pixel shift) may be selected.

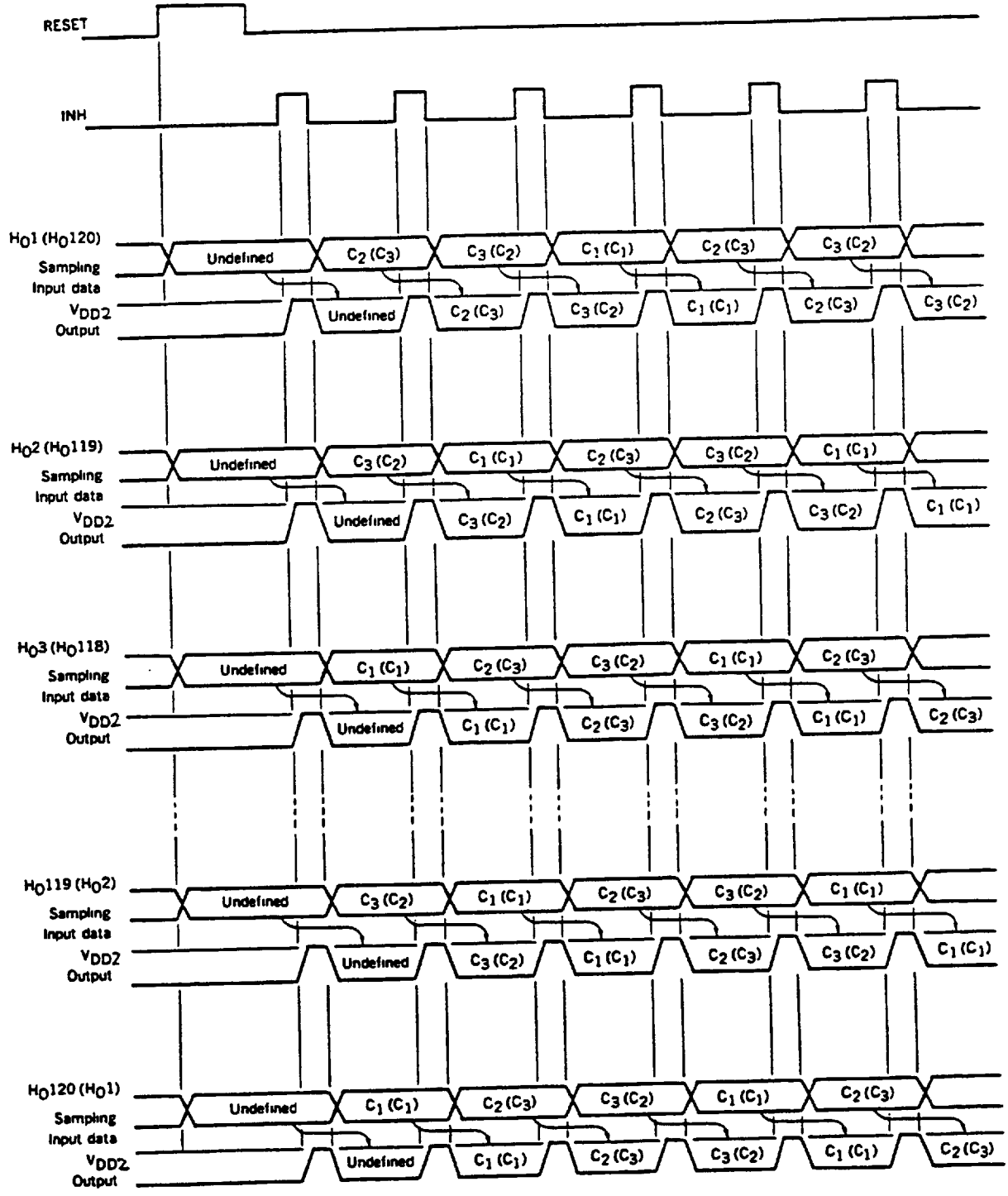
Output states (operation table)

| Line No. | Pin name | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | RESET | INH  | $H_o1$ ($H_o120$) | $H_o2$ ($H_o119$) | $H_o3$ ($H_o118$) | ··· | $H_o119$ ($H_o2$) | $H_o120$ ($H_o1$) |
| – | "H" |  | Undefined | ← | ← | ··· | ← | ← |
| 1 | "L" |  | Sampling $C_2$ ($C_3$) | Sampling $C_3$ ($C_2$) | Sampling $C_1$ ($C_1$) | ··· | Sampling $C_3$ ($C_2$) | Sampling $C_1$ ($C_1$) |
| 2 | "L" |  | Output $C_2$ ($C_3$) | Output $C_3$ ($C_2$) | Output $C_1$ ($C_1$) | ··· | Output $C_3$ ($C_2$) | Output $C_1$ ($C_1$) |
| 3 | "L" |  | Output $C_3$ ($C_2$) | Output $C_1$ ($C_1$) | Output $C_2$ ($C_3$) | ··· | Output $C_1$ ($C_1$) | Output $C_3$ ($C_3$) |
| 4 | "L" |  | Output $C_1$ ($C_1$) | Output $C_2$ ($C_3$) | Output $C_3$ ($C_2$) | ··· | Output $C_2$ ($C_3$) | Output $C_3$ ($C_2$) |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |

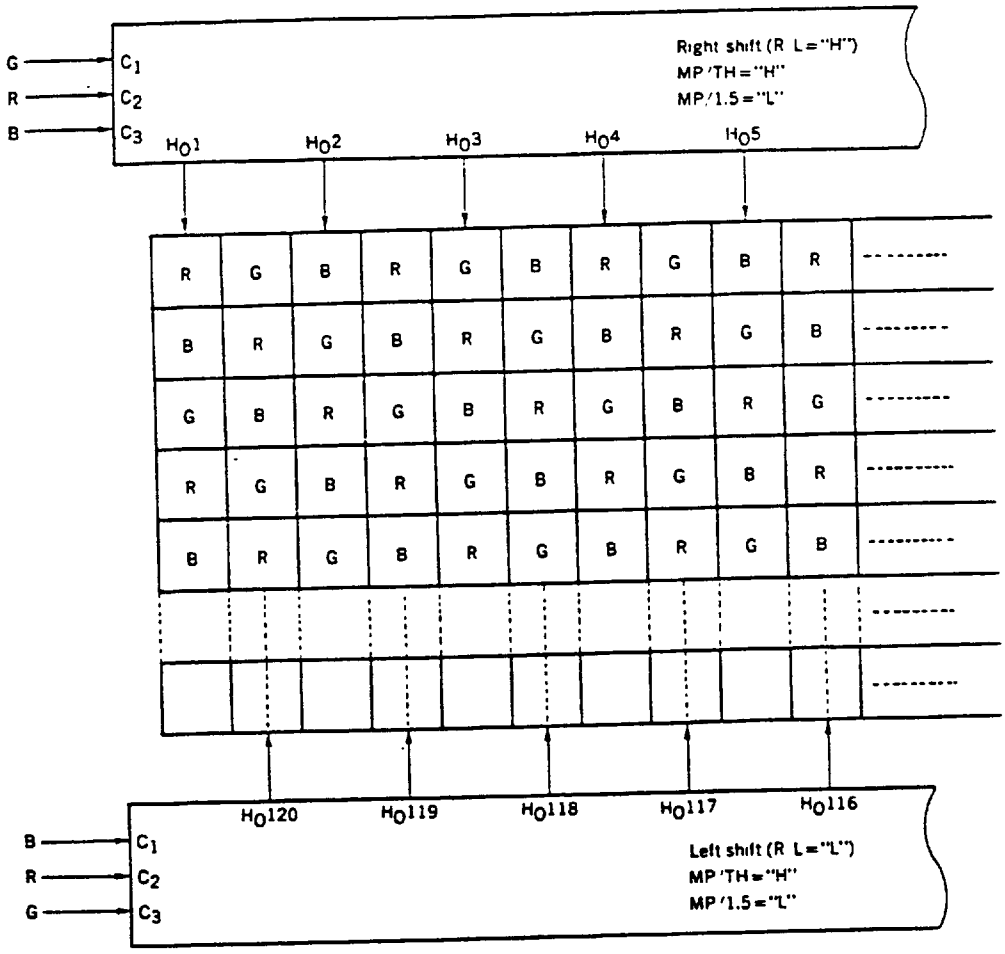
Note: The multiplexer circuit is initialized by a RESET signal.

This table indicates output states in the right shift mode. Pin numbers in ( ) indicate output states in the right shift mode.

Timing Chart in Mosaic Layout Mode



Example of Operation of Multiplexer in Mosaic Layout Mode



(3) Delta layout mode ⇨ MP/TH pin H-level
MP/1.5 pin H-level

A delta mode (half pixel shift) may be selected.

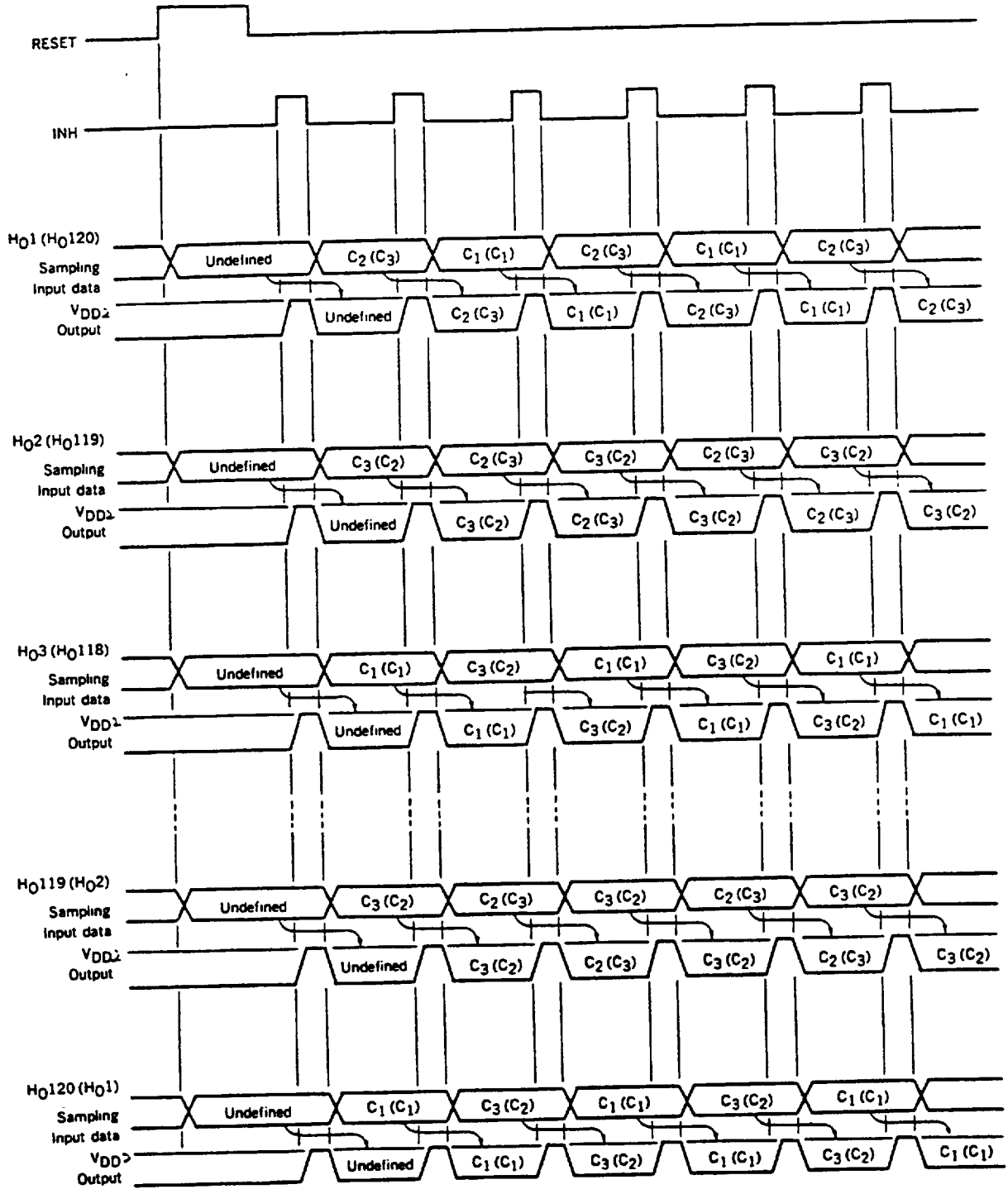
Output states (operation table)

| Line No. | Pin name | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | RESET | INH | $H_o1$ ($H_o120$) | $H_o2$ ($H_o119$) | $H_o3$ ($H_o118$) | ··· | $H_o119$ ($H_o2$) | $H_o120$ ($H_o1$) |
| – | "H" | L | Undefined | ← | ← | ··· | ← | ← |
| 1 | "L" | ⊓ | Sampling $C_2$ ($C_3$) | Sampling $C_3$ ($C_2$) | Sampling $C_1$ ($C_1$) | ··· | Sampling $C_3$ ($C_2$) | Sampling $C_1$ ($C_1$) |
| 2 | "L" | ⊓⊓ | Output $C_2$ ($C_3$) | Output $C_3$ ($C_2$) | Output $C_1$ ($C_1$) | ··· | Output $C_3$ ($C_2$) | Output $C_1$ ($C_1$) |
| 3 | "L" | ⊓⊓⊓ | Output $C_1$ ($C_1$) | Output $C_2$ ($C_3$) | Output $C_3$ ($C_2$) | ··· | Output $C_2$ ($C_3$) | Output $C_3$ ($C_2$) |
| 4 | "L" | ⊓⊓⊓⊓ | Output $C_2$ ($C_3$) | Output $C_3$ ($C_2$) | Output $C_1$ ($C_1$) | ··· | Output $C_3$ ($C_2$) | Output $C_1$ ($C_1$) |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |

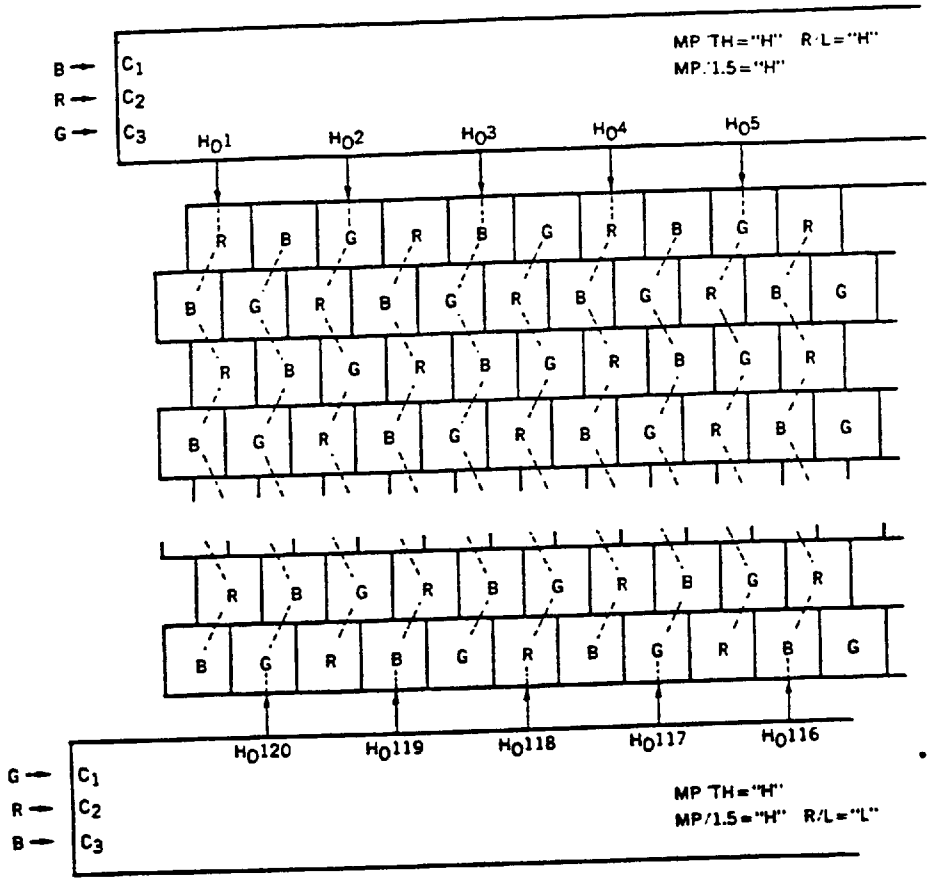
Note: The multiplexer circuit is initialized by a RESET signal.

This table indicates output states in the right shift mode. Pin numbers in ( ) indicate output states in the right shift mode.

Timing Chart for Delta Mode



Example of Operation of Multiplexer in Delta Layout Mode



2. Sample-and-hold Circuit

In the sample-and-hold circuit, video signals $C_1$ and $C_2$ are sampled from video signals $C_1$, $C_2$, and $C_3$ (see the explanation of the multiplexer circuit) by the signal sent from the shift register and $SW_{a1}$ and $SW_{a2}$ signals controlled by the binary signal (F/F) (that is reset by the RESET signal and changes at the rising edge of the INH signal). The sampled video signals are switched by $SW_{b1}$ and $SW_{b2}$ signals at the rising edge of the INH signal and sent to the succeeding circuit.

In the output circuit, the TFT is discharged by the $SW_c/SW_d$ signal. When the INH signal level becomes low, the $SW_c/SW_d$ signal is turned off, the TFT is charged by $I_{VOH}$, and video signals are output. Since the load is charged by $I_{VOH}$ after it is discharged by $I_{VOL2}$ and $I_{VOL1}$, $I_{VOL1}$ may be used as the buffer idling current during the output period, which contributing power saving.

3. Shift Register Circuit

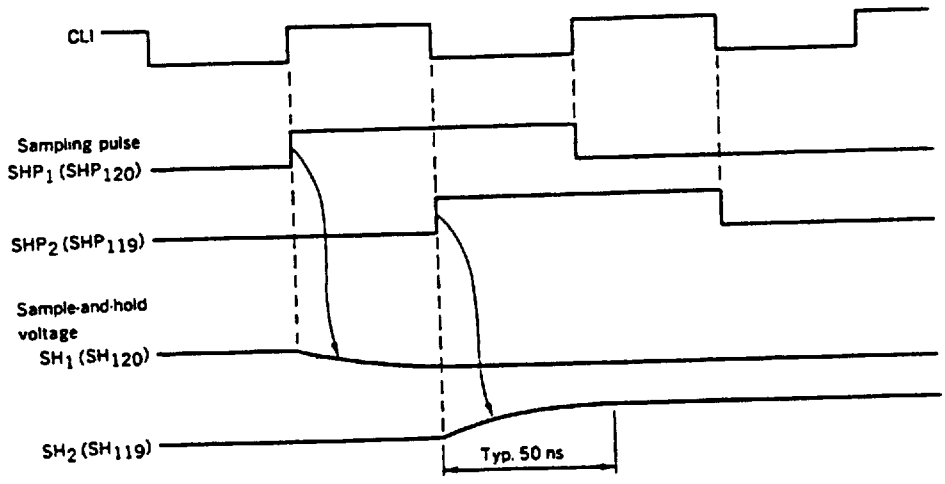
Video signal sampling timing pulses are generated to control the sample-and-hold circuit.

Shift pulses input from the SP pin are sequentially shifted by the shift clock pulses input to the CLI pin. Thus, sample-and-hold timing pulses are generated. A start pulse is output from the SO pin to the next driver which is connected between the SO pin and cascade.

If another driver is selected, issue of shift clock pulses stops to save power.

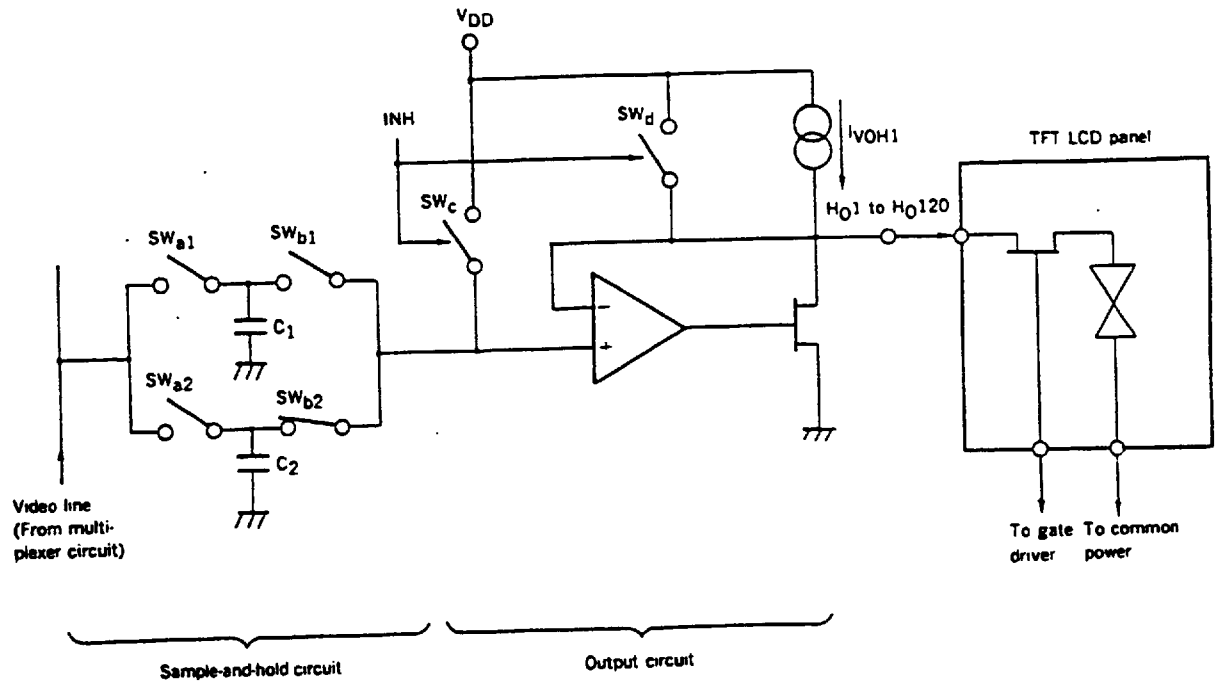
Sample-and-hold pulses are shifted every 1/2 cycle of the clock input to the CLI pin. It takes several tens of nanoseconds to charge the sample-and-hold circuit via the video line and data is sampled and held at almost all clock pulse change points. That is, shift clock pulses can be halved, reducing current consumption.

Sample-and-hold Timing

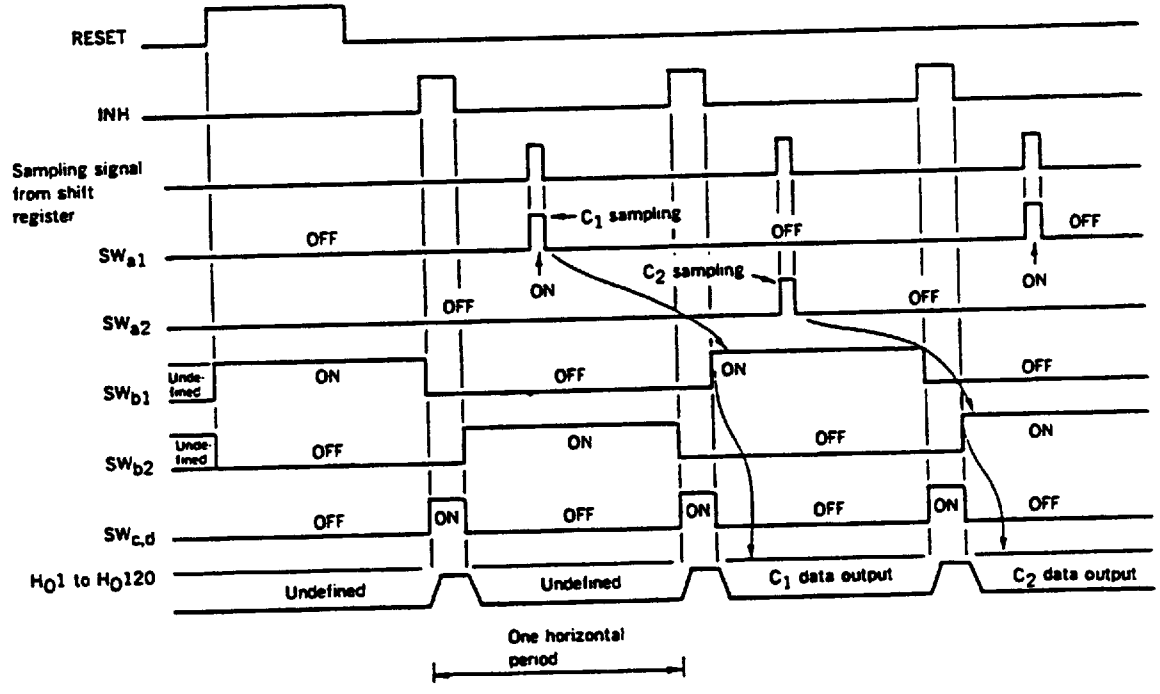



This chart indicates sample-and-hold timings in the right shift mode. Pin numbers in ( ) indicate sample-and-hold timings in the right shift mode.

## Sample-and-hold Circuit and Output Circuit

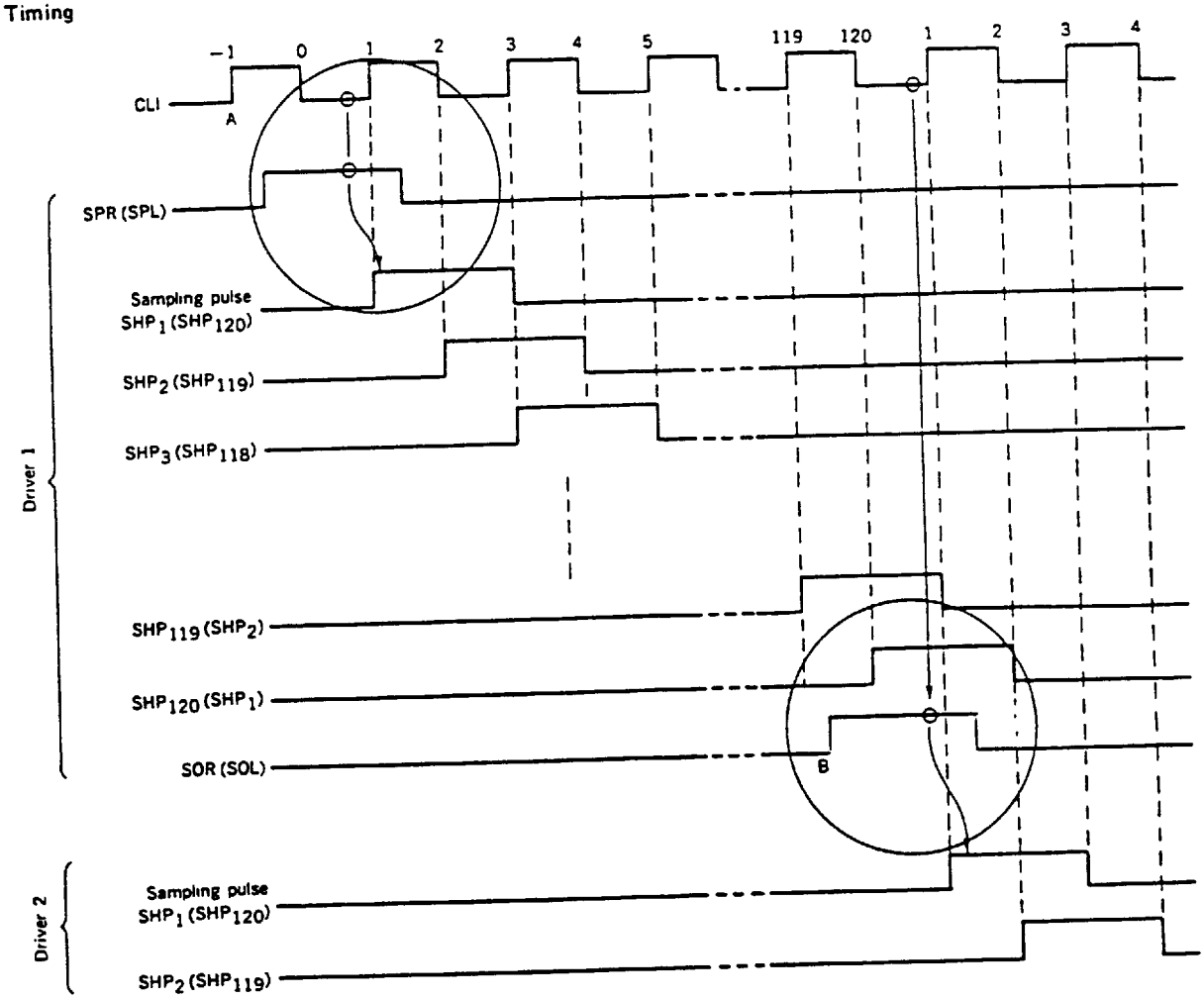



## Timing Chart

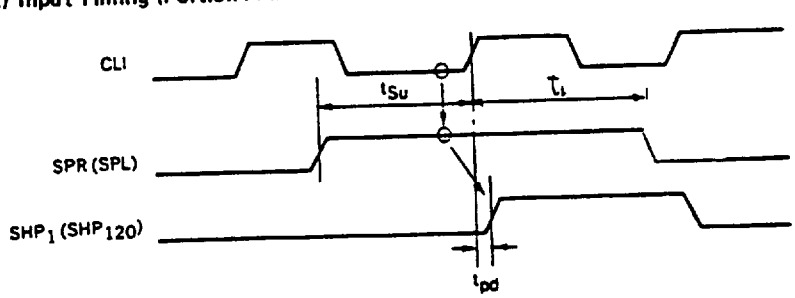


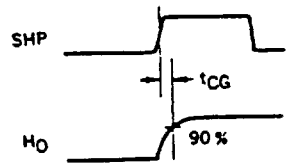

Note: $C_1$ and $C_2$ sample-and-hold switching signals $SW_a/SW_b$ are controlled by the binary signal (F/F) that is reset by the RESET signal and changes at the rising edge of the INH signal.

Shift Timing

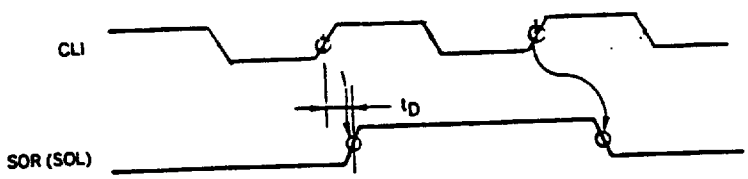



SPR (SPL) Input Timing (Portion A in the above shift timing chart)



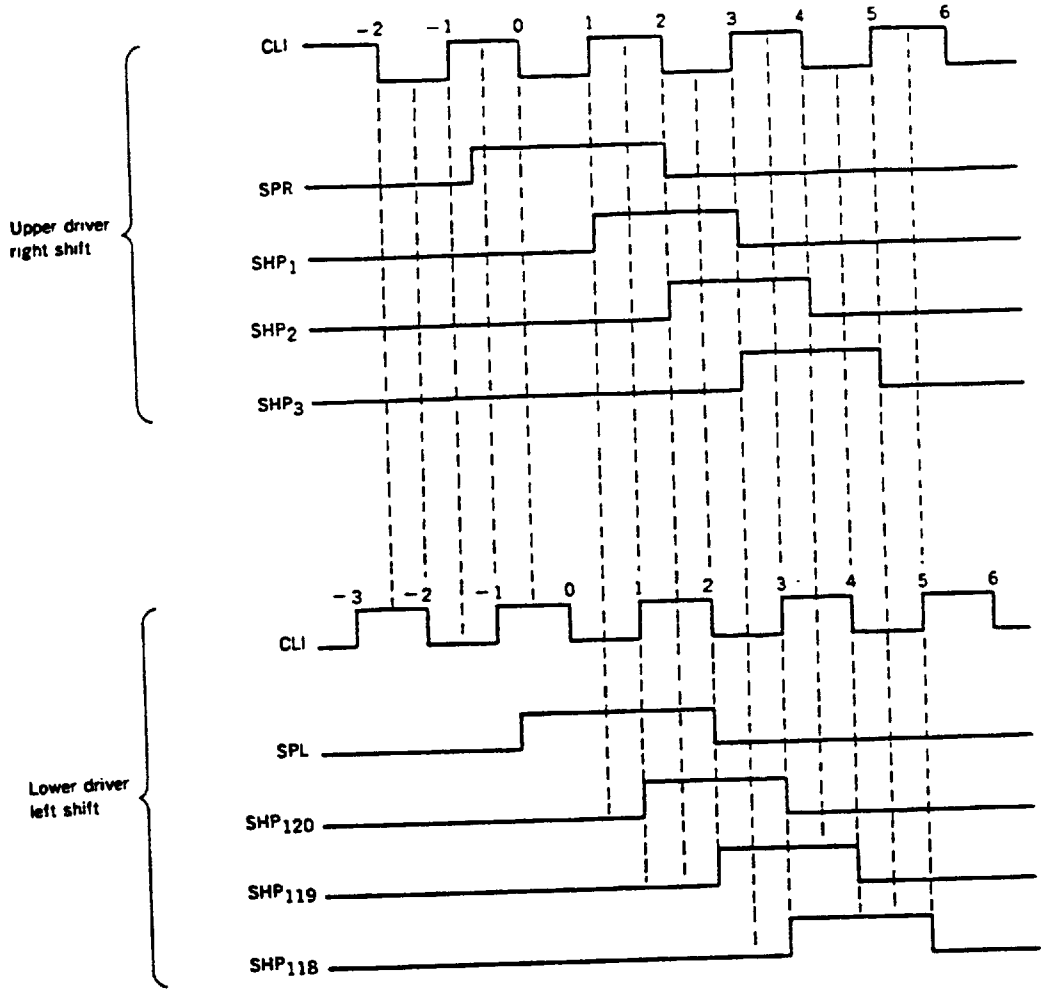



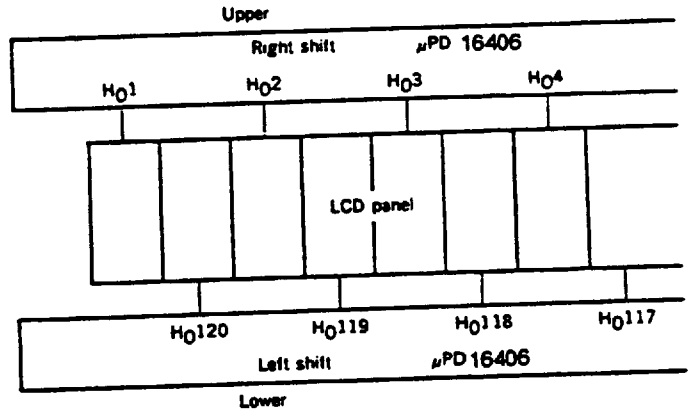

Sampling and charge time




SOR (SOL) Output Timing (Portion B in the above shift timing chart)

**Comb Connection (Upper and lower drivers) Shift Timing**

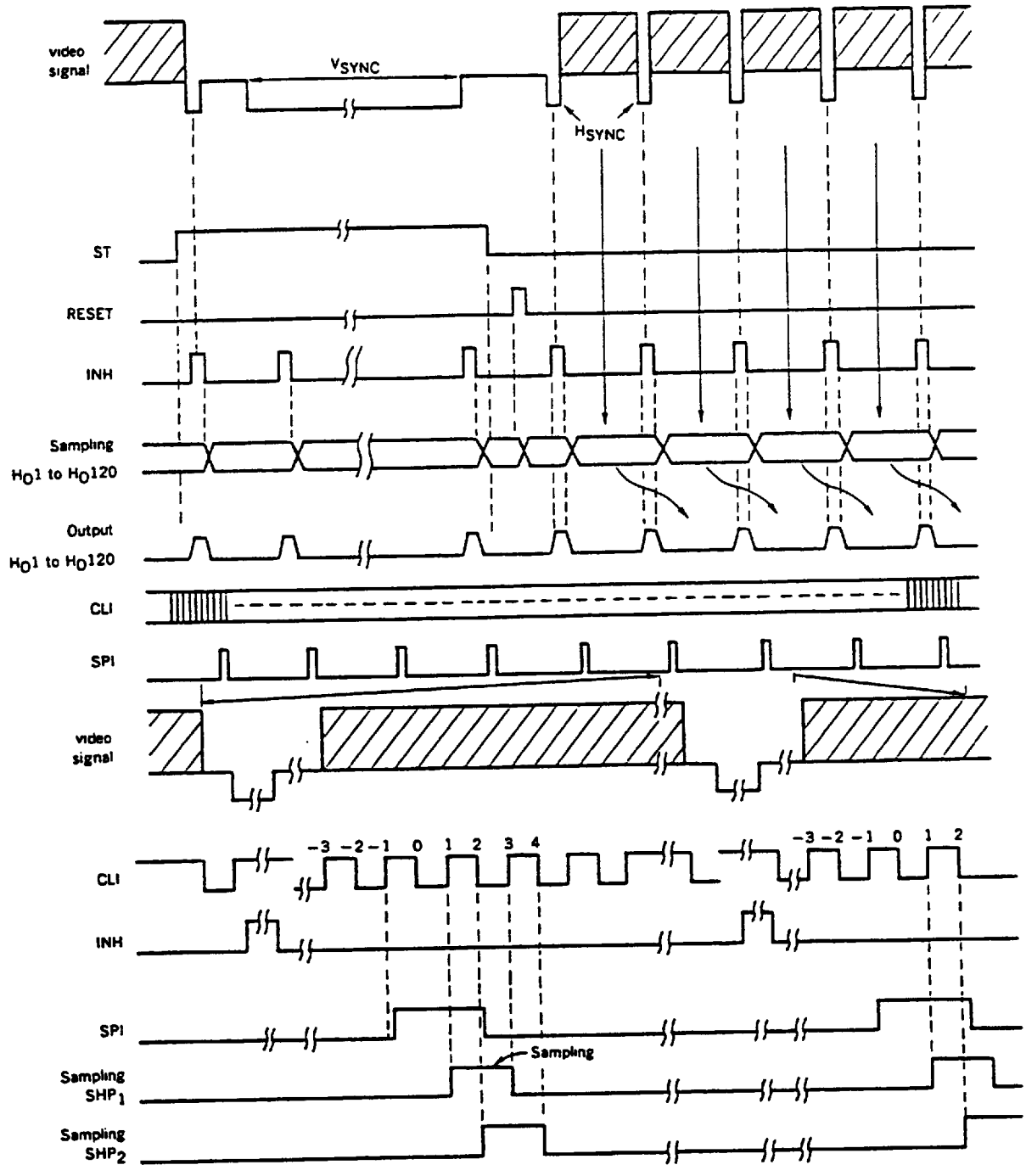


4. Power Saving Circuit

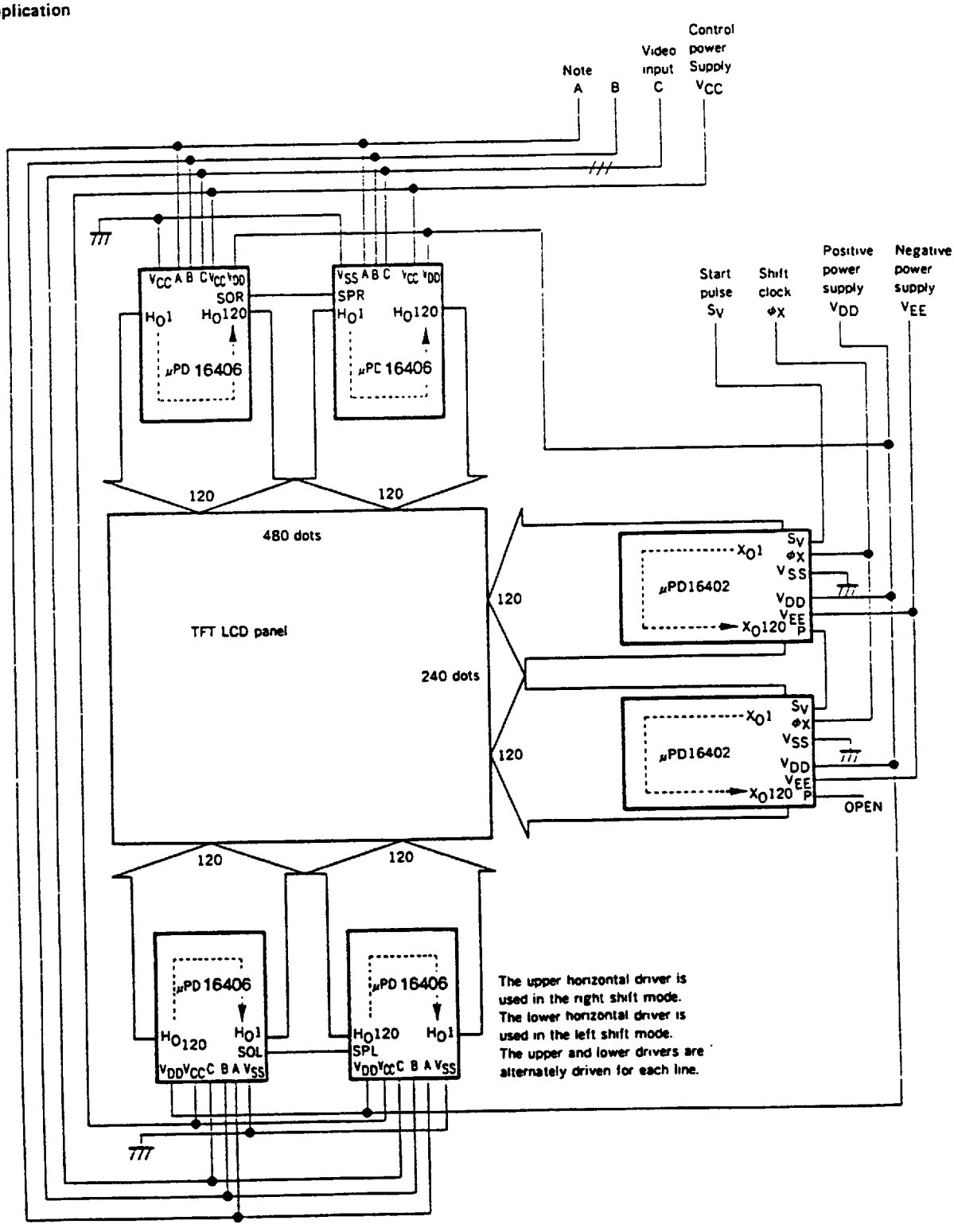
All video output pins can be set at the $V_{DD}$ level as making the level of the power saving pin (ST) to high. In this case, $I_{DD}$ can be reduced. Power consumption can be reduced by inputting a vertical blanking signal to the ST pin.

Timing Chart




ST: Power consumption can be reduced by inputting this signal to the ST pin during the vertical blanking period.

Application




Note: Horizontal driver
A indicates a control pin (RESET, R/L, MP/1.5, MP/TH, INH, or ST).
B indicates a shift clock pin.
C indicates a video input pin ($C_1$, $C_2$, or $C_3$).

The above circuit and constants are given just to explain an application of this chip; they are not for full-scale production.